► Analog multiplexer 8:1

E910.02

FEATURES

- Supply voltage range VDD 4.5V to 5.5V
- Supply voltage range VS 8V to 40V
- Fast buffer amplifier with 1.5V/µs driving 1nF load capacitance
- Low crosstalk in case of current-injection into input-protection diodes
- Low offset voltage < 4mV
- Output voltage limitation to VDD
- Buffer output with high impedance tri-state-mode
- I/O compatible to standard multiplexer 4051
- –40°C to +85°C operating temperature
- SO16n package

APPLICATION

- Buffered analog multiplexing

DESCRIPTION

The IC is an 8 channel analog multiplexer with a buffer amplifier. The input signals IN0 to IN7 are fed to the multiplexer consisting of analog transmission gates which are controlled by the digital inputs SEL0-2. The multiplexer is designed for low crosstalk in case of current injection into the input protection diodes.

VS is used as the positive supply voltage for the buffer and has to be at least 2.5V higher than the maximum analog voltage to avoid clipping or slew rate reduction of the output signal.

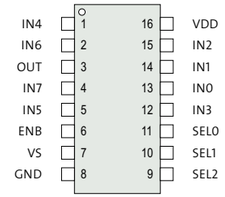
The buffer drives a 1nF load capacitance to avoid EMI disturbance of the output signal. To achieve high output slewrates, this capacitance is used for compensation also and thus has to be applied.

A high level on pin ENB disables the output buffer and switches it into high impedance mode. This allows multiple IC outputs to be connected in parallel. Additionally the VDD current consumption is reduced in tristate mode.

PINNING

Pin	Name	Description
1	IN4	Analog input 4
2	IN6	Analog input 6
3	OUT	Buffer output
4	IN7	Analog input 7
5	IN5	Analog input 5
6	ENB	Enable for buffer output, active low
7	VS	Supply voltage for buffer amplifier
8	GND	Ground
9	SEL2	Control - input for multiplexer
10	SEL1	Control - input for multiplexer
11	SEL0	Control - input for multiplexer
12	IN3	Analog input 3
13	IN0	Analog input 0
14	IN1	Analog input 1
15	IN2	Analog input 2
16	VDD	Voltage for output voltage limitation

PACKAGE



BLOCK DIAGRAM