DI2CM

I²C Bus Interface - Master

ver 3.08

OVERVIEW

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. The DI2CM core provides an interface between a microprocessor / microcontroller and an I²C bus. It can work as a master transmitter or master receiver depending on working mode determined by microprocessor/microcontroller. The DI2CM core incorporates all features required by the latest I²C specification including clock synchronization, arbitration, multi-master systems and High-speed transmission mode. Built-in timer allows operation from a wide range of the clk frequencies.

KEY FEATURES

- Conforms to v.2.1 of the I²C specification
- Master operation
  - *Master transmitter*
  - *Master receiver*
- Support for all transmission speeds
  - *Standard (up to 100 kb/s)*
  - *Fast (up to 400 kb/s)*
  - *High Speed (up to 3,4 Mb/s)*
- Arbitration and clock synchronization
- Support for multi-master systems
- Support for both 7-bit and 10-bit addressing formats on the I²C bus
- Interrupt generation
- Build-in 8-bit timer for data transfers speed adjusting
- Host side interface dedicated for microprocessors/microcontrollers
- User-defined timing (data setup, start setup, start hold, etc.)
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

DELIVERABLES

- Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- Technical documentation
  - ◊ Installation notes

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- HDL core specification
- Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

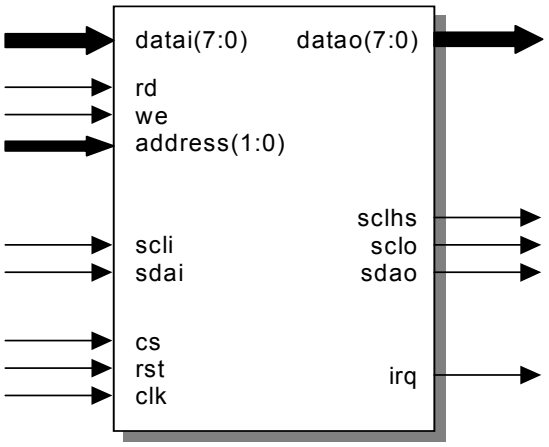
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL

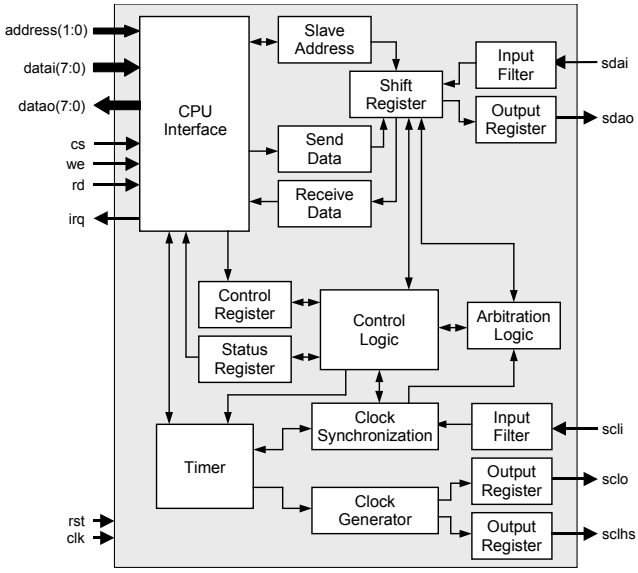


PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
address(1:0)	input	Processor address lines
cs	input	Chip select
we	input	Processor write strobe
rd	input	Processor read strobe
scli	input	I^2C bus clock line (input)
sdai	input	I^2C bus data line (input)
datai(7:0)	input	Processor data bus (input)
datao(7:0)	output	Processor data bus (output)
sclo	output	I^2C bus clock line (output)
sclhs	output	High-speed clock line (output)
sdao	output	I^2C bus data line (output)
irq	output	Processor interrupt line

BLOCK DIAGRAM

Figure below shows the DI2CM IP Core block diagram.



CPU Interface – Performs the interface functions between DI2CM internal blocks and microprocessor. Allows easy connection of the core to a microprocessor/microcontroller system.

Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.

Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.

Control Register – Contains five control bits used for performing all types of I^2C Bus transmissions.

Status Register – Contains seven status bits that indicates state of the I^2C Bus and the DI2CM core.

Clock Generator – Performs generation of the serial clock.

Input Filter – Performs spike filtering.

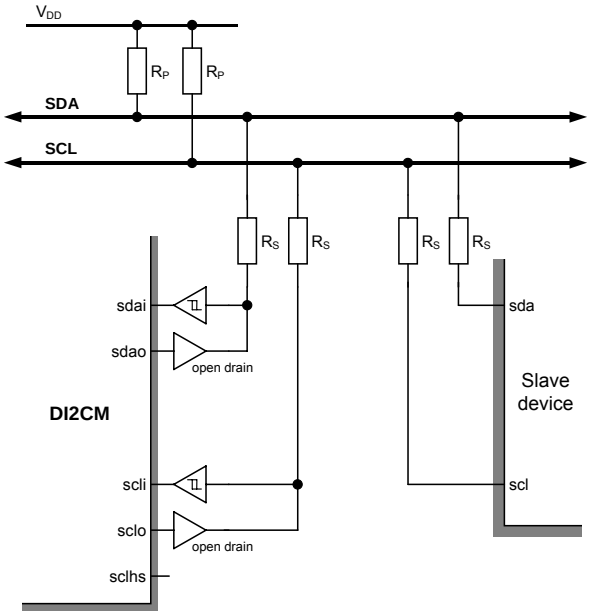
Clock Synchronization – Performs clock synchronization.

Arbitration Logic – Performs arbitration during operations in multi-master systems.

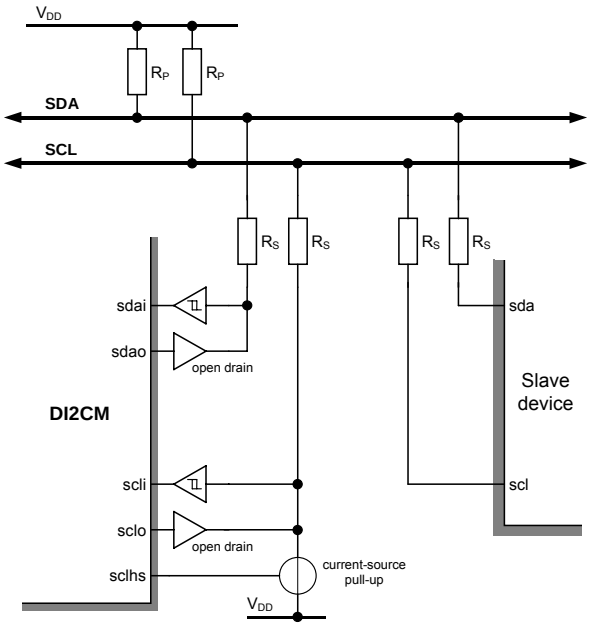
Timer – Allows operation from a wide range of the input frequencies. It is programmed by an user before transmission and can be reprogrammed to change the SCL frequency.

IMPLEMENTATION

Figures below show the typical DI2CM implementations in system with Standard/Fast and High-speed devices.



DI2CM implementation in I^2C-bus system with Standard/Fast devices only



DI2CM implementation in I^2C-bus system with High-speed devices

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F_{max}
STRATIX-II	-3	205	380 MHz
CYCOLNE-II	-6	244	263 MHz
MERCURY	-5	290	210 MHz
STRATIX	-5	241	254 MHz
CYCLONE	-6	241	250 MHz
APEX II	-7	268	192 MHz
APEX20KC	-7	268	180 MHz
APEX20KE	-1	268	160 MHz
APEX20K	-1	268	122 MHz
ACEX1K	-1	287	135 MHz
FLEX10KE	-1	287	140 MHz
MAX 2	-3	241	187 MHz
MAX 7000AE	-5	137	67 MHz
MAX 3000A	-7	137	49 MHz

Core performance in ALTERA® devices

The main features of each Digital Core Design I^2C compliant cores have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application.

Design	I^2C specification version	Master operation	Slave operation	CPU interface	Passive device interface	Interrupt generation	Clock synchronization	Arbitration	7-bit addressing	10-bit addressing	Standard mode	Fast mode	High-speed mode	User defined timing	Spike filtering
DI2CM	2.1	✓	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DI2CS	2.1	-	✓	✓	-	✓	✓	-	✓	-	✓	✓	✓	✓	✓
DI2CSB	2.1	-	✓	-	✓	-	-	-	✓	-	✓	✓	✓	-	✓

I^2C cores summary table

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