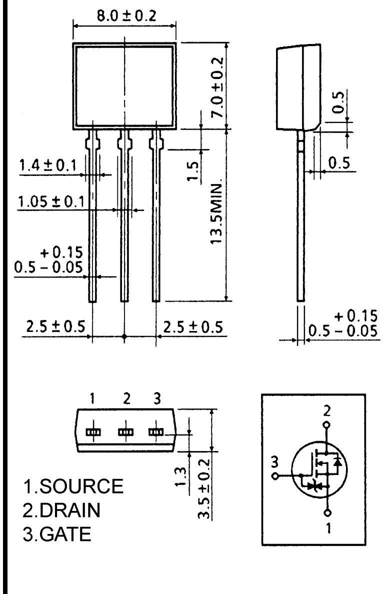
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSV)

2SK3302

Switching Regulator and DC-DC Converter Applications

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-8MIB

Weight: 1.9 g (typ.)

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 11.5 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 0.4 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 500 V)
- Enhancement model: V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	500	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	500	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	0.5	A
	Pulse (Note 1)	I_{DP}	1.5	
Drain power dissipation		P_D	1.3	W
Single pulse avalanche energy (Note 2)		E_{AS}	14.3	mJ
Avalanche current		I_{AR}	0.5	A
Repetitive avalanche energy (Note 3)		E_{AR}	0.13	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	96.1	°C/W

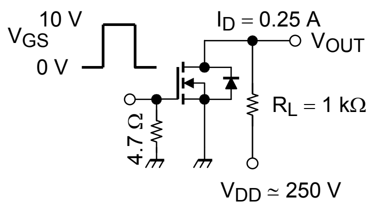
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C, L = 100 mH, R_G = 25 Ω, I_{AR} = 0.5 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature.

This transistor is an electrostatic-sensitive device. Please handle with caution.

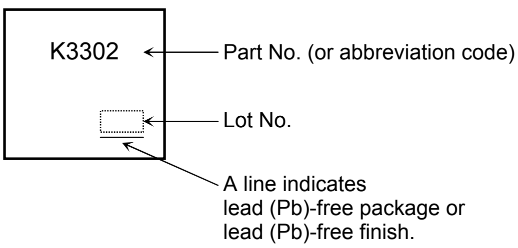
Electrical Characteristics (Ta = 25°C)

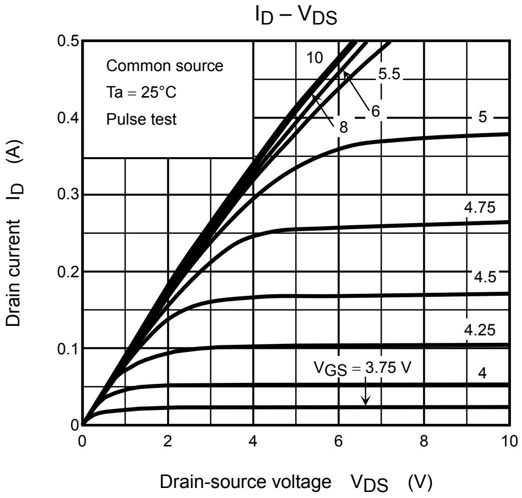
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate-source breakdown voltage	$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{GS} = 0 V	±30	—	—	V
Drain cut-OFF current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	500	—	—	V
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance	$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 0.25 A	—	10	18	Ω
Forward transfer admittance	$\lvert Y_{fs} \rvert$	V_{DS} = 10 V, I_D = 0.25 A	0.2	0.4	—	S
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	75	—	pF
Reverse transfer capacitance	C_{rss}		—	7	—	
Output capacitance	C_{oss}		—	24	—	
Switching time: Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	11	—	ns
Switching time: Turn-ON time	t_{on}		—	18	—	
Switching time: Fall time	t_f		—	54	—	
Switching time: Turn-OFF time	t_{off}		—	95	—	
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≃ 400 V, V_{GS} = 10 V, I_D = 0.5 A	—	3.8	—	nC
Gate-source charge	Q_{gs}		—	1.9	—	
Gate-drain ("miller") charge	Q_{gd}		—	1.9	—	

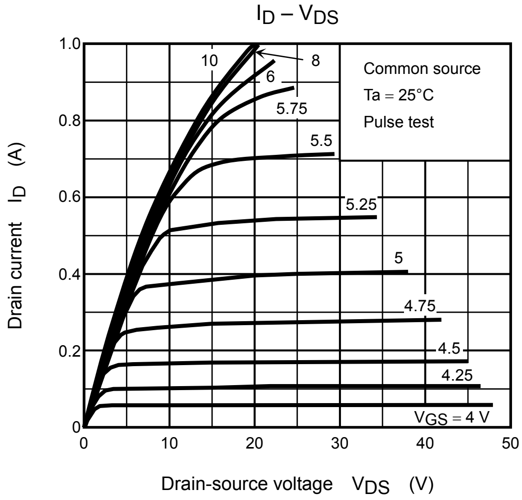
Source-Drain Ratings and Characteristics (Ta = 25°C)

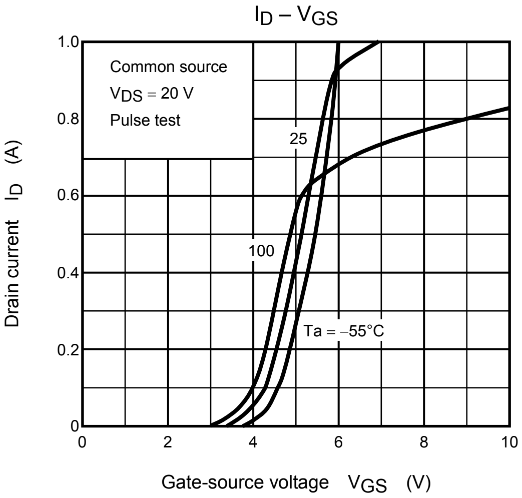
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	0.5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	1.5	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 0.5 A, V_{GS} = 0 V	—	—	−1.5	V
Reverse recovery time	t_{rr}	I_{DR} = 0.5 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	190	—	ns
Reverse recovery charge	Q_{rr}		—	380	—	nC

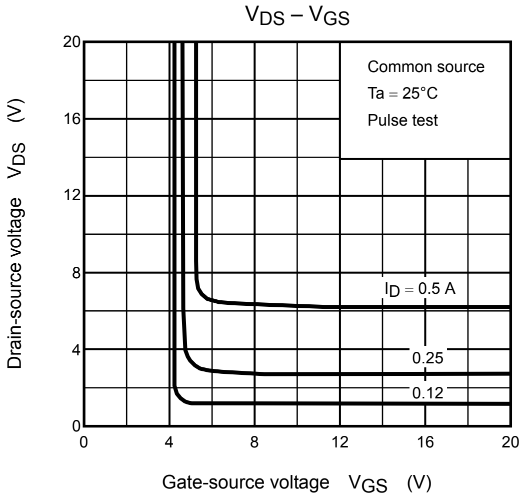
Marking

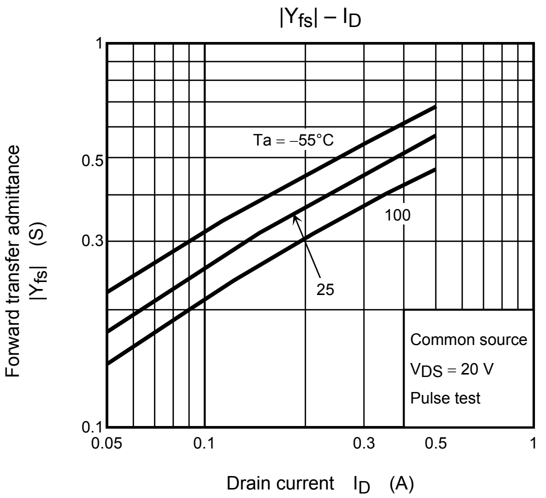


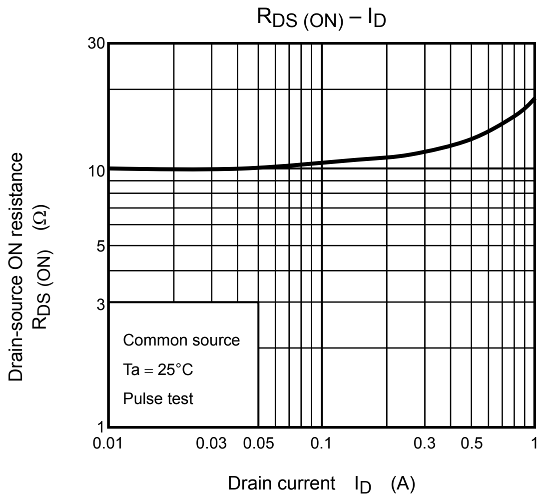

I_D – V_DS
Common source
Ta = 25°C
Pulse test
10
5.5
6
8
5
4.75
4.5
4.25
V_GS = 3.75 V
4
Drain current I_D (A)
Drain-source voltage V_DS (V)

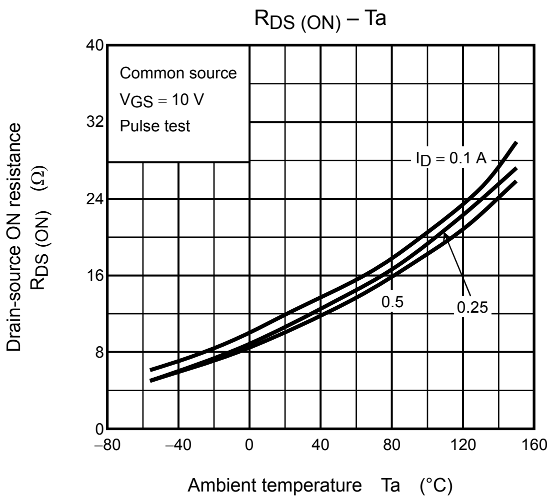

I_D – V_DS
Common source
Ta = 25°C
Pulse test
10
8
6
5.75
5.5
5.25
5
4.75
4.5
4.25
V_GS = 4 V
Drain current I_D (A)
Drain-source voltage V_DS (V)

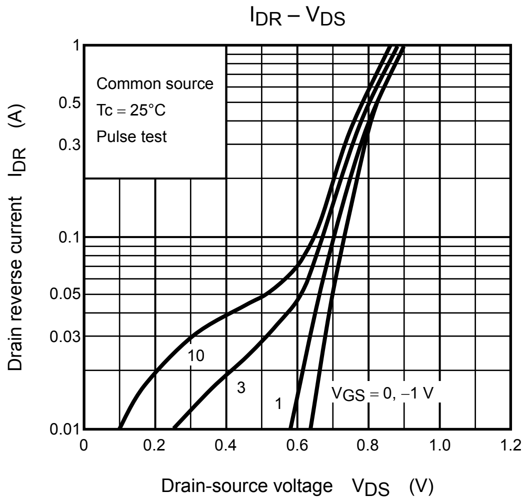

I_D – V_GS
Common source
V_DS = 20 V
Pulse test
25
100
Ta = −55°C
Drain current I_D (A)
Gate-source voltage V_GS (V)

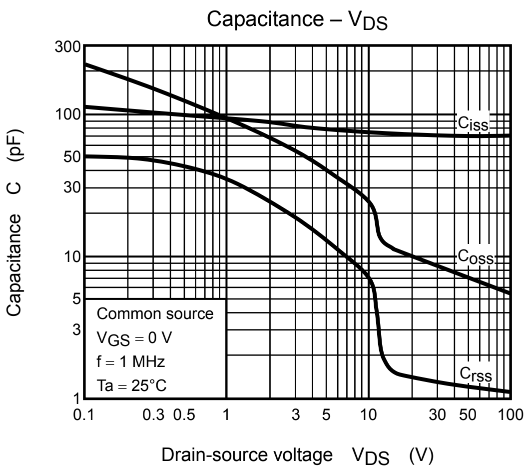

V_DS – V_GS
Common source
Ta = 25°C
Pulse test
I_D = 0.5 A
0.25
0.12
Drain-source voltage V_DS (V)
Gate-source voltage V_GS (V)

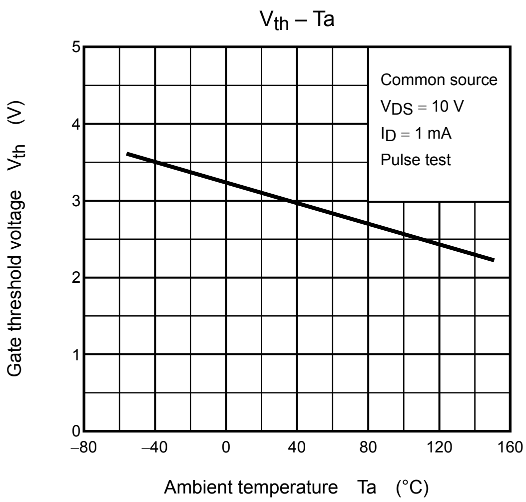

|Y_fs| – I_D
Ta = −55°C
100
25
Common source
V_DS = 20 V
Pulse test
Forward transfer admittance |Y_fs| (S)
Drain current I_D (A)

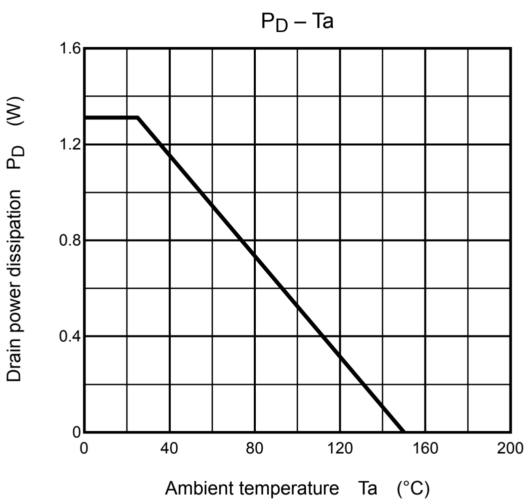

R_DS (ON) – I_D
Common source
Ta = 25°C
Pulse test
Drain-source ON resistance R_DS (ON) (Ω)
Drain current I_D (A)

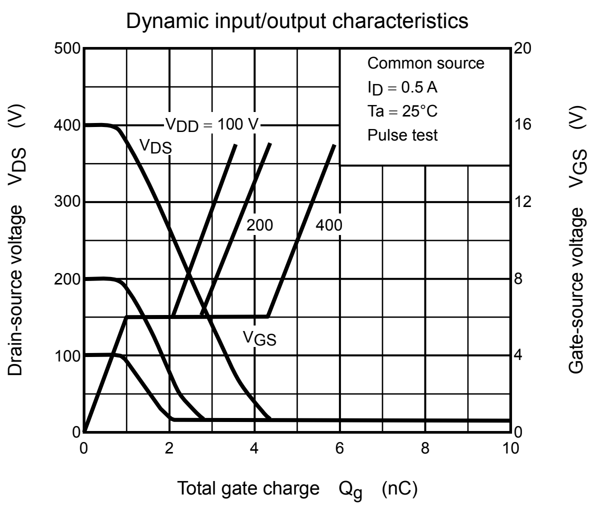

RDS (ON) – Ta
Common source
VGS = 10 V
Pulse test
ID = 0.1 A
0.5
0.25
Drain-source ON resistance RDS (ON) (Ω)
Ambient temperature Ta (°C)


IDR – VDS
Common source
Tc = 25°C
Pulse test
10
3
1
VGS = 0, −1 V
Drain reverse current IDR (A)
Drain-source voltage VDS (V)

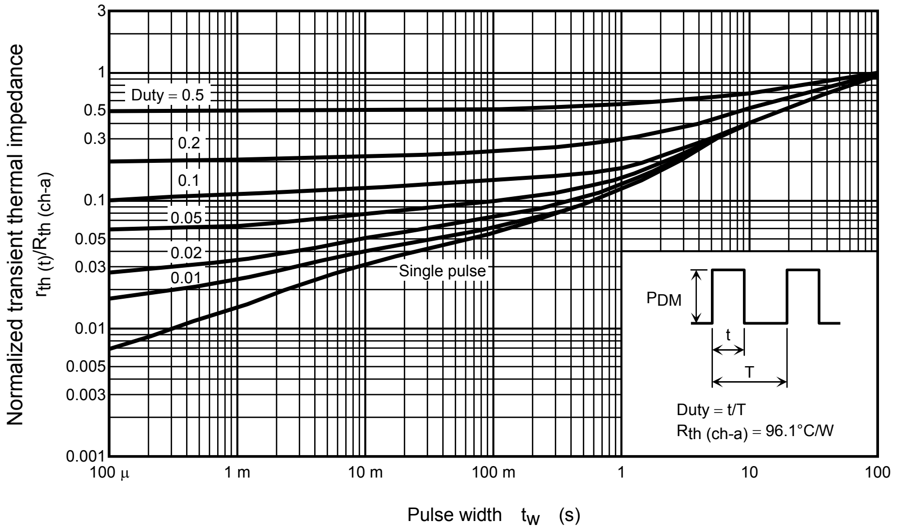

Capacitance – VDS
Ciss
Coss
Crss
Common source
VGS = 0 V
f = 1 MHz
Ta = 25°C
Capacitance C (pF)
Drain-source voltage VDS (V)


Vth – Ta
Common source
VDS = 10 V
ID = 1 mA
Pulse test
Gate threshold voltage Vth (V)
Ambient temperature Ta (°C)

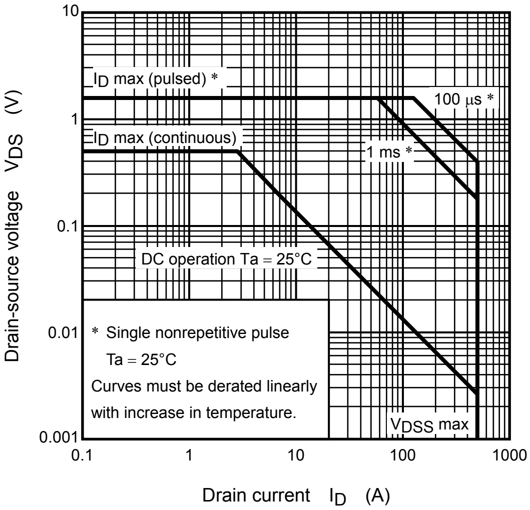

PD – Ta
Drain power dissipation PD (W)
Ambient temperature Ta (°C)


Dynamic input/output characteristics
Common source
ID = 0.5 A
Ta = 25°C
Pulse test
VDD = 100 V
VDS
200
400
VGS
Drain-source voltage VDS (V)
Gate-source voltage VGS (V)
Total gate charge Qg (nC)

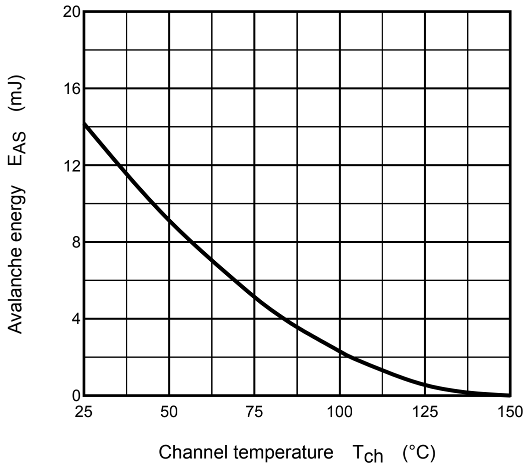
$r_{th} - t_w$

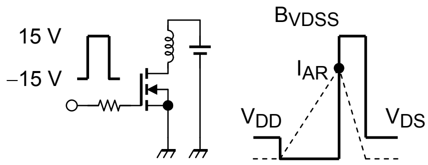


Safe operating area



$E_{AS} - T_{ch}$





Test circuit Wave form

R_G = 25 Ω
V_{DD} = 90 V, L = 100 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

RESTRICTIONS ON PRODUCT USE

20070701-EN