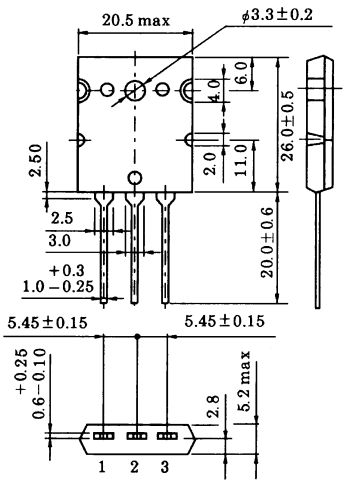
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSIII$^{.5}$)

2SK1486

Chopper Regulator, DC−DC Converter and Motor Drive Applications

- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.08 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 14 S (typ.)
- Low leakage current : I_{DSS} = 300 μA (max) (V_{DS} = 300 V)
- Enhancement mode : V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-21F1B

Weight: 9.75 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	300	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	300	V
Gate−source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	32	A
	Pulse (Note 1)	I_{DP}	128	
Drain power dissipation (Tc = 25°C)		P_D	200	W
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

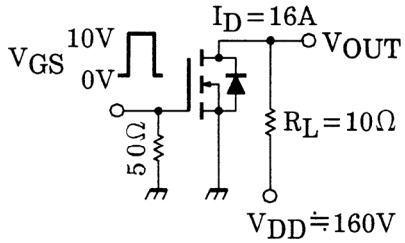
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	0.625	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	35.7	°C / W

Note 1: Ensure that the channel temperature does not exceed 150°C.

This transistor is an electrostatic-sensitive device.
Please handle with caution.

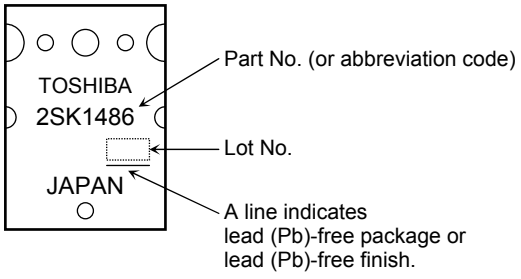
Electrical Characteristics (Ta = 25°C)

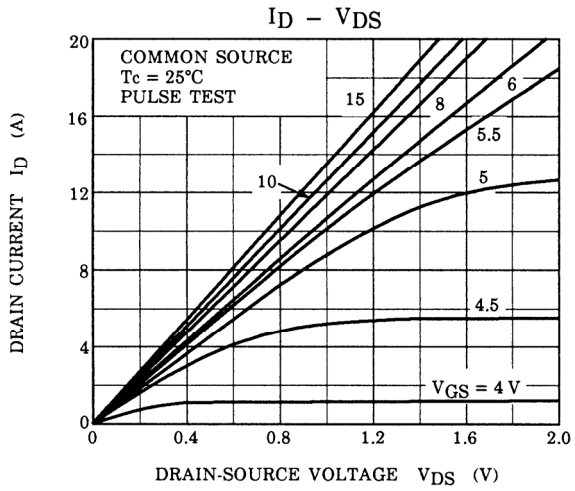
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±100	nA
Drain cut−off current		I_{DSS}	V_{DS} = 300 V, V_{GS} = 0 V	—	—	300	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	300	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	I_D = 16 A, V_{GS} = 10 V	—	0.08	0.095	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 16 A	10	14	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	3500	—	pF
Reverse transfer capacitance		C_{rss}		—	800	—	
Output capacitance		C_{oss}		—	1250	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, $t_w = 10\mu s$	—	255	—	ns
	Turn−on time	t_{on}		—	325	—	
	Fall time	t_f		—	280	—	
	Turn−off time	t_{off}		—	540	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 240 V, V_{GS} = 10 V, I_D = 32 A	—	140	—	nC
Gate−source charge		Q_{gs}		—	60	—	
Gate−drain (“miller”) charge		Q_{gd}		—	80	—	

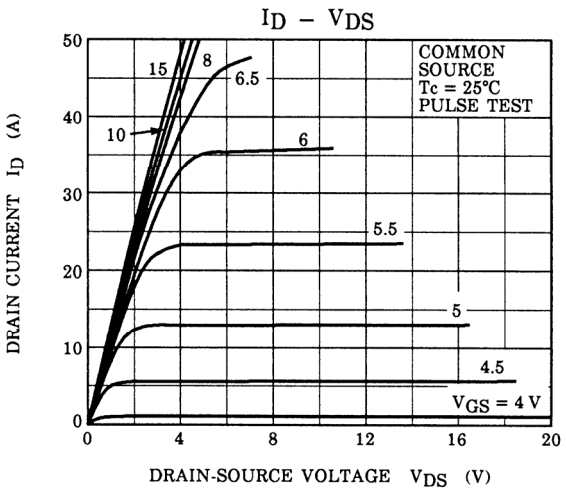
Source−Drain Ratings and Characteristics (Ta = 25°C)

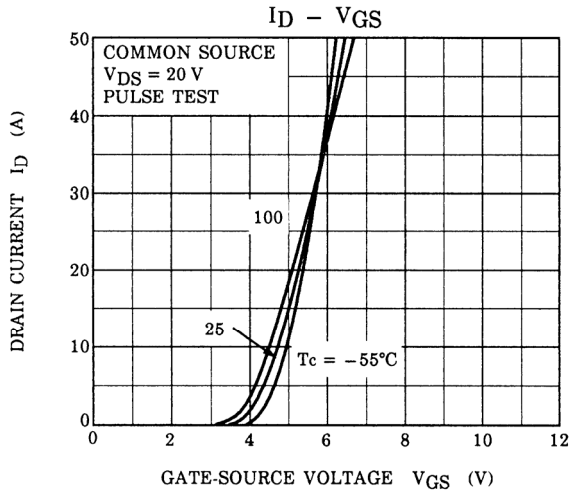
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	32	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	128	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 32 A, V_{GS} = 0 V	—	—	−1.8	V
Reverse recovery time	t_{rr}	I_{DR} = 32 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	615	—	ns
Reverse recovered charge	Q_{rr}		—	6.8	—	μC

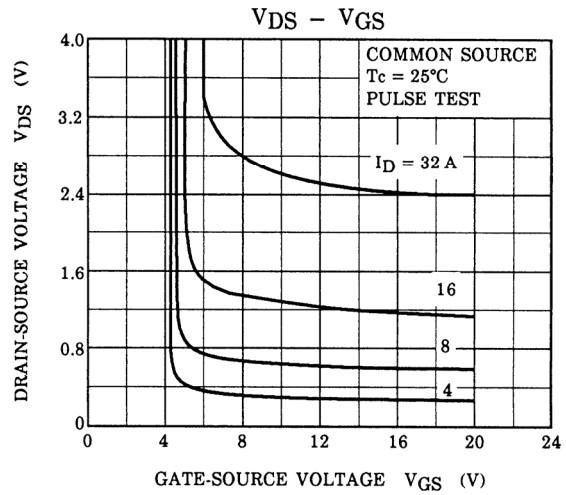
Marking

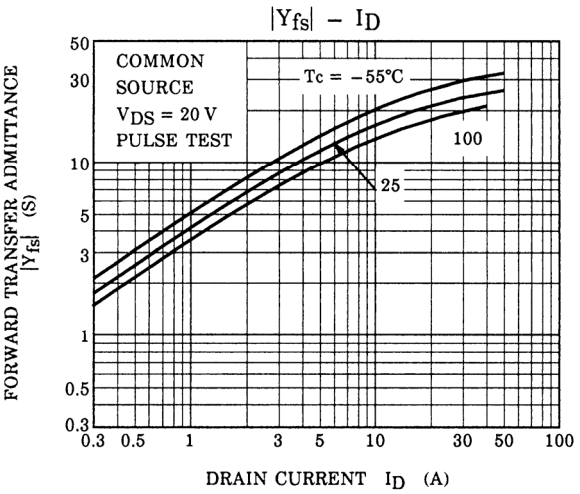


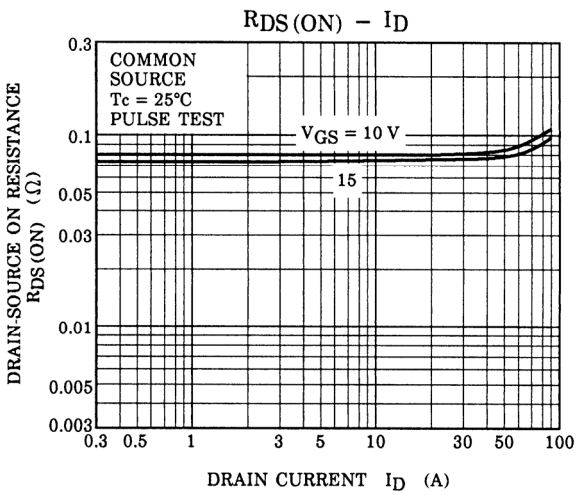

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
15
8
6
5.5
5
10
4.5
V_{GS} = 4 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
0
0.4
0.8
1.2
1.6
2.0
4
8
12
16
20


I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
15
8
6.5
10
6
5.5
5
4.5
V_{GS} = 4 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
0
4
8
12
16
20
10
30
40
50

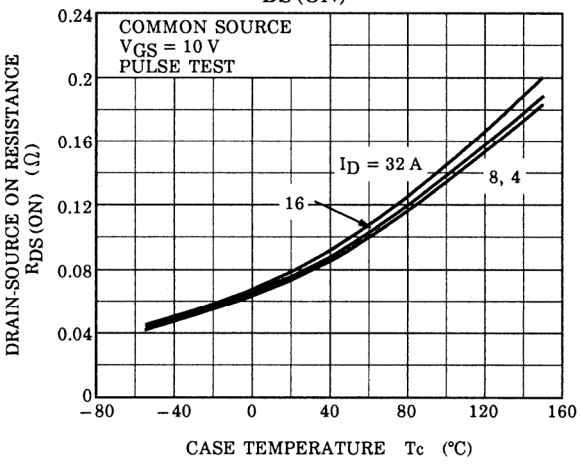

I_D – V_{GS}
COMMON SOURCE
V_{DS} = 20 V
PULSE TEST
100
25
Tc = −55°C
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)
0
2
4
6
8
10
12
20
30
40
50


V_{DS} – V_{GS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = 32 A
16
8
4
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)
0
0.8
1.6
2.4
3.2
4.0
4
8
12
16
20
24

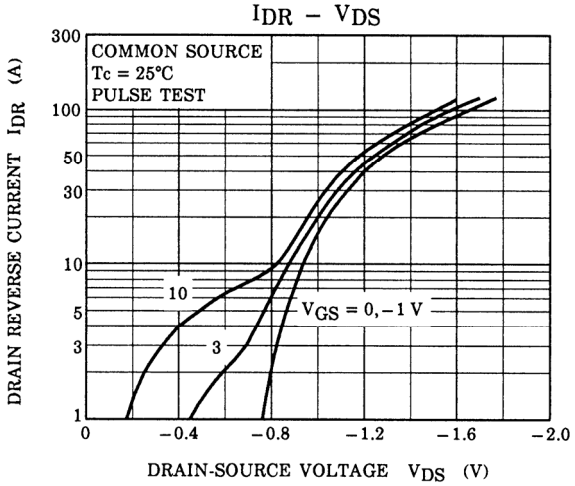

$|Y_{fs}|$ – I_D
COMMON SOURCE
V_{DS} = 20 V
PULSE TEST
Tc = −55°C
100
25
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)
0.3
0.5
1
3
5
10
30
50
100


$R_{DS\,(ON)}$ – I_D
COMMON SOURCE
Tc = 25°C
PULSE TEST
V_{GS} = 10 V
15
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (Ω)
DRAIN CURRENT I_D (A)
0.003
0.005
0.01
0.03
0.05
0.1
0.3
0.3
0.5
1
3
5
10
30
50
100

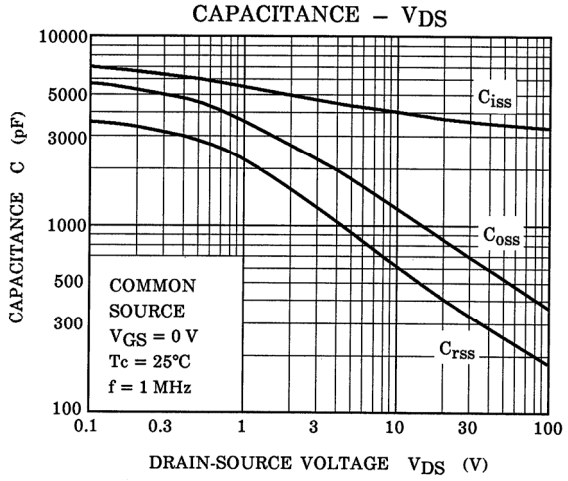
$R_{DS\,(ON)}$ – Tc



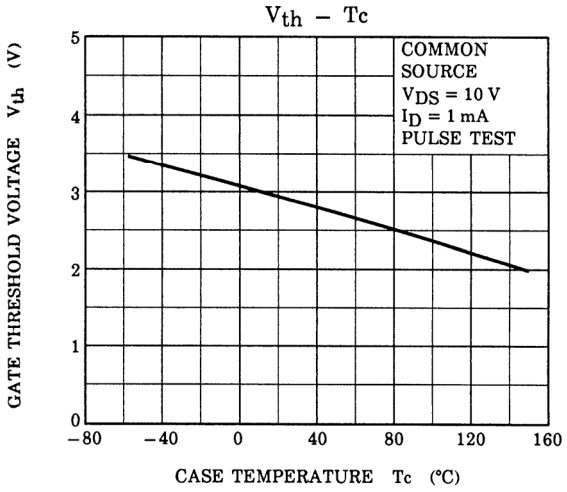
I_{DR} – V_{DS}



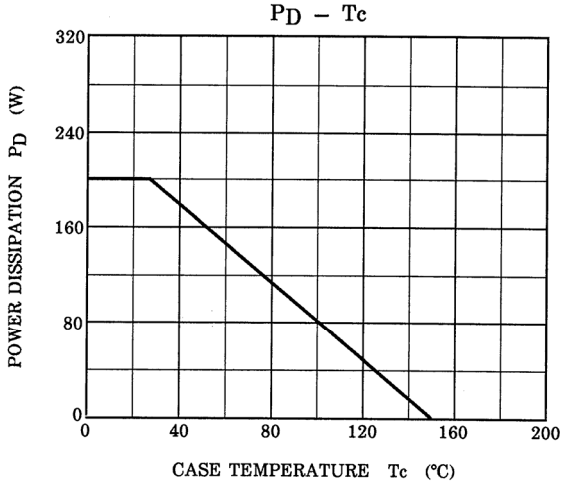
CAPACITANCE – V_{DS}

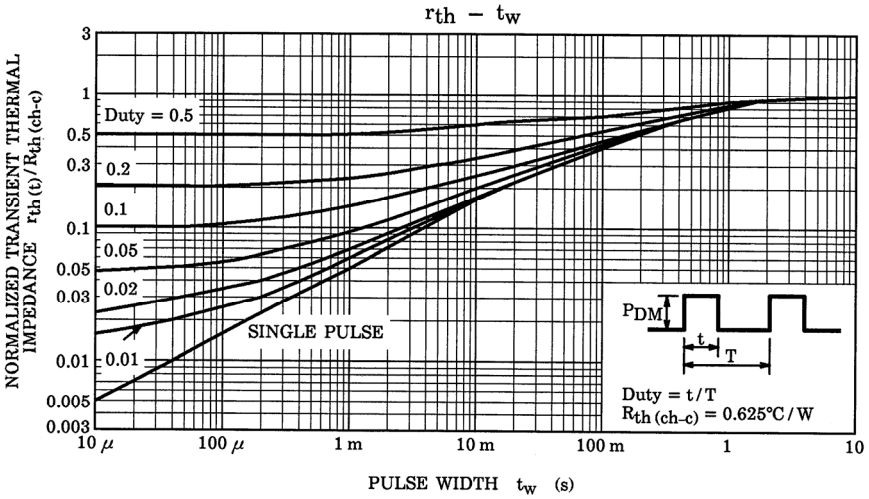


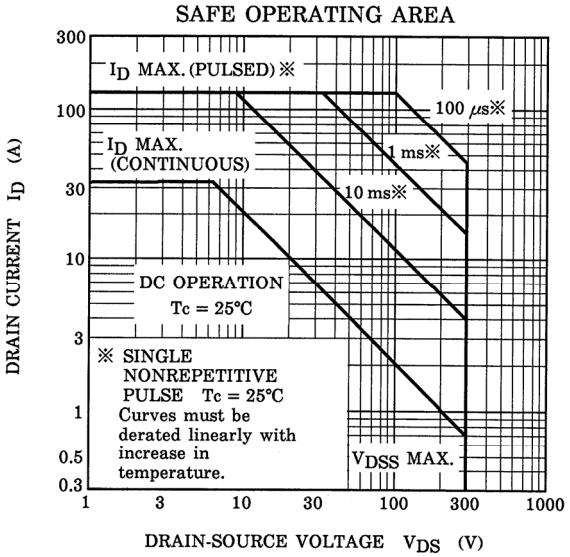
V_{th} – Tc



P_D – Tc




rth – tw
NORMALIZED TRANSIENT THERMAL IMPEDANCE rth (t)/Rth (ch-c)
3
1
0.5
0.3
0.1
0.05
0.03
0.01
0.005
0.003
Duty = 0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE
PDM
t
T
Duty = t/T
Rth (ch-c) = 0.625°C/W
10 μ
100 μ
1 m
10 m
100 m
1
10
PULSE WIDTH tw (s)


SAFE OPERATING AREA
DRAIN CURRENT ID (A)
300
100
30
10
3
1
0.5
0.3
ID MAX. (PULSED) ※
100 μs※
1 ms※
ID MAX. (CONTINUOUS)
10 ms※
DC OPERATION
Tc = 25°C
※ SINGLE NONREPETITIVE PULSE Tc = 25°C
Curves must be derated linearly with increase in temperature.
VDSS MAX.
1
3
10
30
100
300
1000
DRAIN-SOURCE VOLTAGE VDS (V)

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