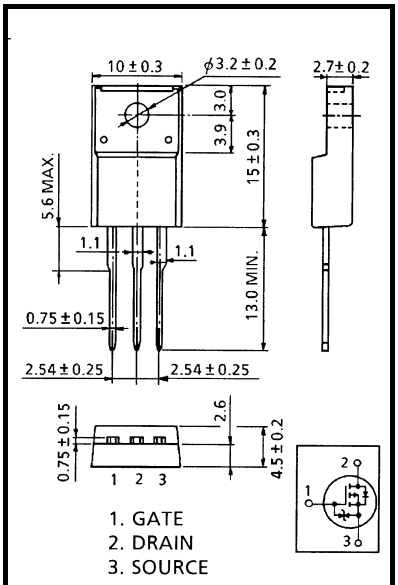
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (π−MOSV)

2SJ407

Chopper Regulator, DC−DC Converter and Motor Drive Applications

- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.8 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 4.0 S (typ.)
- Low leakage current : I_{DSS} = −100 μA (max) (V_{DS} = −200 V)
- Enhancement mode : V_{th} = −1.5~−3.5 V (V_{DS} = −10 V, I_D = −1 mA)

Unit: mm



JEDEC	—
JEITA	SC-67
TOSHIBA	2-10R1B

Weight: 1.9 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	−200	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−200	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	−5	A
	Pulse (Note 1)	I_{DP}	−20	A
Drain power dissipation (Tc = 25°C)		P_D	30	W
Single pulse avalanche energy (Note 2)		E_{AS}	195	mJ
Avalanche current		I_{AR}	−5	A
Repetitive avalenche energy (Note 3)		E_{AR}	3.0	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	4.16	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C / W

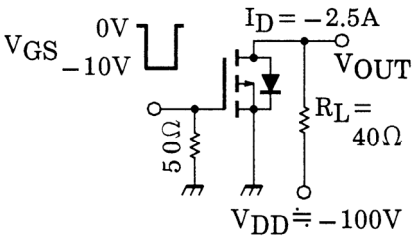
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = −50 V, T_{ch} = 25°C (initial), L = 12.6 mH, R_G = 25 Ω, I_{AR} = −5 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device.
Please handle with caution.

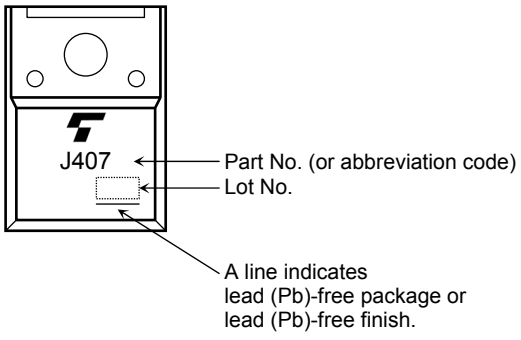
Electrical Characteristics (Ta = 25°C)

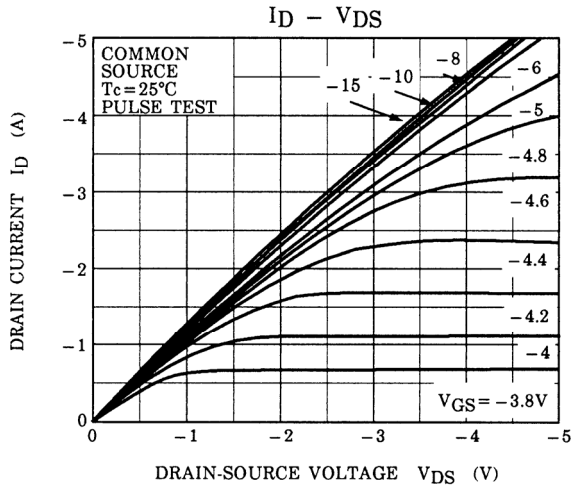
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = −200 V, V_{GS} = 0 V	—	—	−100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−200	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−1.5	—	−3.5	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −10 V, I_D = −2.5 A	—	0.8	1.0	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.5 A	2.0	4.0	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	800	—	pF
Reverse transfer capacitance		C_{rss}		—	80	—	
Output capacitance		C_{oss}		—	270	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn−on time	t_{on}		—	30	—	
	Fall time	t_f		—	6	—	
	Turn−off time	t_{off}		—	65	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ −160 V, V_{GS} = −10 V, I_D = −5 A	—	20	—	nC
Gate−source charge		Q_{gs}		—	13	—	
Gate−drain (“miller”) charge		Q_{gd}		—	7	—	

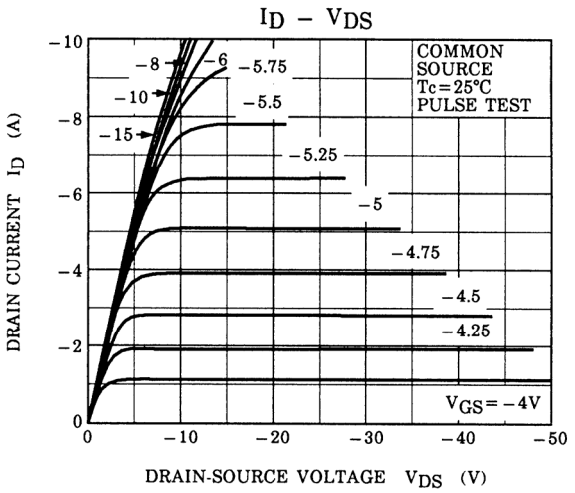
Source−Drain Ratings and Characteristics (Ta = 25°C)

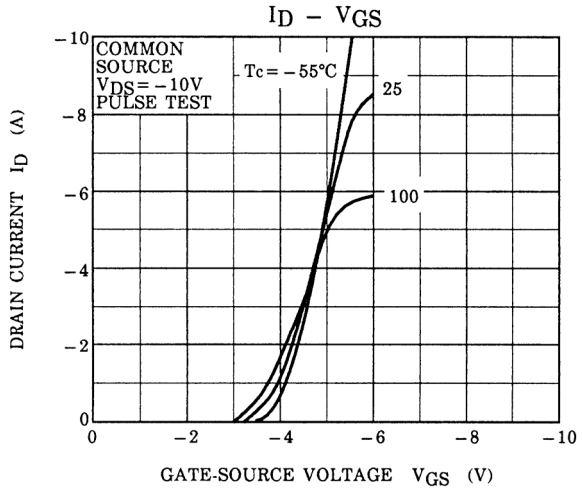
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	−5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	−20	A
Forward voltage (diode)	V_{DSF}	I_{DR} = −5 A, V_{GS} = 0 V	—	—	2.0	V
Reverse recovery time	t_{rr}	I_{DR} = −5 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	210	—	ns
Reverse recovery charge	Q_{rr}		—	1.2	—	μC

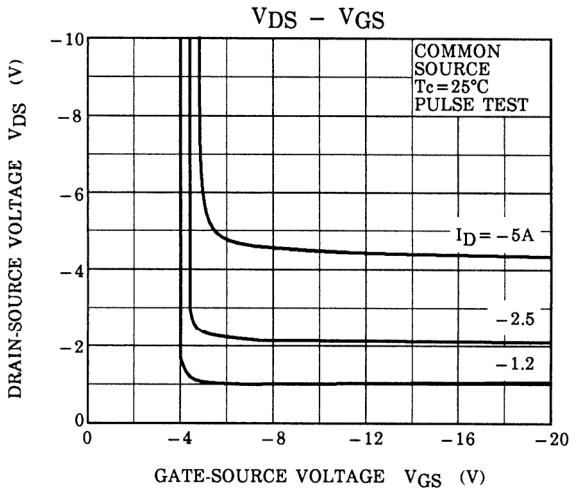
Marking

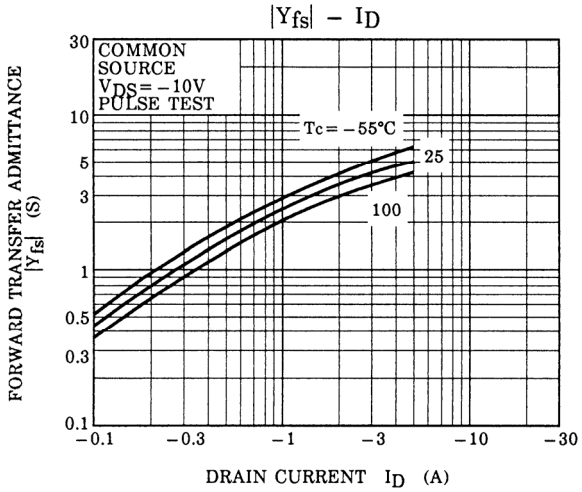


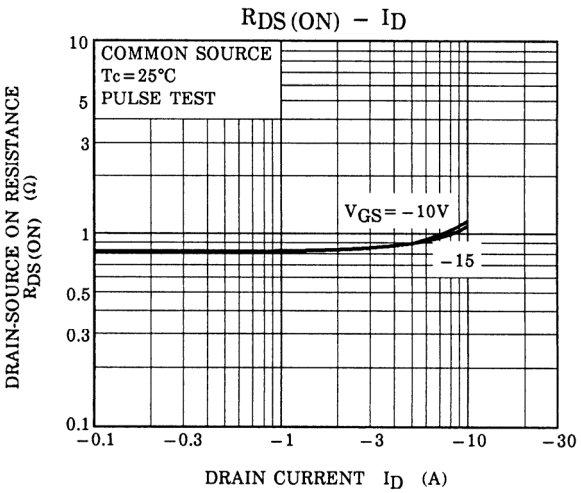

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
−8
−6
−15
−10
−5
−4.8
−4.6
−4.4
−4.2
−4
V_{GS} = −3.8V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
−8
−6
−5.75
−10
−5.5
−15
−5.25
−5
−4.75
−4.5
−4.25
V_{GS} = −4V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)

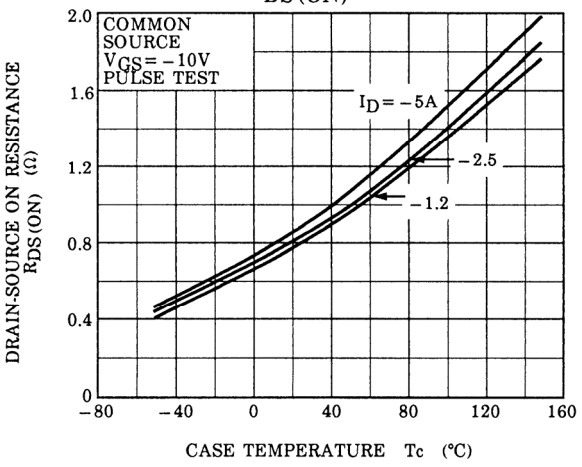

I_D – V_{GS}
COMMON SOURCE
V_{DS} = −10V
PULSE TEST
Tc = −55°C
25
100
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)


V_{DS} – V_{GS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = −5A
−2.5
−1.2
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)

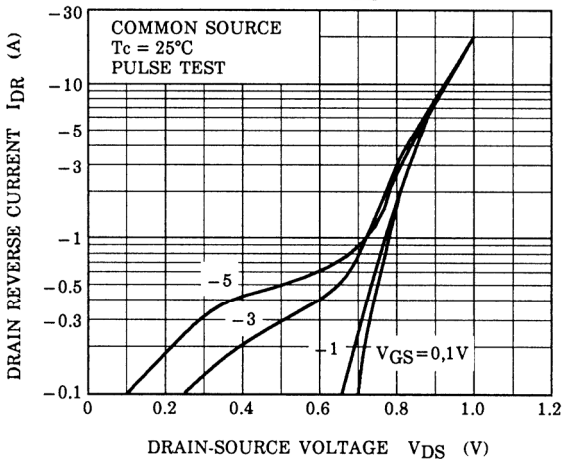

$|Y_{fs}|$ – I_D
COMMON SOURCE
V_{DS} = −10V
PULSE TEST
Tc = −55°C
25
100
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)


$R_{DS(ON)}$ – I_D
COMMON SOURCE
Tc = 25°C
PULSE TEST
V_{GS} = −10V
−15
DRAIN-SOURCE ON RESISTANCE $R_{DS(ON)}$ (Ω)
DRAIN CURRENT I_D (A)

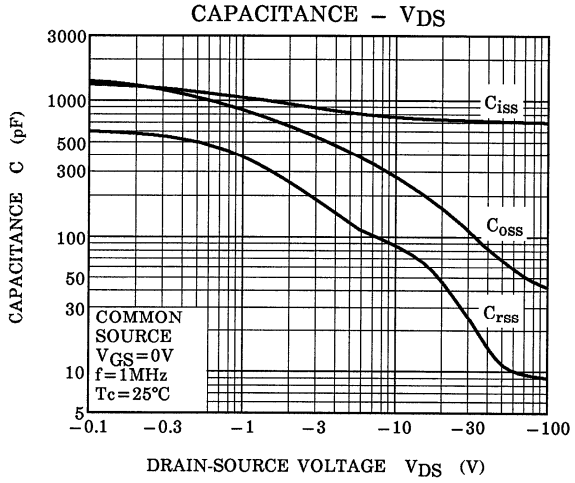
$R_{DS\,(ON)}$ – Tc



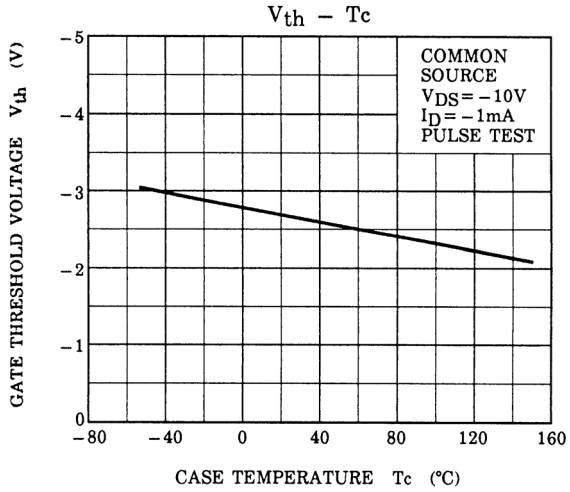
I_{DR} – V_{DS}



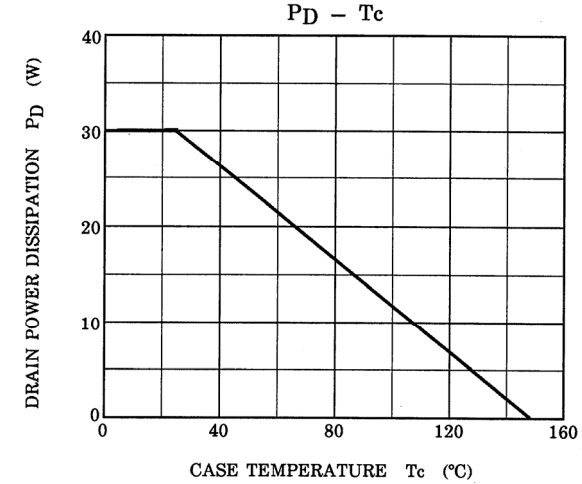
CAPACITANCE – V_{DS}



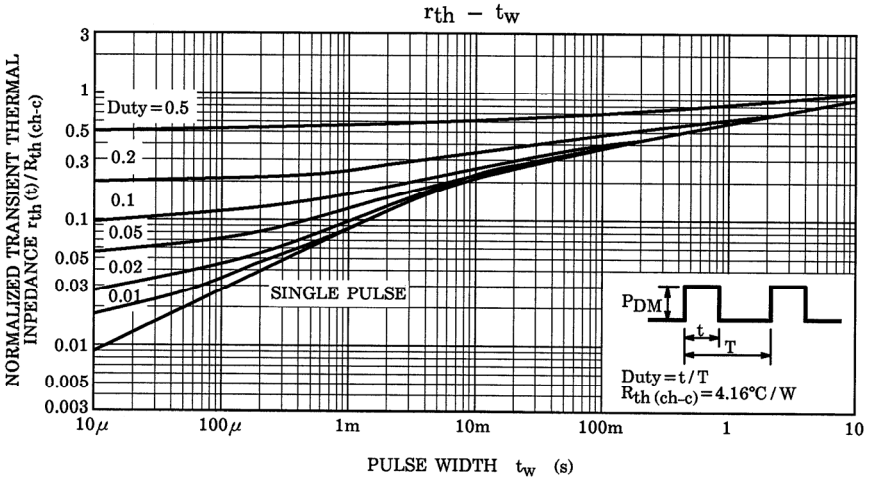
V_{th} – Tc



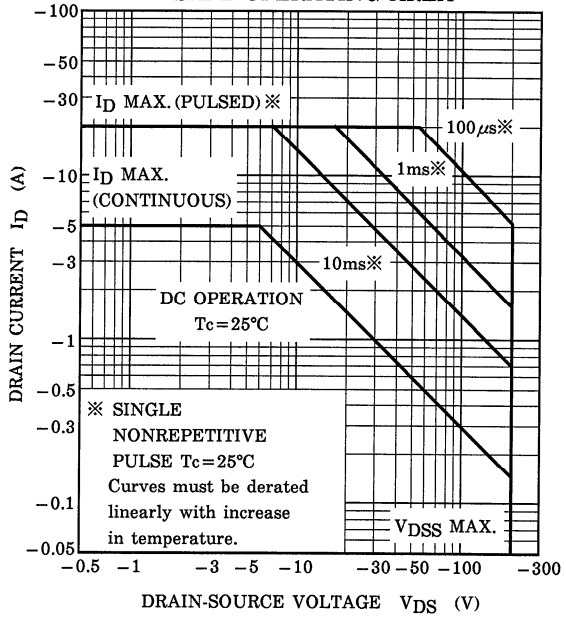
P_D – Tc



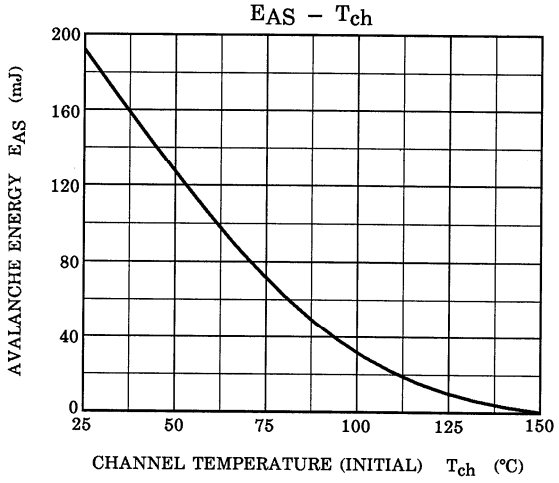
$r_{th} - t_w$

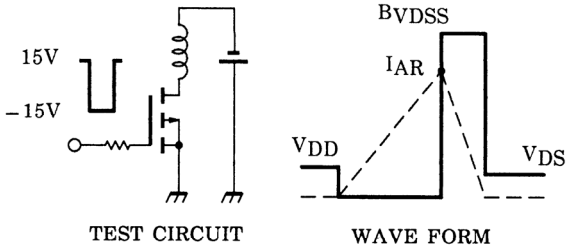


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





$R_G = 25\Omega$
$V_{DD} = -50V$, L = 12.6mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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