



# QUAD BI-DIRECTIONAL TVS/ZENER FOR ESD PROTECTION

This Quad TVS/Zener Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.

### **SPECIFICATION FEATURES**

- 150W Power Dissipation (8/20µs Waveform)
- Low Leakage Current, Maximum of 1µA @ 5Vdc
- Very low Clamping voltage (Max of 10V @ 14A 8/20µs)
- IEC61000-4-2 ESD 15kV air, 8kV Contact Compliance
- Industry standard SOT23-6L
- 100% Tin Matte Finish (RoHS Compliant)

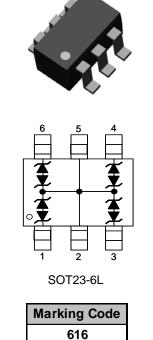
#### **APPLICATIONS**

- Personal Digital Assistant (PDA)
- SIM Card Port Protection (Mobile Phone)
- Portable Instrumentation
- Mobile Phones and Accessories
- Computer Data Ports

Rating	Symbol	Value	Units				
Peak Pulse Power (8/20µs Waveform)	P pp	150	W				
Peak Pulse Current (8/20µs Waveform)	۱ <sub>pp</sub>	14	А				
ESD Voltage (HBM)	V <sub>ESD</sub>	>25	kV				
Operating Temperature Range	Тј	-55 to +150	°C				
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C				

#### ELECTRICAL CHARACTERISTICS Tj = 25°C

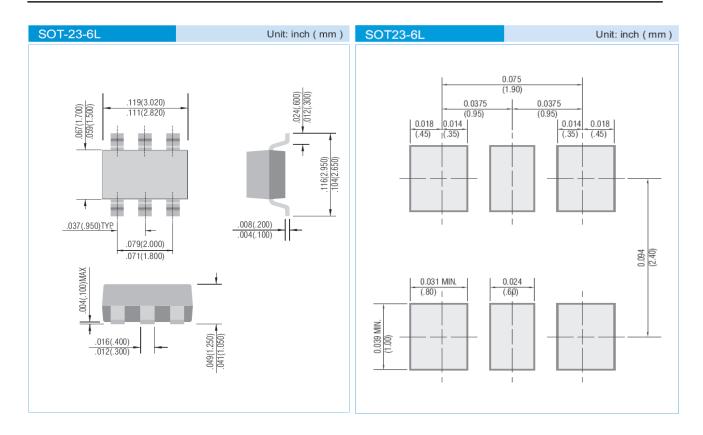
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V <sub>WRM</sub>				5	V
Reverse Breakdown Voltage	$V_{BR}$	I <sub>BR</sub> =1 mA	6.2		7.2	V
Reverse Leakage Current	۱ <sub>R</sub>	$V_R = 5V$			1	μΑ
Clamping Voltage (8/20µs)	Vc	I <sub>pp</sub> =5 Amps			11	V
Clamping Voltage (8/20µs)	Vc	I <sub>pp</sub> = 10 Amps			13	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 7			90	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 7			50	pF







# PACKAGE LAYOUT DIMENSIONS



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