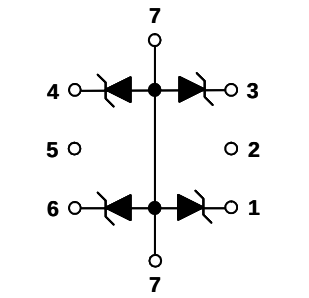
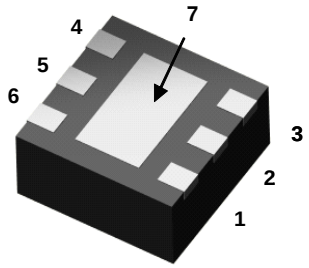
QUAD TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This Quad TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.





QFN 2X2
Bottom View

SPECIFICATION FEATURES

- **350W Power Dissipation (8x20µsec Waveform)**
- **Low Leakage Current, Maximum of 5µA at rated voltage**
- **Very Low Clamping Voltage**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **New SMT package QFN 2mm x 2mm (Height 0.75mm) Compatible with the SOT363 footprint.**

APPLICATIONS

- **Personal Digital Assistant (PDA)**
- **SIM Card Port Protection (Mobile Phone)**
- **Portable Instrumentation**
- **Mobile Phones and Accessories**
- **Memory Card Port Protection**

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8x20µsec Waveform)	P_{pp}	350	W
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-50 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJQMS05

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1mA	6			V
Reverse Leakage Current	I_R	V_R = 5V			5	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			9.8	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 24A			13	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 7			225	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 7			125	pF

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJQMS12

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	13.3			V
Reverse Leakage Current	I_R	V_R = 12V			1	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			20	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 15A			25	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 7			100	pF

PJQMS15

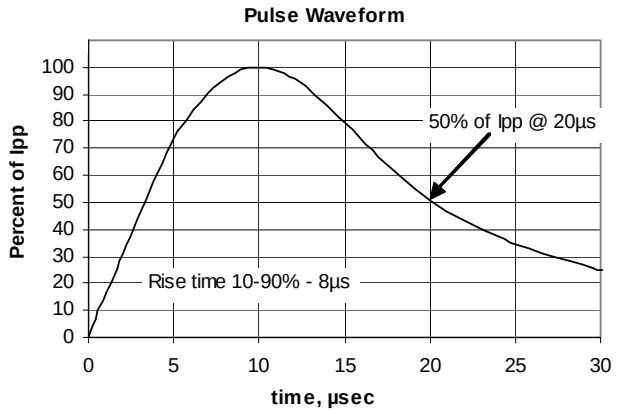
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	16.7			V
Reverse Leakage Current	I_R	V_R = 15V			1	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			24	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 12A			29	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 7			80	pF

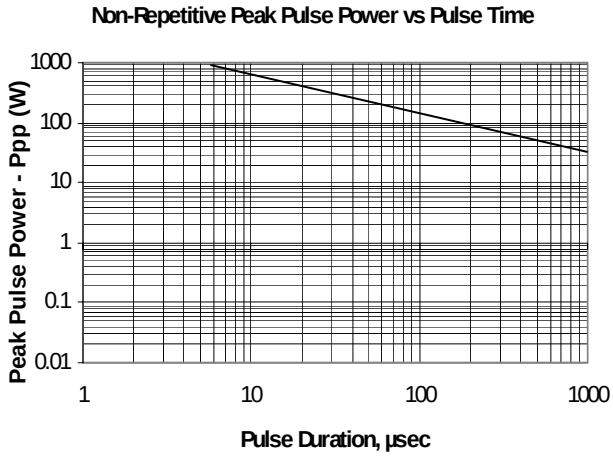
PJQMS24

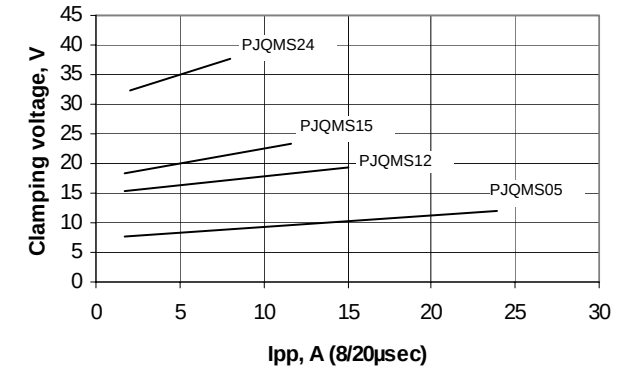
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	26.7			V
Reverse Leakage Current	I_R	V_R = 24V			1	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			40	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 8A			44	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 7			60	pF

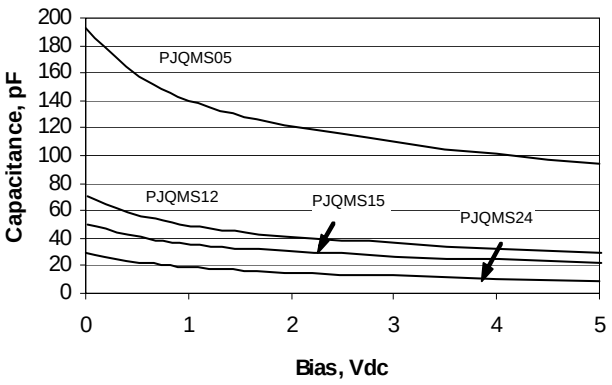
TYPICAL CHARACTERISTICS TJ = 25°C unless otherwise noted

Surge Pulse Waveform Definition

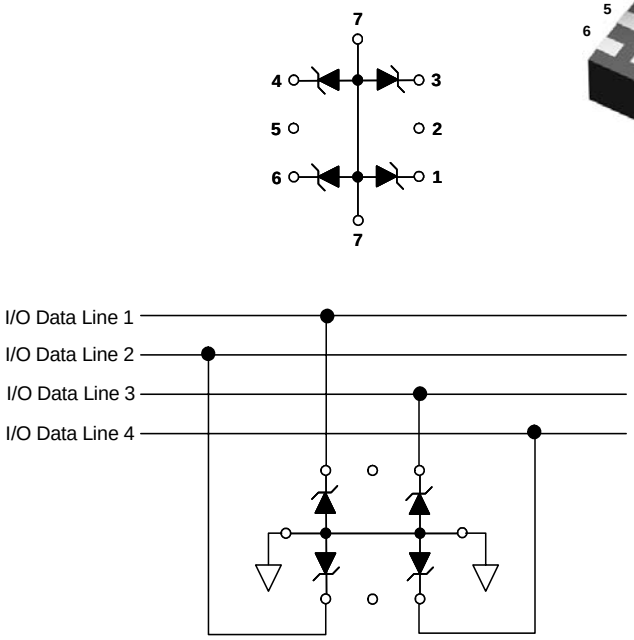


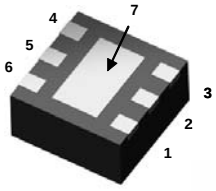




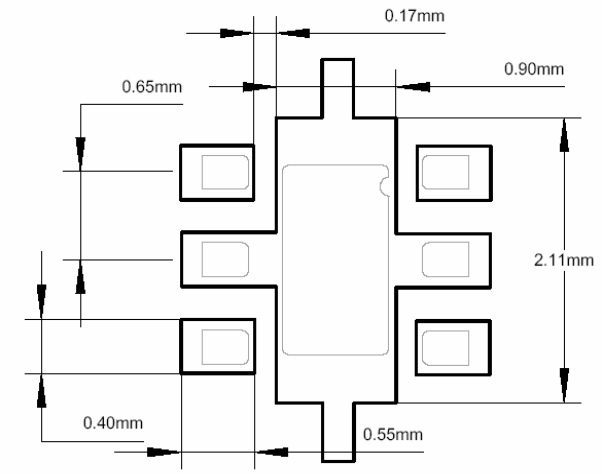


TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS (in mm)





SUGGESTED PAD LAYOUT



Note: pin 2 and pin 7 could be fused with the pin 7 in order to make ground connection to these pins.