

DUAL ULTRA LOW CAPACITANCE ESD PROTECTOR ARRAY

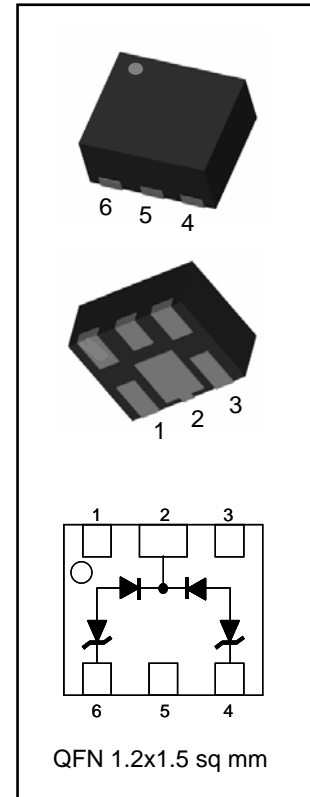
This Dual Unidirectional ESD Protector Array family have been designed to protect sensitive equipment against ESD in high speed transmission buses, operating at 5V and demanding the lowest insertion loss. This array offers an integrated solution to protect up to 2 data lines in applications, where the board space is a premium, in a Quad Flat no-Lead package that only occupies an area of 1.8 sq mm.

SPECIFICATION FEATURES

- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- Low Leakage Current, Maximum of 1μA at rated voltage
- Maximum Capacitance of 1pF per device at 0Vdc 1MHz
- Peak Power Dissipation of 40W 8/20μs Waveform
- Quad Flat No Lead package QFN (1.2x1.5 sq mm, Height: 0.75mm)
- Lead Free Package 100% Tin Plating, Matte finish

APPLICATIONS

- USB2.0 and IEEE 1394 Firewire Ports
- RF Power Amplifier Protection
- RF/Antenna Circuits



MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20μs Waveform)	P _{PP}	40	W
Peak Pulse Current (8/20μs Waveform)	I _{PPM}	3	A
ESD Voltage (HBM Per MIL STD883C - Method 3015-6)	V _{ESD}	25	kV
Operating Temperature Range	T _J	-55 to +150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

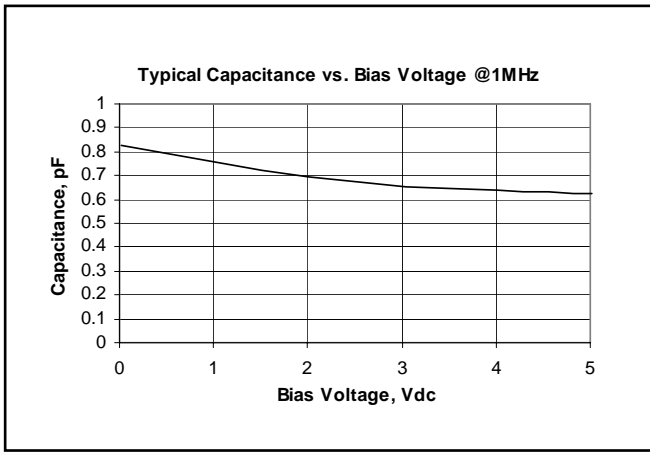
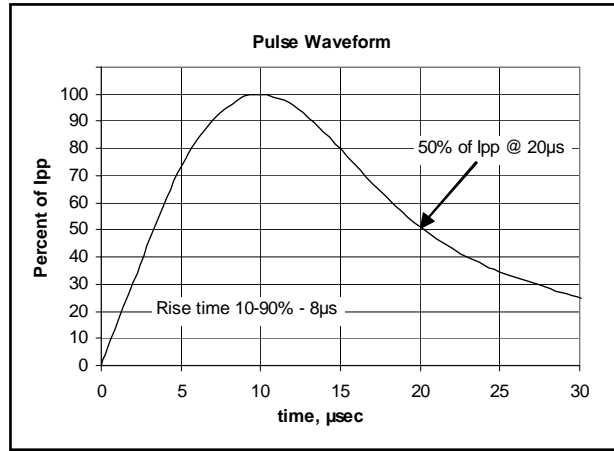
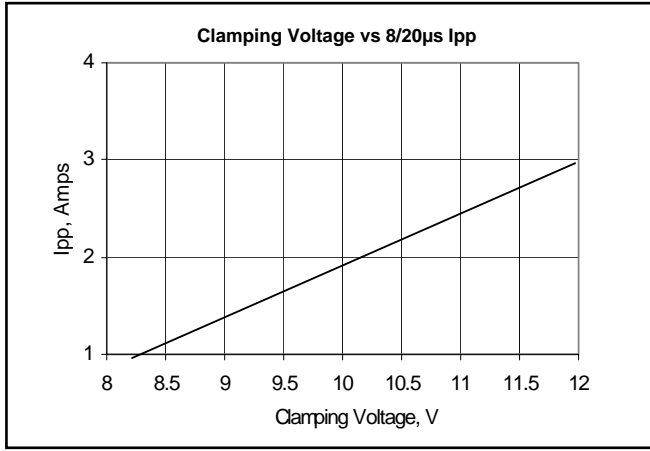
ELECTRICAL CHARACTERISTICS (Per Device) T_j = 25°C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V _{WRM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 1mA	6			V
Reverse Leakage Current	I _R	V _R = 5V			1	μA
Clamping Voltage (8/20μs)	V _C	I _{pp} = 3A			12	V
Off State Junction Capacitance	C _j	0 Vdc Bias f = 1MHz between 4&2 or 6&2			1	pF



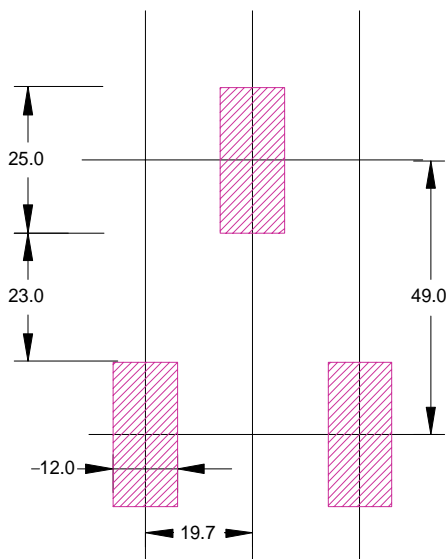
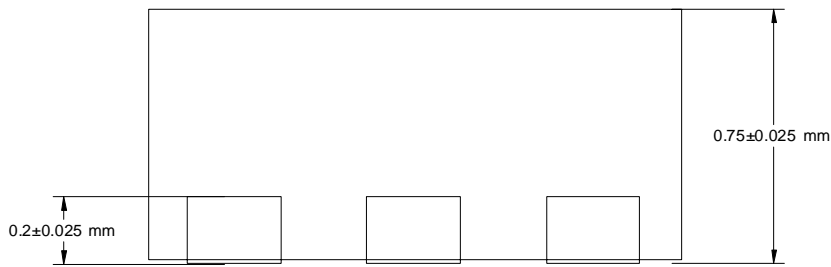
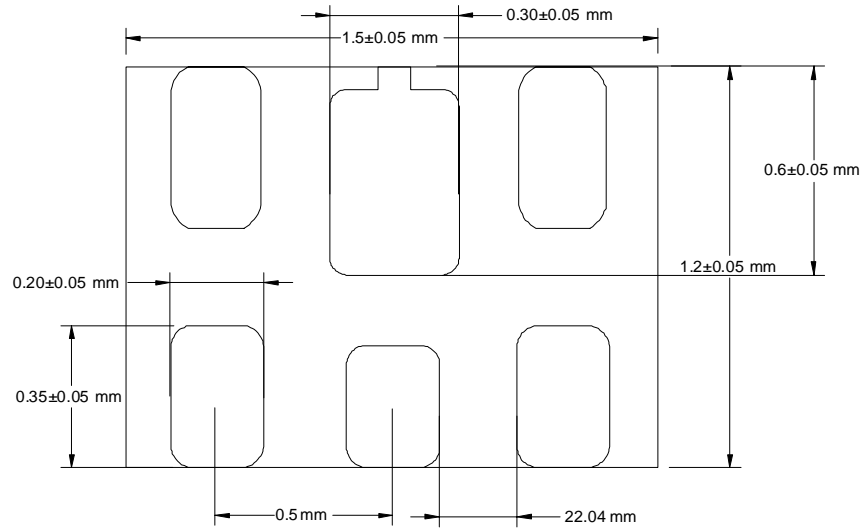
TYPICAL CHARACTERISTIC CURVES (Per Device) Tj = 25°C

PRELIMINARY

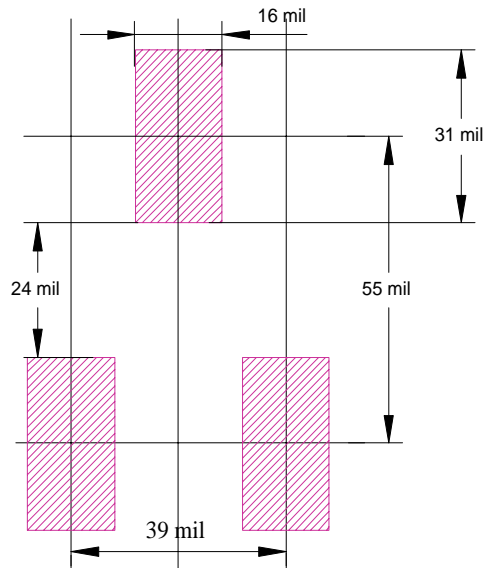


PACKAGE DIMENSIONS AND SUGGESTED PAD LAYOUT

PRELIMINARY



Suggested Pad Layout (in mils)



Alternate Pad Layout SOT523 (in mils)