King Billion Electronics Co., Ltd
駿 億 電 子 股 份 有 限 公 司

HF88M32B

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1. General Description

The HF88M32B is a command interfaced 4M x 8 bit Mask ROM. It features command mode interface with external CPU or MCU. In other words, it uses only 8-bit data bus and a few additional control pins to load addresses and provide the ROM access as well as extension I/O ports capability. This design not only reduces pin count required to access data in ROM dramatically but also allows for systems extension to higher capacity memories while using the existing board design. The application areas include voice, graphic, data storage in consumer products.

2. Features

✓ Data File Mode with only 11 pin interface

✓ Sixteen-bit Extension I/O pins with three-state mode

✓ Voltage range: 2.4 ~ 3.6V

✓ Organization

- Memory Cell Array: 4M x 8

✓ Sequential Read Operation in Data File Operation Mode

- Sequential Access : 100 ns (min.) at V_{DD} = 3.3V

✓ Command/Address/Data Multiplexed I/O port

✓ Low Operation Current (Typical)

- 10 μA standby mode current.

- 30 mA active read current at 100 ns cycle time.

✓ Package: bare chip

3. Functional block diagram
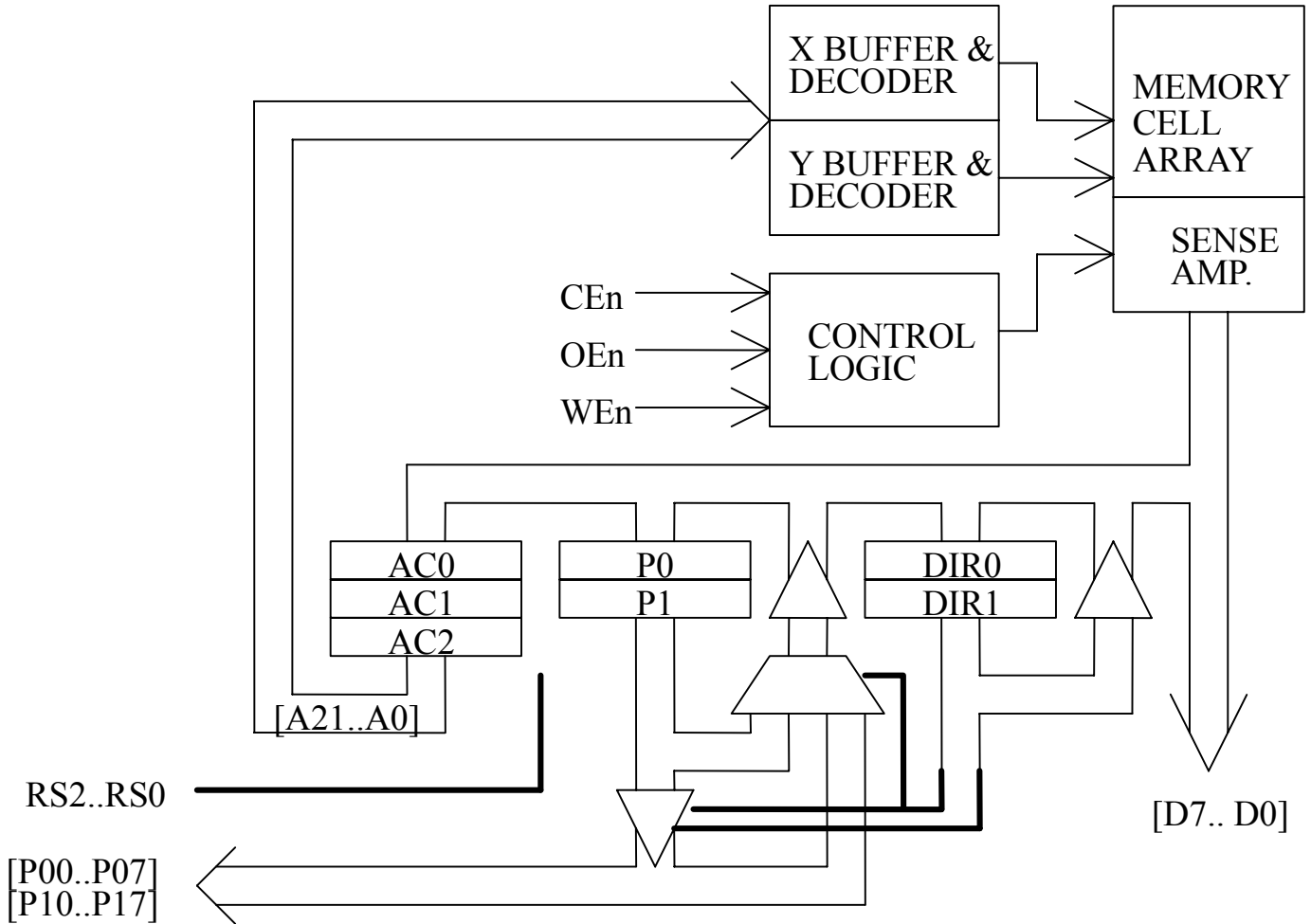
4. Pin Description

1	RS2	NC	43
2	RS1	WE	42
3	P07	P10	41
4	P06	P11	40
5	P05	P12	39
6	P04	P13	38
7	P03	P14	37
8	P02	P15	36
9	P01	P16	35
10	P00	P17	34
11	CE	RS0	33
12	GND	NC	32
13	OE	GND	31
14	D0	NC	30
15	NC	D7	29
16	D1	NC	28
17	NC	D6	27
18	D2	NC	26
19	NC	D5	25
20	D3	NC	24
21	NC	D4	23
		VCC	22

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Symbol	Pin No.	I/O	Description
RS0~RS2	33, 2, 1	I	Register Select pins RS2 ~ RS0 for accessing ROM data, Address Counter, as well as extension I/O ports.
P07 ~ P00	3 ~ 10	I/O	Bi-directional I/O port P0.
CEn	11	I	The CEn (Chip Enable) input is the device selection and power control for internal Mask ROM array. Whenever CEn goes high, the internal Mask ROM will enter standby (power saving) mode and accesses to internal registers are inhibited. Otherwise, it is in active mode and the contents of the ROM and registers can be accessed. Please note that only accesses to the internal registers are inhibited, but the status of I/O registers are not affected by the CEn pin and will remain unchanged. CEn is also useful to uniquely select a certain device for applications where multiple-chip array is required.
GND	12, 31	P	Negative power supply input pin.
OEn	13	I	OEn (Output Enable) is the output control which gates ROM array data, extension I/O ports, Direction Registers to the data I/O pins D7 ~ D0. The internal Address Counter will automatically increment by one with each rising edge of OEn pin in Sequentially Read mode.
VCC	22	P	Postive power supply input pin.
D7 ~ D0	14, 16, 18, 20, 23, 25, 27, 29	I/O	The Bi-directional Data I/O pins are used to set starting addresses, set the Extension I/O Direction and Output Registers, and to output ROM array data during read operations, contents of I/O Registers and status of input pins. The D7 ~ D7 float to high-impedance when the chip is deselected (CEn high) or when the outputs are disabled.
P17 ~ P10	34 ~ 41	I/O	Bi-directional I/O port P1.
WEn	42	I	WEn controls writing to internal registers such as the Output Port Registers, Direction Registers, Address Counter and Data on D7 ~ D0 are latched on the rising edge of the WE pulse.

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5. Pad Location

Left	Right
NC	GND
GND	GND
RS0	GND
P17	NC
P16	D7
P15	NC
P14	D6
P13	NC
P12	D5
P11	NC
P10	D4
WEN	GND
GND	
NC	VDD
	GND
GND	VDD
NC	GND
GND	VDD
NC	NC
RS2	D3
RS1	NC
P07	D2
P06	NC
P05	D1
P04	NC
P03	D0
P02	OEN
P01	GND
P00	GND
CEN	GND
NC	

LOGO

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Die Size: X= 40130 μm, Y=7138 μm, and substrate is connected to GND.

Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
1	NC	-1941.5	3231.86	31	GND	1941.5	-3262.78
2	GND	-1941.5	3008.86	32	GND	1941.5	-3039.78
3	RS0	-1941.5	2785.86	33	GND	1941.5	-2816.78
4	P17	-1941.5	2562.86	34	OEN	1941.5	-2593.78
5	P16	-1941.5	2339.86	35	D0	1941.5	-2370.78
6	P15	-1941.5	2116.86	36	NC	1941.5	-2140.78
7	P14	-1941.5	1893.86	37	D1	1941.5	-1917.78
8	P13	-1941.5	1670.86	38	NC	1941.5	-1687.78
9	P12	-1941.5	1447.86	39	D2	1941.5	-1464.78
10	P11	-1941.5	1224.86	40	NC	1941.5	-1234.78
11	P10	-1941.5	1001.86	41	D3	1941.5	-1011.78
12	WEN	-1941.5	778.86	42	NC	1941.5	-781.78
13	GND	-1941.5	555.86	43	VDD	1941.5	-558.78
14	NC	-1941.5	332.86	44	GND	1941.5	-335.78
15	GND	-1941.5	-34.78	45	VDD	1941.5	-112.78
16	NC	-1941.5	-257.78	46	GND	1941.5	110.22
17	GND	-1941.5	-480.78	47	VDD	1941.5	333.22
18	NC	-1941.5	-703.78	48	GND	1941.5	712.16
19	RS2	-1941.5	-926.78	49	D4	1941.5	935.16
20	RS1	-1941.5	-1149.78	50	NC	1941.5	1165.16
21	P07	-1941.5	-1372.78	51	D5	1941.5	1388.16
22	P06	-1941.5	-1595.78	52	NC	1941.5	1618.16
23	P05	-1941.5	-1818.78	53	D6	1941.5	1841.16
24	P04	-1941.5	-2041.78	54	NC	1941.5	2071.16
25	P03	-1941.5	-2264.78	55	D7	1941.5	2294.16
26	P02	-1941.5	-2487.78	56	NC	1941.5	2517.16
27	P01	-1941.5	-2710.78	57	GND	1941.5	2740.16
28	P00	-1941.5	-2931.48	58	GND	1941.5	2963.16
29	CEN	-1941.5	-3152.18	59	GND	1941.5	3186.16
30	NC	-1941.5	-3372.88				

NC: No Connection

6. Device Operation

The device provides the capability of accessing the contents of ROM array by external MCU not through standard address and data bus configuration but through minimal number of 8-bit data bus and control pins. Only 11 pins D7 ~ D0, CEn, OEn, WEn are required to use the device as a Data File device. By fixing the RS2 pin to '0', only CEn, WEn, OEn and D0 ~ D7 are required to access the ROM array data.

The CEn pin is device selection pin to uniquely select one device when more than one device are used in parallel and control the access to Mask ROM contents and internal registers. Whenever CEn goes high, the internal Mask ROM will enter standby (power saving) mode and accesses to internal registers are inhibited. Otherwise, it is in active mode. Therefore, when accessing contents of ROM is not intended, the

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CEn pin should be held at '1' to conserve the power consumption.

In addition to Data File mode, the device also provides the extension I/O capability. Two I/O ports (P0, P1) and total 16 pins are provided. The I/O ports can be configured to function as output pin or high-impedance input pins. Only 14 pins, CEn, WEn, OEn, RS2, RS1, RS0 and D0 ~ D7 are required to provide the Data File function and full access to two I/O ports.

There are seven internal registers used to provide the functionality of Data file access as well as Extension I/O capability. These registers are selected by RS2 ~ RS0. All registers are 8-bit wide except AC2. AC2 ~ AC0 are write-only and constitute the complete 22-bit address counter used as pointer to the accessed data. While the I/O ports P0, P1, DIR0 and DIR1 can be read as well as written. Their initial values are as indicated in the following table. When RS2 = '0', the RS1 ~ RS0 are ignored, the address counter can be loaded or contents of Data File can be read. This is to reduce the required pin needed for external MCU to interface with the device and also simplify the procedure for loading the address counter.

The P0, P1, DIR0, and DIR1 are used for extension I/O registers. The P0 and P1 are output registers of extension I/O and DIR0 and DIR1 are the direction registers that determine the I/O mode of P0 and P1. Each pin can be configured as output or input mode individually by setting or resetting the corresponding pin of the DIR registers. Initially, both P0 and P1 are default to input mode at 'Hi' state.

The accesses to the internal registers will be inhibited when CEn is '1'. However, the status of internal registers, such as extension I/O ports, will not be affected. For example, if a certain pin is in output mode and driving 'Hi', it will not change when CEn pin goes to '1' state. Therefore, the users are advised to take care of the power down condition of I/O ports when entering sleep mode to prevent unnecessary power drain.

RS[2:0]	Symbol	Type	Description	Initial Value
0xx		R	Read data by Indirect access	
	AC2	W	Address latch 2 for A21 ~ A16	"--------"
	AC1	W	Address latch 1 for A15 ~ A8	"--------"
	AC0	W	Address latch 0 for A7 ~ A0	"--------"
100	P0	R/W	Port 0 Output Register	"11111111"
101	DIR0	R/W	Direction Register of Port0	"00000000"
110	P1	R/W	Port 1 Output Register	"11111111"
111	DIR1	R/W	Direction Register of Port1	"00000000"

The writing sequence of address counters are AC0 first, AC1 second and AC2 last, once the OEn pin is active to low, and writing pointer of address counter (AC) will be reset to AC0 and always stay at AC0 until the RS2 is set to "0" and WEn pin has a low to high toggle to increase the writing pointer of address counter (AC).

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6.1. Retrieve data in Data File

Accesses to the ROM contents, extension I/O, address counter and direction registers are made through D[7:0] data pins. With register selection pins RS[2:0] set to "0xx", the starting addresses can be written into the address counter through D[7:0] data pins by bringing WEn to low and back to high. The D[7:0] data are latched into the address counter on the rising edge of WEn.

Once the starting address of data block is latched into the address counter AC2~0, data can be read out by sequentially pulsing OEn with CEn held low. When CEn is held at '0', the OEn gate the data of the selected address unto Data I/O pin D[7:0]. With the rising edge of OEn, the internal address counter is increased by one automatically.

6.2. Loading the Address Counter

Before the data can be retrieved, the address counter (AC) must be initialized with the starting address, then the contents of ROM pointed to by address counter can be accessed through D[7:0]. In order to simplify the procedure of loading 22-bit address counter (AC), a internal pointer is implemented and used to point to next register to write in the up to three-cycle address loading sequence. Initially, with RS = "0xx" CEn goes from '1' to '0' and the AC pointer is initialized. The pointer is then incremented to point to next register with falling edge of each WEn pulse. So when randomly accessing data within a 256-byte page, or within a 64K-byte block mode, then only one or two-cycle address reload process is needed to access different locations within a page or block.

The Address Counter pointer will be held in reset state in the following conditions:

1. When CEn is '1' (the device is deselected).
2. By the Read pulse (OEn is '0') and RS2 = '0' (ROM is being accesses).

The inclusion of the 3rd condition is to force the address loading to start from LSB of Address Counter once the read cycle is initiated. However, the AC Pointer will not be reset when reading or writing from/to extension I/O registers (P0, P1, DIR0, DIR1). This design is useful in certain application scenarios where in the midst of the multi-byte address loading process, an interrupt to the MCU main loop occurs. And in the interrupt service routine, manipulation of extension I/O registers is performed, i.e., key board is scanned using P0 and P1. When the execution of program returns to main loop after interrupt service routine completed, the loading of address can still resume from where it was interrupted.

6.3. Sequential Read Mode and Auto Increment of Address Counter

With each read access to the ROM data (RS = "0xx"), the Address Counter is incremented automatically by one with rising edge of OEn to facility sequential access to a block of ROM data and avoid repeated loading of addresses.

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6.4. Output data to External I/O

The device's 16-bit Extension I/O capability provides additional I/O ports for applications where the I/O pins are heavily used. To use as a certain pin as output pin, the corresponding bit in Direction Register must be set to '1'. Please refer to the following example where output 0x00 to P0 to '0' is intended.

1. Set RS to "101" (DIR0).
2. Keep D7 ~ D0 at 0xff (all bits in output mode).
3. Pulse the WEn to low then high to write to write contents of D-bus to DIR0.
4. Set RS to "100" (P0 Output Register).
5. Set D7 ~ D0 to 0x00.
6. Pulse the WEn to low then high to write contents of D-bus to P0 and drive all bits in P0 to low.

6.5. Reading Input pin status

To use extension I/O ports as input pins and read the status from them, the corresponding bit in direction register must be set to '0'. Please see the following example where reading inputs from of P1 is intended.

1. Set RS to "111" (DIR1).
2. Set D7 ~ D0 to 0x00h.
3. Pulse the WEn to low then high to set DIR1 to all High-Impedance input modes.
4. Set RS to "110" (P1 Output Register).
5. Pulse the OEn to low.
6. Read P1 then set the OEn back to high.

There is one thing should be noted. For any unused (open) extension I/O pin, it is advisable to set the port to output mode either at '0' or '1' state to prevent it from floating or fix it at VCC or GND if it is set to input mode. Otherwise, the noise might cause the unnecessary power consumption.

6.6. Retrieving the Contents of Extension I/O registers

The contents of all four registers can be read through data bus. The ability to access the contents of registers avoids the necessity of using the RAM as mirror to keep the current status of latches in applications. However, extra care should be taken when reading P0 and P1. To read the contents of P0 and P1, the DIR0 and DIR1 should be set to output mode. Otherwise, the pin status instead of P0 and P1 will be read. The same precaution should be applied in Read-Modify-Write sequence that read back the contents of the output latch of output mode pins and input status of input mode pins.
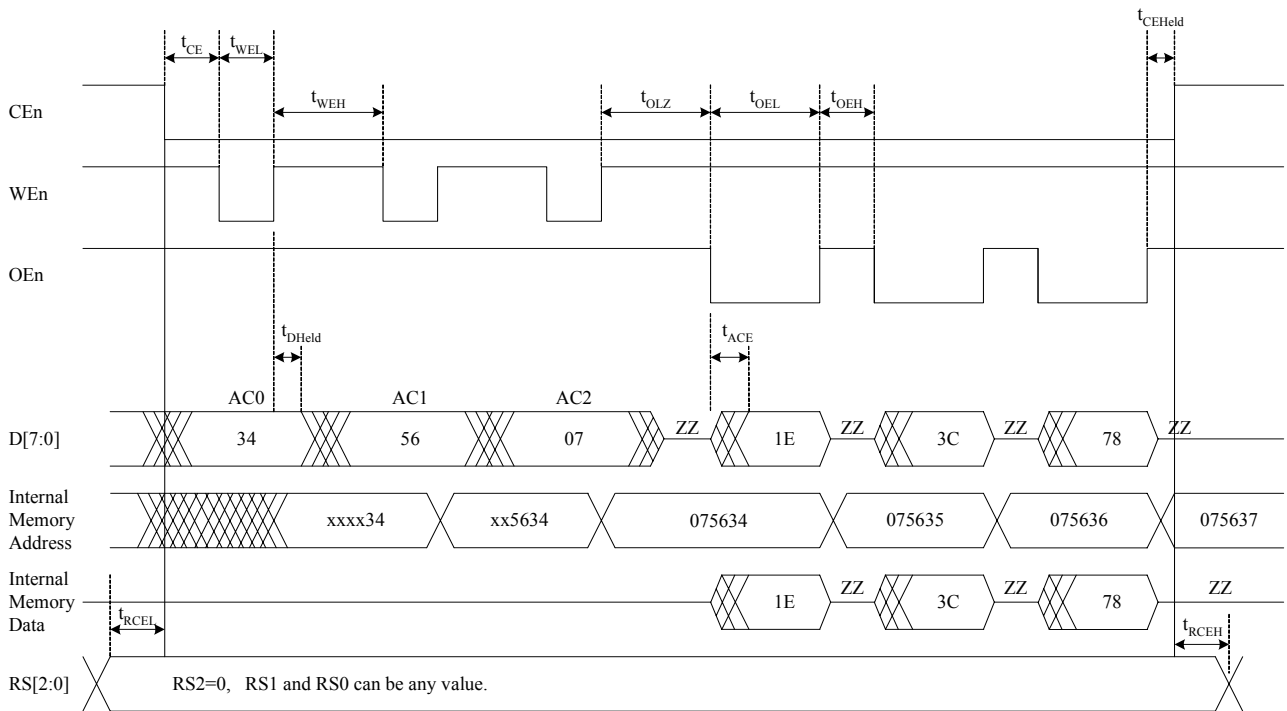
7. Timing Diagrams

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{CE}	Chip selected to active width	0	50	-	ns

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T_{WEL}	WEn active low width	100	-	-	ns
T_{WEH}	WEn inactive low width	100	-	-	ns
T_{DHeld}	Written data hold time	50	-	-	ns
T_{OLZ}	Read-Write mode transient time	200	-	-	ns
T_{ACE}	ROM data file available time	50	-	-	ns
T_{OEL}	Output enable low duty for access ROM	250	-	-	ns
T_{OEH}	Output enable low duty for access ROM	150	-	-	ns
T_{CEHeld}	Chip selection signal holding time	50	-	-	ns
T_{ACER}	Register data available time	30	-	-	ns
T_{ORL}	Output enable low duty for access register	100	-	-	ns
T_{ORH}	Output enable low duty for access register	100	-	-	ns
T_{RCEL}	RS signal setup time	50	-	-	ns
T_{RCEH}	RS signal hold time	50	-	-	ns

7.1. Data File Read Cycle

Data File Read Cycle

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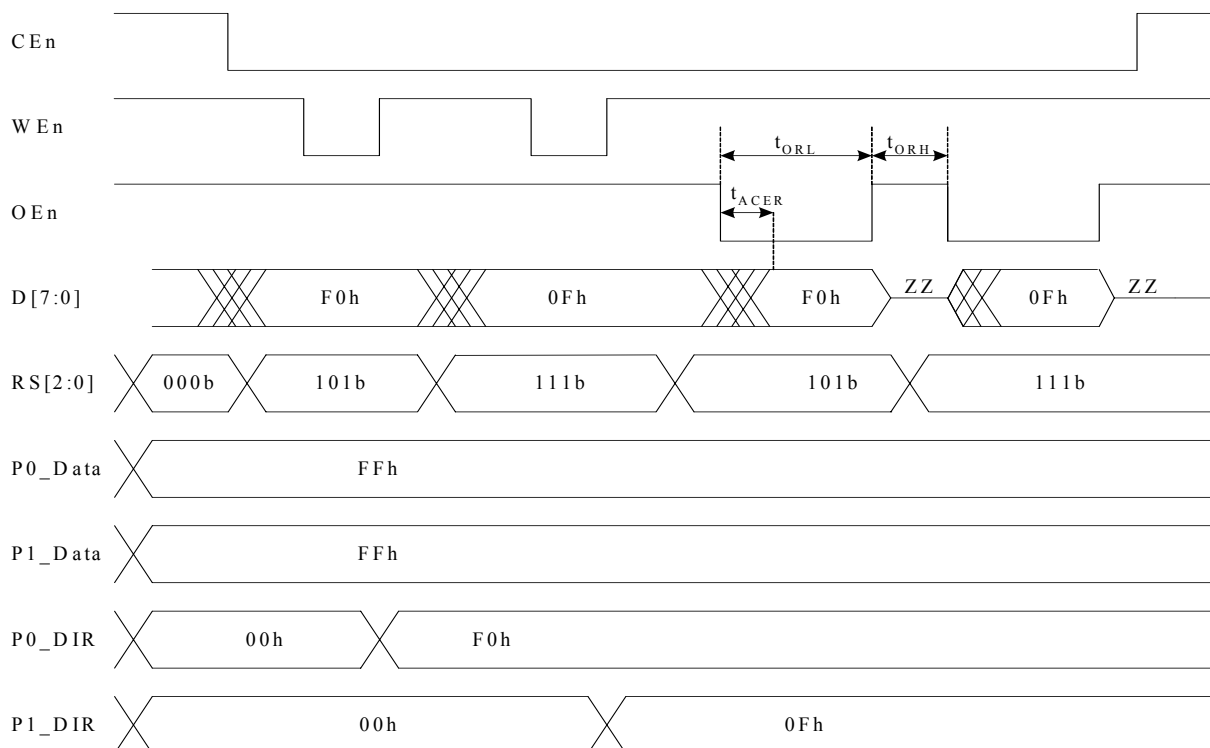
7.2. Interrupted by I/O when Loading Address Counter
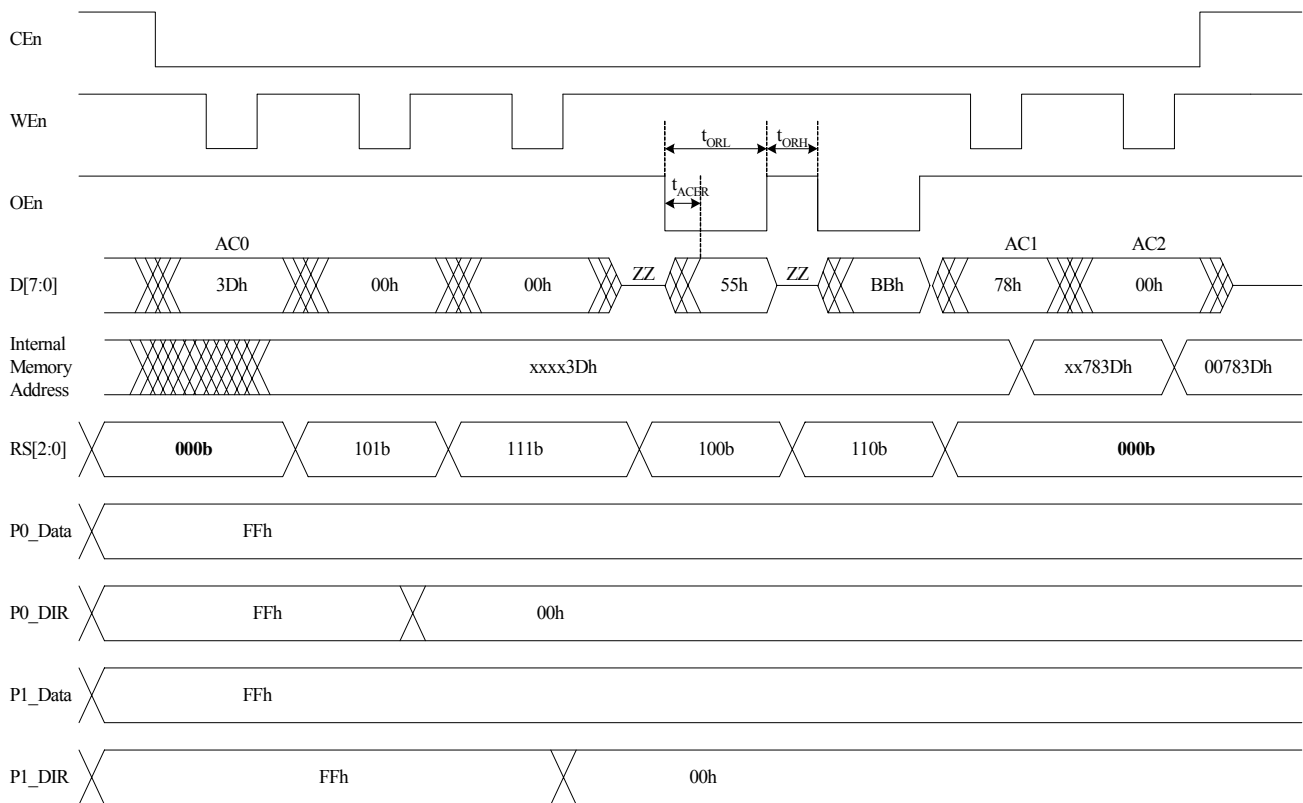
Interrupted by I/O when Loading Address Counter

7.3. Setting and Reading the I/O Mode for P0 and P1

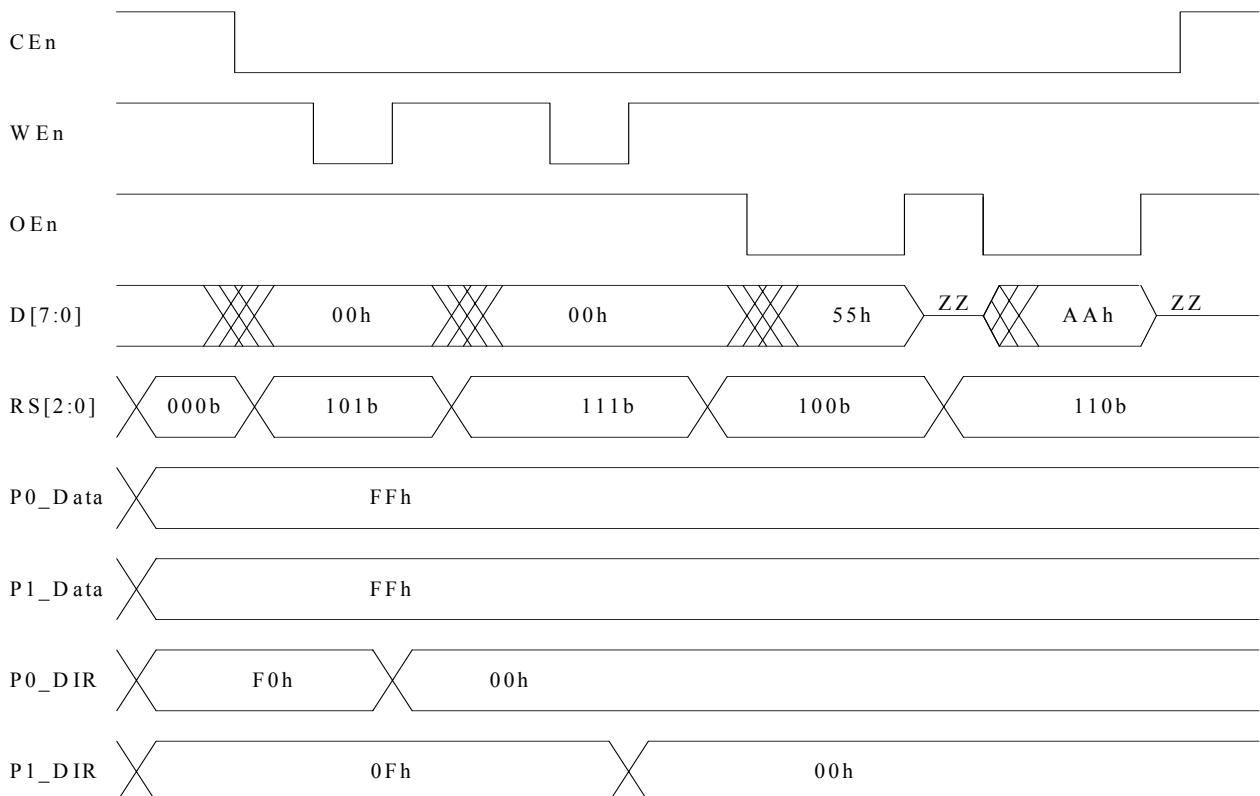Setting and Reading the I/O Mode for P0 and P1

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7.4. Reading P0 and P1 in Mixed-I/O Mode
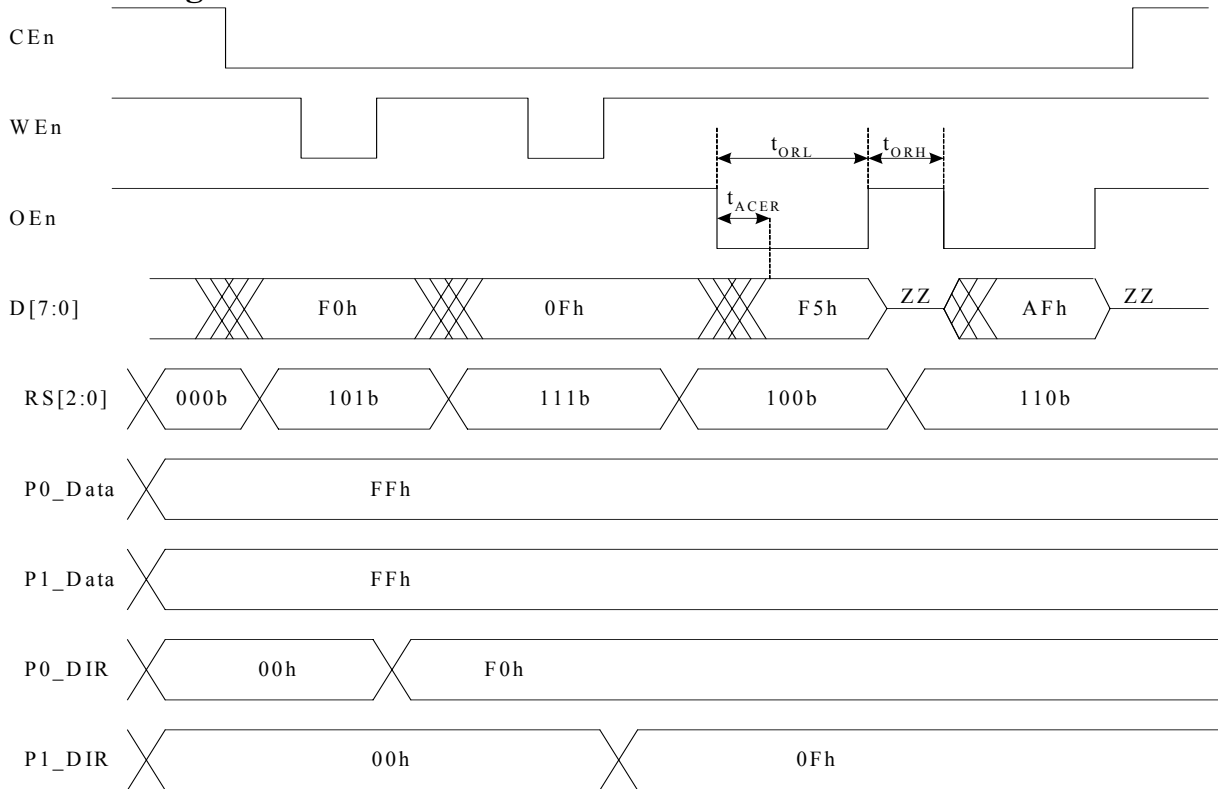
Reading P0 and P1 in Mixed-I/O Mode

7.5. Reading the input pins

Reading the Input Pins

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7.6. Output to P0 and P1 Ports
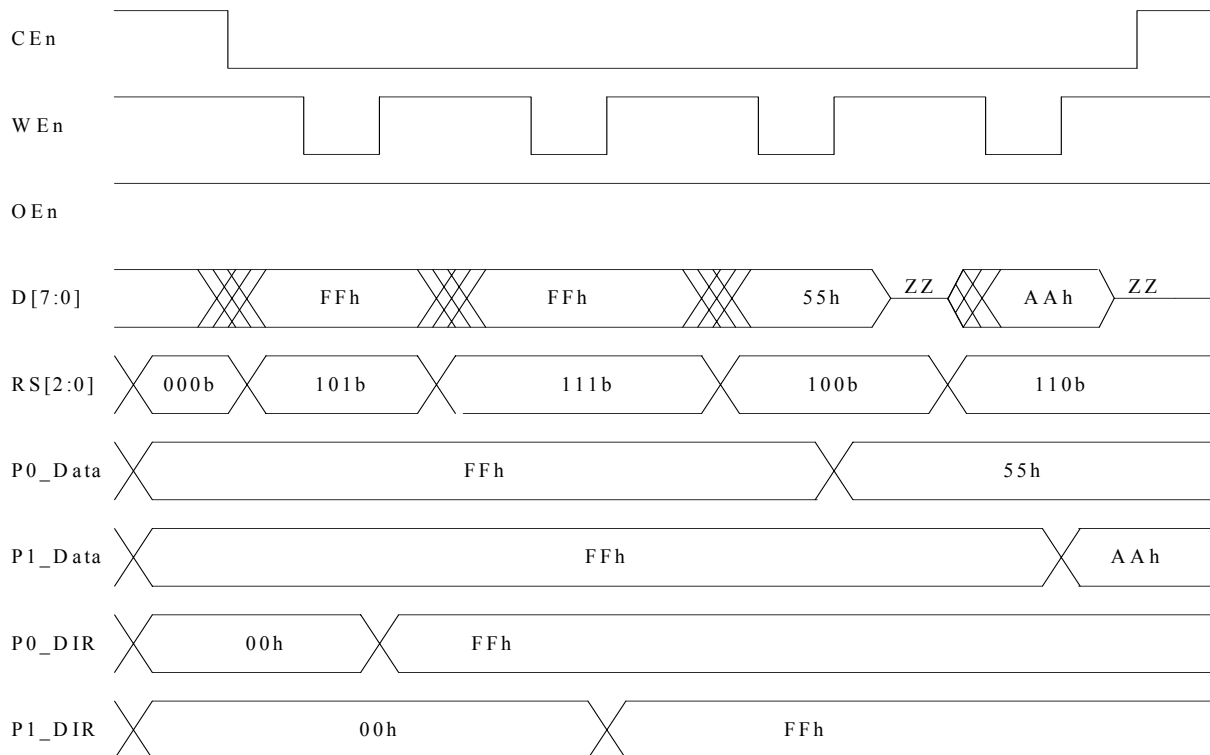
Output to P0 and P1 Ports

8. Absolute Maximum Rating

Items	Symbol	Rating
Supply Voltage	V_{CC}	2.4 ~ 3.6 V
Input Voltage	V_{IN}	-0.3 to Vdd+0.3 V
Operating Temperature	T_{OPR}	-0 to 70 °C
Storage Temperature	T_{STR}	-55 to 125 °C

9. AC/DC Electrical Characteristics

(GND = 0V, V_{CC} = 3.0V, T_{OPR} = 25°C unless otherwise noted)

Parameter	Symbol	Min.	Typical	Max.	Unit	Condition
Supply Voltage	V_{CC}	2.4	-	3.6	V	
Operating Current	I_{CC}	-	30	-	mA	No load, t_{RC}@ 100 ns
Standby Current	I_{STBY}	-	10	-	μA	No load
Input voltage	V_{IH}	2/3	-	1	V_{CC}	V_{CC} = 2.4V ~ 3.6V
	V_{IL}	0	-	1/3		
Input current leakage	I_{IL}	-	-	± 10	μA	
P0, P1 Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 0.3 mA
P0, P1 Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
D Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 1.4 mA
D Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3 mA

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10. Application Circuit Diagram

This application circuit illustrates that how KB83760 MCU uses two external HF88M32Bs for ROM extension as well as keyboard scan functions.

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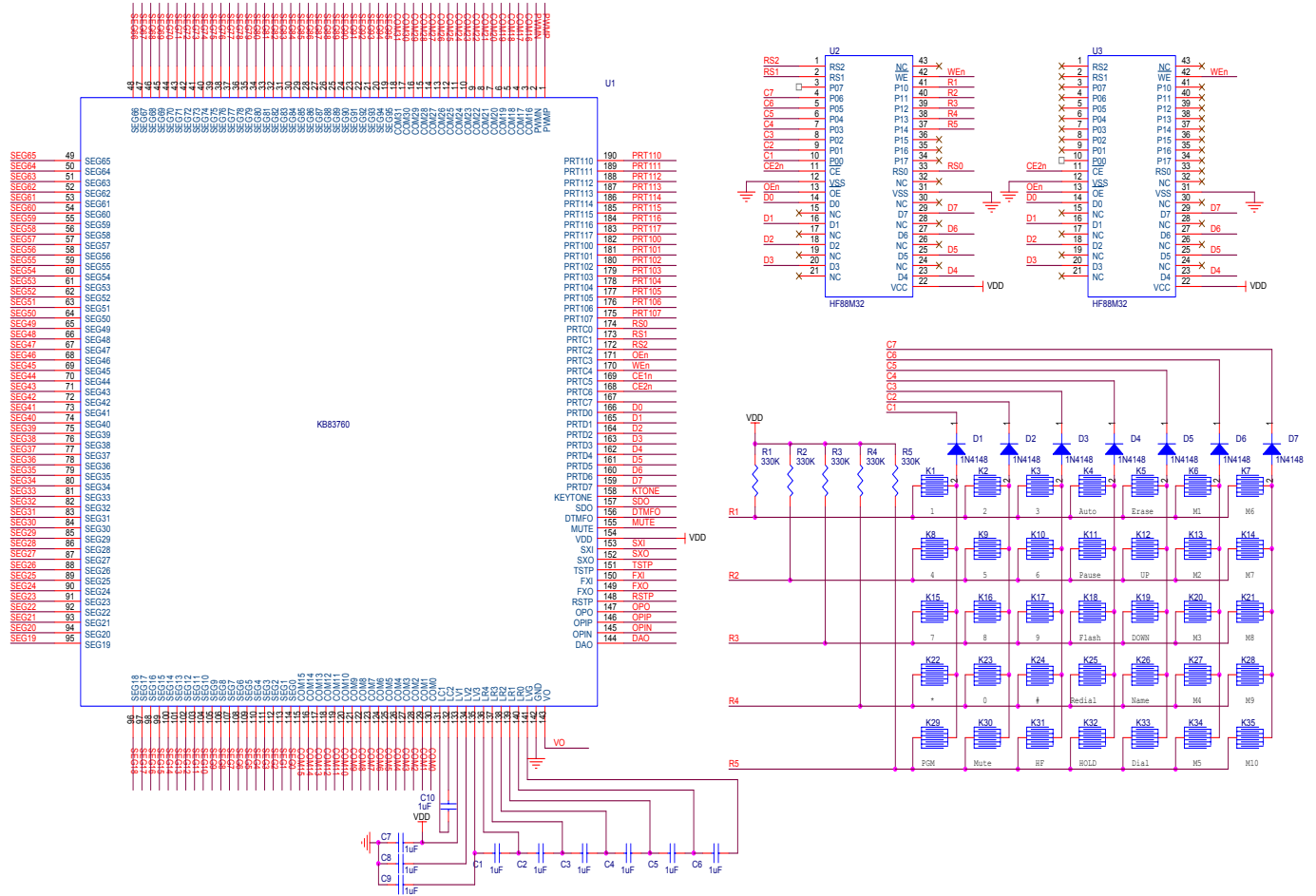
11. Updated History

Version	Date	Update Description
1.10	2003/8/27	Timing diagrams modified.
1.11	2004/1/16	Add the die size.

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