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1. General Description

HE89C21 is a member of 8-bit Micro-controller series developed by King Billion Electronics for telecom applications. This chip has 4-COM x 32-SEG LCD driver with built-in regulator to provide stable visual effect over the battery life, 16-bit general purpose I/O port, DTMF generator for the dialing tone generation. It is suitable for application in feature telephone products.
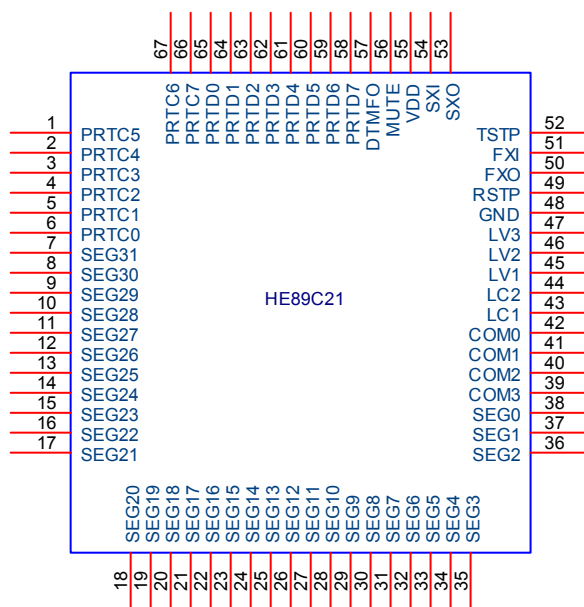
The instruction set of HE80000 are easy to learn and simple to use. Thirty-two instructions with four-type

addressing mode are provided. Most of instructions take only 3 oscillator clocks to execute.

2. Features

- ✓ Operation Voltage: 2.4V ~ 5.5V
- ✓ Internal ROM: 16 KB Program ROM
- ✓ Internal RAM: 512 Bytes.
- ✓ Dual Clock System: Fast clock: 32768 ~ 8M Hz
                                 Slow clock: 32768 Hz
- ✓ Operation Mode: Fast, Slow, Idle, Sleep Mode.
- ✓ 16 bit Bi-directional general purpose I/O port with output type (push-pull or open drain) selectable for each I/O pin by mask option.
- ✓ 4 COM x 32 SEG LCD driver (A, B type waveform selectable).
- ✓ Built-in Regulator for providing LCD with a stable operation voltage over the battery life.
- ✓ Built-in DTMF Generator.
- ✓ Built-in Low Voltage Reset function
- ✓ Two external interrupts and three internal timer interrupts.
- ✓ Two 16-bit timers and one Time Base timer.
- ✓ Watch Dog Timer to prevent deadlock condition.
- ✓ Instruction set: 32 instructions with 4 addressing modes.

3. Pin Description

Pin Name	Pin #	I/O	Description
PRTC[7..0]	66,67,1~6	B	8-bit bi-directional general purpose I/O port C. The output type of I/O pad can also be selected by mask option MO_CPP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin.
SEG[31..0]	7 ~ 38	O	LCD SEGMENT SEG[31..0] outputs.
COM[3..0]	39 ~ 42	O	LCD COMMON COM[3..0[outputs.
LC1	43	B	Charge Pump Capacitor Pin
LC2	44	B	Charge Pump Capacitor Pin

Pin Name	Pin #	I/O	Description
LV1	45	B	LCD Charge Pump Voltage V1
LV2	46	B	LCD Charge Pump Voltage V2
LV3	47	B	LCD Charge Pump Voltage V3
GND	48	P	Power ground Input.
RSTP_N	49	I	System Reset input pin. Level trigger, active low on this pin will put the chip in reset state.
FXO, FXI	50, 51	O, B	External fast clock pin. Two types of oscillator can be selected by MO_FXTAL ('0' for RC type and '1' for crystal type). For RC type oscillator, one resistor need to be connected between FXI and GND. For crystal oscillator, one crystal need to be placed between FXI and FXO. Please refer to application for details.
TSTP_P	52	I	Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
SXO, SXI	53, 54	O, I	External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base, DTMF generator and other internal blocks. 32768 Hz crystal or resonator should be used for DTMF generator to function properly.
VDD	55	P	Positive power Input. 0.1 μF decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect.
MUTE	56	O	MUTE is open drain type output for muting microphone of telephone speech network.
DTMFO	57	O	Dual-Tone Multiple Frequency Tone Output for dialing purpose. It can also be used as two-channel general purpose tone generator with frequency resolution of 1 Hz.
PRTD[7..0]	58 ~ 65	B	8-bit bi-directional general purpose I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin. The initial state of PRTD[2..0] can be determined by mask option MO_IH[2..0], while initial state of PRTD[7..3] is always '1'. PRTD[7..2] can be used as wake-up pins. PRTD[7..6] can be used as external interrupt sources.

4. Pad Diagram
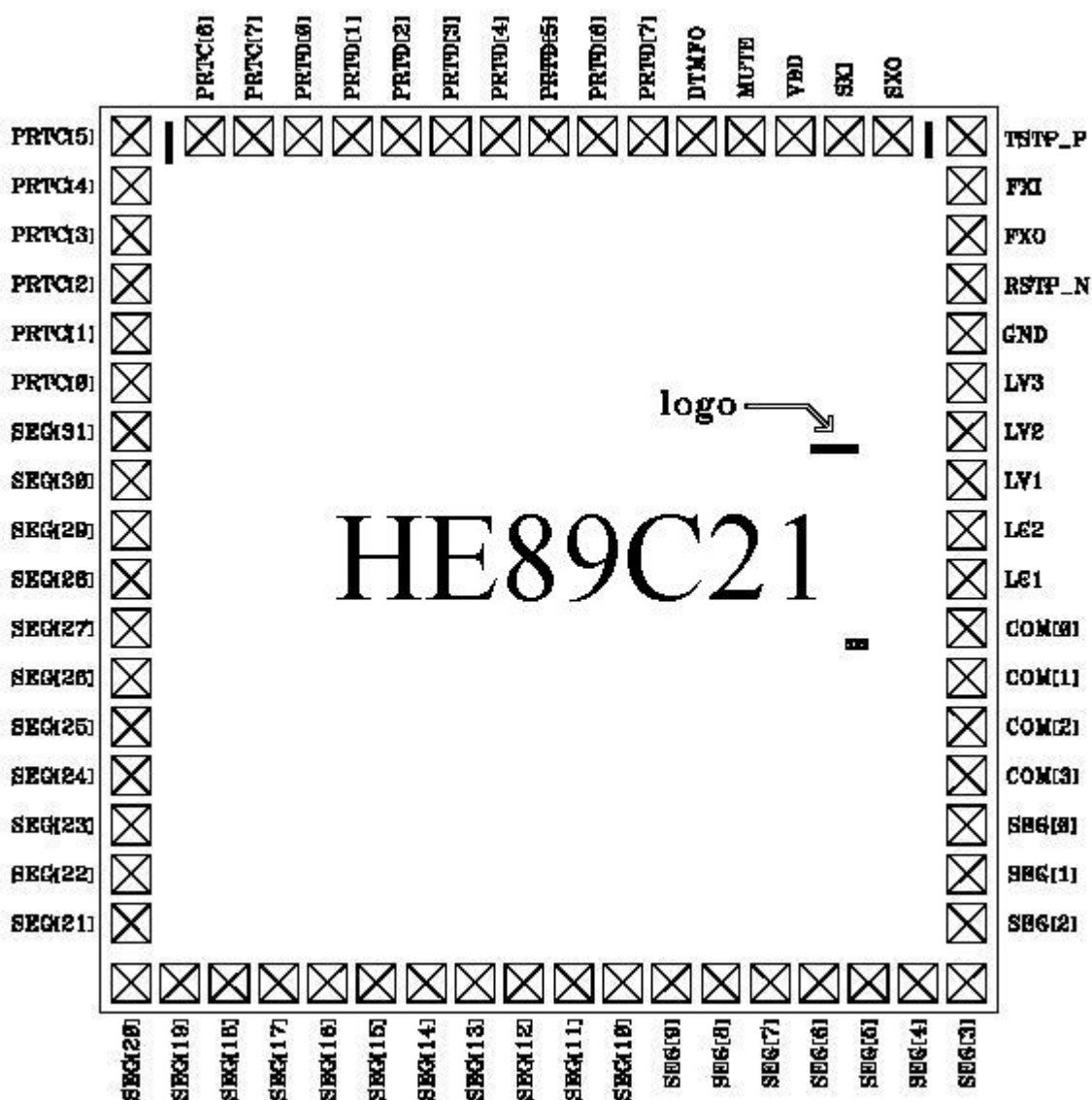
5. Pad Coordinations

Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
1	PRTC[5]	-977.5	989.5	35	SEG[3]	977.5	-989.5
2	PRTC[4]	-977.5	874.5	36	SEG[2]	977.5	-850.5
3	PRTC[3]	-977.5	759.5	37	SEG[1]	977.5	-735.5
4	PRTC[2]	-977.5	644.5	38	SEG[0]	977.5	-620.5
5	PRTC[1]	-977.5	529.5	39	COM[3]	977.5	-505.5
6	PRTC[0]	-977.5	414.5	40	COM[2]	977.5	-390.5
7	SEG[31]	-977.5	299.5	41	COM[1]	977.5	-275.5
8	SEG[30]	-977.5	184.5	42	COM[0]	977.5	-160.5
9	SEG[29]	-977.5	69.5	43	LC1	977.5	-45.5
10	SEG[28]	-977.5	-45.5	44	LC2	977.5	69.5

Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
11	SEG[27]	-977.5	-160.5	45	LV1	977.5	184.5
12	SEG[26]	-977.5	-275.5	46	LV2	977.5	299.5
13	SEG[25]	-977.5	-390.5	47	LV3	977.5	414.5
14	SEG[24]	-977.5	-505.5	48	GND	977.7	529.5
15	SEG[23]	-977.5	-620.5	49	RSTP_N	977.5	644.5
16	SEG[22]	-977.5	-735.5	50	FXO	977.5	759.5
17	SEG[21]	-977.5	-850.5	51	FXI	977.5	874.5
18	SEG[20]	-977.5	-989.5	52	TSTP_P	977.5	989.5
19	SEG[19]	-862.5	-989.5	53	SXO	805	989.5
20	SEG[18]	-747.5	-989.5	54	SXI	690	989.5
21	SEG[17]	-632.5	-989.5	55	VDD	575	989.5
22	SEG[16]	-517.5	-989.5	56	MUTE	460	989.5
23	SEG[15]	-402.5	-989.5	57	DTMFO	345	989.5
24	SEG[14]	-287.5	-989.5	58	PRTD[7]	230	989.5
25	SEG[13]	-172.5	-989.5	59	PRTD[6]	115	989.5
26	SEG[12]	-57.5	-989.5	60	PRTD[5]	0	989.5
27	SEG[11]	57.5	-989.5	61	PRTD[4]	-115	989.5
28	SEG[10]	172.5	-989.5	62	PRTD[3]	-230	989.5
29	SEG[9]	287.5	-989.5	63	PRTD[2]	-345	989.5
30	SEG[8]	402.5	-989.5	64	PRTD[1]	-460	989.5
31	SEG[7]	517.5	-989.5	65	PRTD[0]	-575	989.5
32	SEG[6]	632.5	-989.5	66	PRTC[7]	-690	989.5
33	SEG[5]	747.5	-989.5	67	PRTC[6]	-805	989.5
34	SEG[4]	862.5	-989.5				

6. LCD Power Supply

The LCD power supply is equipped with input power regulator, voltage Tripler, and bias voltage generating resistor network. The input power of MCU is regulated and multiplied by 3 times to generate LV3 to generate the stable driving voltages for LCD driver. The bias voltages for LCD driver are then generated from LV3 using the internally resistor voltage dividing network. With the regulated LCD power, the LCD display can give steady visual effect over a wide range of operating voltage. The built-in regulator must be enabled by mask option MO_ LVRG to function.
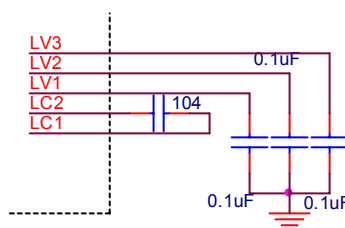
MO_LVRG	Function
0	Disable LCD regulator
1	Enable LCD regulator

6.1. LCDC Control register

LCD Control Register LCDC controls the functions of LCD driver; such as contrast level, LCD waveform type, On/Off, Blank or not, etc.

LCDC	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	-	-	-	-	-	TYPE	BLANK	LCDE

Field	Value	Function
TYPE	0	Select Type A LCD waveform
	1	Select Type B LCD waveform
BLANK	0	Normal display
	1	LCD display blanked. LCD driver changes only COM output signal, SEG signal remains unchanged.
LCDE	0	LCD driver disabled, LCD driver has no output signal.
	1	LCD driver Enabled

Please note that LCD driver must be turned off before the entering sleep mode. That means user must clear the bit 0 of LCDC to turn off LCD driving circuit before setting bit6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed.

Please also note that LCD driver uses slow clock as clock source. The LCD display will not display normally if it works in Fast clock only mode because the LCD refresh action is too fast.

7. LCD RAM Map

| PP=0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
	bit7(C3)	bit6(C2)	bit5(C1)	bit4(C0)	bit3(C3)	bit2(C2)	bit1(C1)	bit0(C0)
F0h	S1				S0			
F1h	S3				S2			
F2h	S5				S4			
F3h	S7				S6			
F4h	S9				S8			
F5h	S11				S10			
F6h	S13				S12			
F7h	S15				S14			
F8h	S17				S16			
F9h	S19				S18			
FAh	S21				S20			
FBh	S23				S22			
FCh	S25				S24			
FDh	S27				S26			
FEh	S29				S28			
FFh	S31				S30			

8. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. So that system designer can select oscillator types based on the cost target, timing accuracy requirements etc. With two clock sources available, the system can switch among operation modes of Fast, Slow, Idle, and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	1	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	-	-	0	-	-	-	-

Crystal, Resonator or RC oscillator can be used as fast clock source. External components should be placed as close to the oscillator pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.
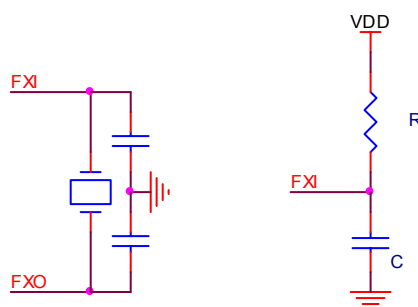
Slow clock is clock source for LCD display, Timer1, and Timer Base, etc. Crystal oscillator can be used as slow clock. If used in feature phone applications, 32768 Hz crystal is suggested to generate DTMF tone.
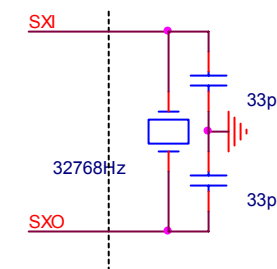
If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

9. General Purpose I/O

There are two dedicated general purpose I/O port, PRTC, PRTD. All the I/O Ports are bi-directional and of non- tri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option. The input port has built-in Schmidt trigger to prevent it from chattering. The hysteresis level of Schmidt trigger is 1/3*VDD.

| MO_?PP[...]	Output Structure
0	Open-drain output
1	Push-pull output

When the I/O port is used as input, the weakly high sourcing PMOS can be used as pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin, otherwise, the pin will always be stuck at '0'. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The initial state of most I/O ports is '1' with one exception. The initial state of PRTD[2..0] is determined by mask option MO_IH[2..0].

PRTD	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	1	1	1	1	1	MO_IH2	MO_IH1	MO_IH0

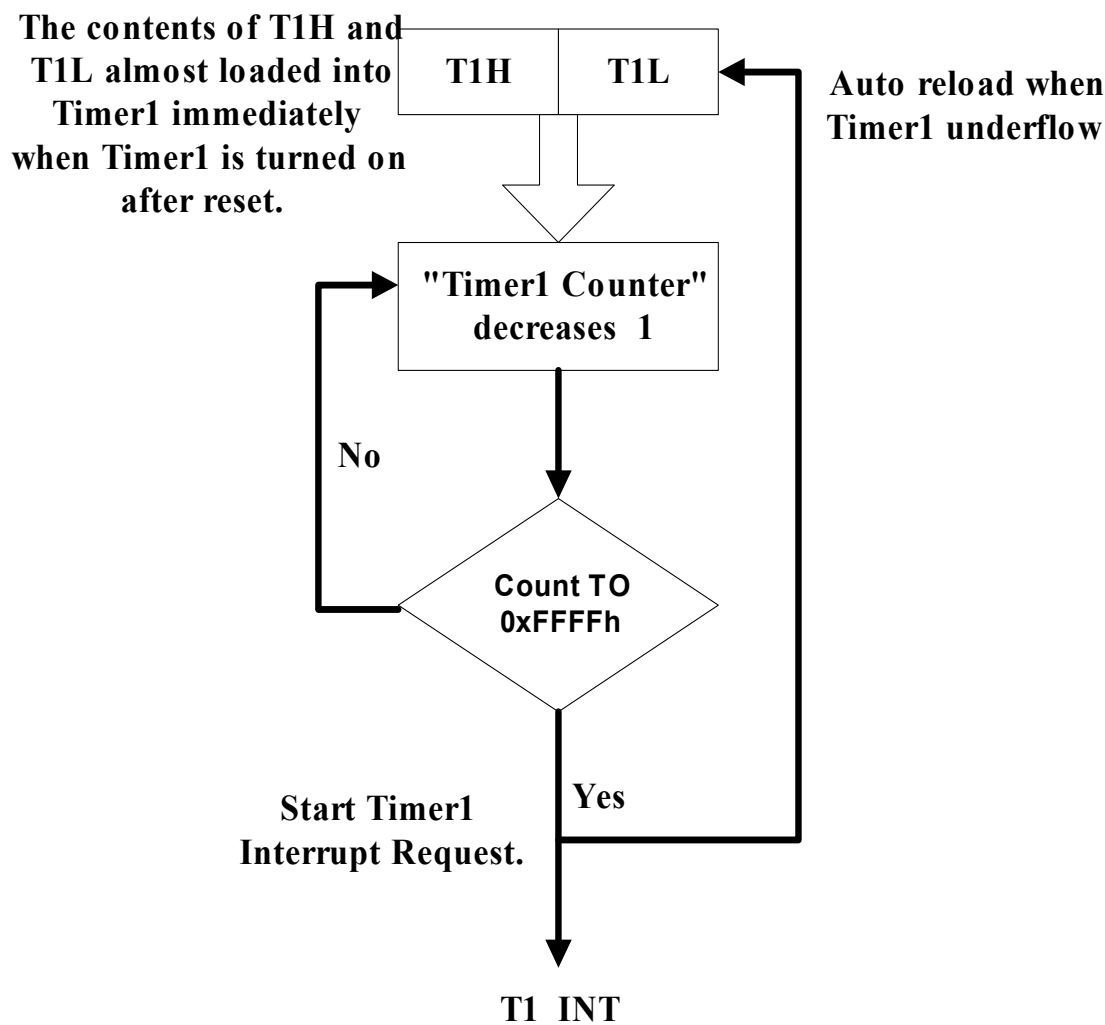| MO_IH[2..0]	Initial State of PRTD[2..0]
0	0
1	1

SCHMIDT Trigger input
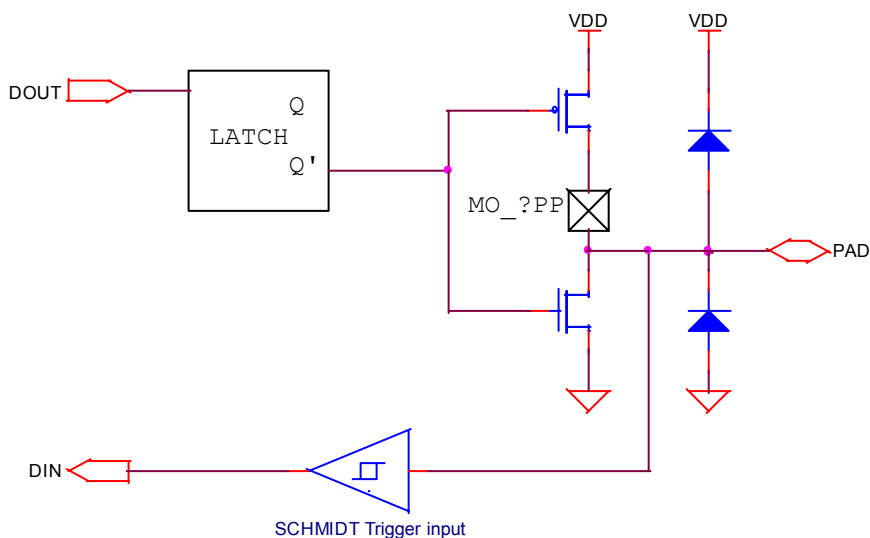
10. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock "SCK" at dual clock or slow clock only mode. And it comes from the fast clock "FCK" at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.

The contents of T1H and T1L almost loaded into Timer1 immediately when Timer1 is turned on after reset.

| T1H | T1L |

Auto reload when Timer1 underflow

"Timer1 Counter" decreases 1

No

Count TO 0xFFFFh

Start Timer1 Interrupt Request.

Yes

T1_INT

The Timer1 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

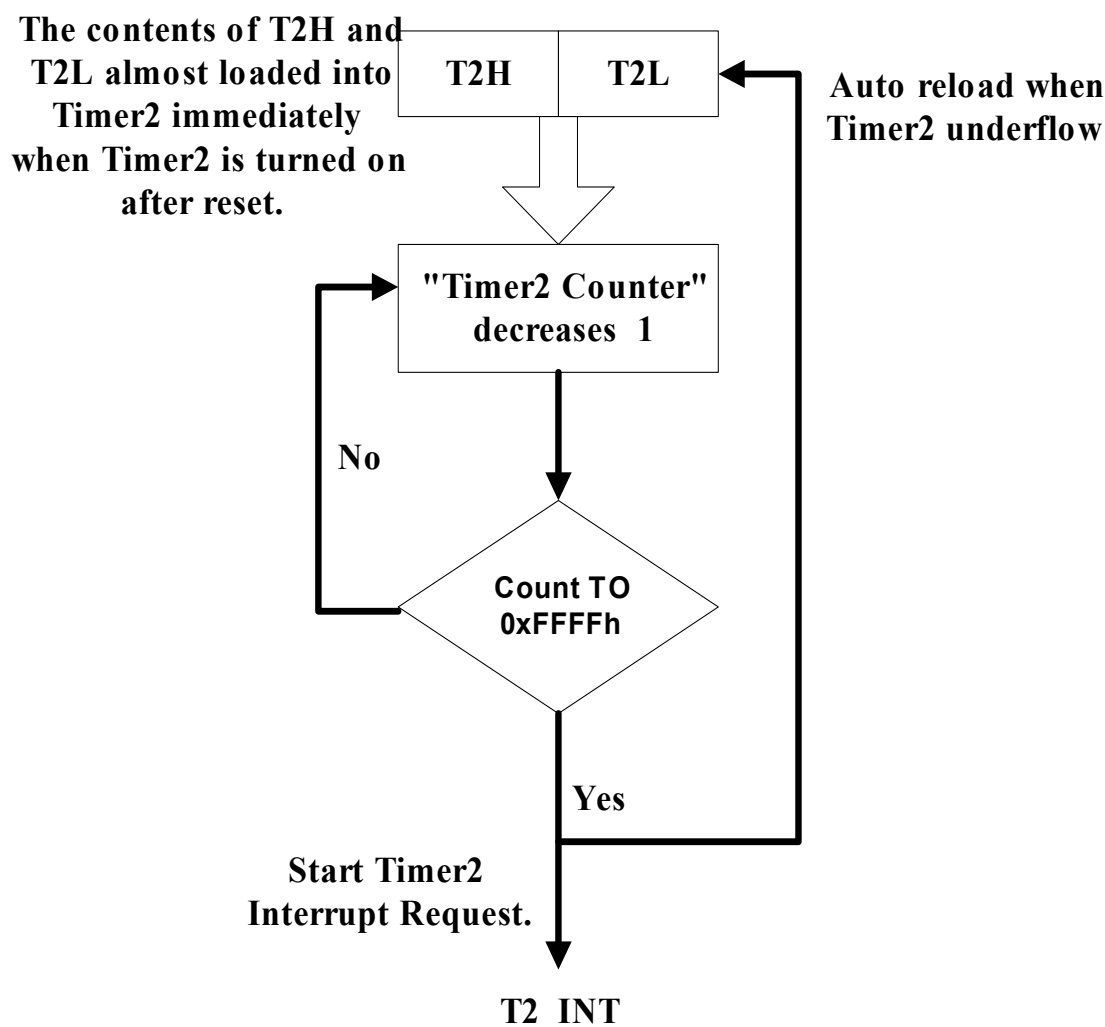# 11. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded

with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.

The contents of T2H and T2L almost loaded into Timer2 immediately when Timer2 is turned on after reset.

| T2H | T2L |

Auto reload when Timer2 underflow

"Timer2 Counter" decreases 1

No

Count TO 0xFFFFh

Yes

Start Timer2 Interrupt Request.

T2_INT

The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3..0]. TBE (Time Base Enable) bit

controls enable or disable of the circuit.

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	-	-	0	-	-	-	-

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

12.   Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically prevent system dead lock caused by abnormal hardware activities or program execution.   WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

To use WDT function, "CLRWDT" instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated.

WDT is the enabling signal generated by calculating 32768-clock overflow.   Reset Register content is same as TC1 (Timer1 clock), which uses the same clock count source.   WDT function can be generated in Normal, Slow and Idle Mode.   However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

13.   Low Voltage Reset

Low voltage reset circuit prevents the CPU from operating below its physical limit. When the supply voltage drops below V_{DET}, the CPU will be held in reset state until the supply voltage rises to V_{RLS}. Then CPU will be released from reset state. V_{RLS} will be higher than V_{DET} by 5% to provide hysteresis and prevent CPU from bouncing back and forth between reset and operating state.

MO_LVR_LVL	Detection voltage	Release voltage
00	1.9 volts	1.995 volts
01	2.0 volts	2.1 volts
10	2.1 volts	2.205 volts

The low voltage reset circuit can be disabled/enable by mask option MO_LVR_N.

MO_LVR_N	LVR function
0	Enable
1	Disable

The voltage detection circuit is temperature compensated to prevent the detection voltage from drifting with temperature variation.
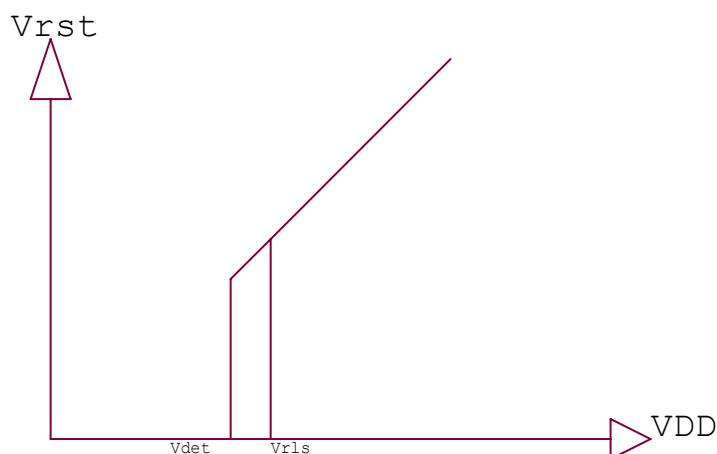
14.   Dual-Tone Multiple Frequency Generator

The Dual-Tone Multiple Frequency (DTMF) generator is used to generate the Tone Dialing signal used in Telecommunication applications. In fact, it can be used to generate any two channel sine wave signal with frequency ranging from 1 ~ 2047 Hz with 1 Hz resolution. The DTMF generator derives its clock from 32768 Hz oscillator.

The DTMF generator is controlled through DTMFC (DTMF Control) Register. It is write only, and can not be to read. The DTMFC register actually maps to Row Register, Column Register and Command Register. So when writing to DTMFC, the actual register being written is determined by Bit 7 and 6.

DTMFC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ROW HIGH	0	0	X	M10	M9	M8	M7	M6
ROW LOW	0	0	M5	M4	M3	M2	M1	M0
COL HIGH	0	1	X	M10	M9	M8	M7	M6
COL LOW	0	1	M5	M4	M3	M2	M1	M0
COMMAND	1	1	HOOK	-	MUTE	-	DTMF	HB(1)/LB(0)

Bit 5 of command register (HOOK bit) is the main switch of DTMF Generator block. When HOOK Bit is '1', the entire block will be turned off and all internal registers will be reset. When HOOK Bit is '0', the block will be turned on.

The Row and Column registers determine the frequencies of two channels sine wave generator. As they are 11-bit register, they need to be divided into high parts and low part when writing. The procedure of changing the Row and Column frequency is by selecting High or Low byte to be written in the command register, write to the target register, then toggle the HB/LB bit, and then write to the second part of the register. When both frequencies are set, the DTMF tone can be sent to DTMFO output by turning on bit 1 (DTMF bit) of command register. When DTMF bit is '1', DTMF signal can be output, and the output is disabled when DTMF bit is '0'.

In addition to DTMF generation function, this function block also provides others features which are useful for the phone application. For example, MUTE bit (bit 3) of command register directly controls the state of output pin MUTE. When MUTE bit is '1', the state is MUTE pin is set to high impedance 'Z', while MUTE bit is '0', the state of MUTE pin is '0'. This pin is useful for muting the microphone of telephone speech network to prevent speech signal from interfering the DTMF dialing signal when it is been generated.

15. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

16. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

17. AC/DC Characteristics

Test Condition: Temp. = 25℃, VDD = 3V±10%, GND=0V

PARAMETER	Symbol	MIN	TYP	MAX	UNIT	CONDITION
Normal mode current	I_{FAST}		0.75	1	mA	2M ext. R/C
Slow mode current	I_{SLOW}		6	9	μA	32768 Hz, LCD Disabled
Idle mode current	I_{IDLE}		4	7	μA	32768 Hz, LCD Disabled
Additional current if LCD ON	I_{LCD}		2	3	μA	LCD Enabled
Sleep mode current	I_{SLEEP}			1	μA	
Input high voltage	V_{IH}	0.8			V_{DD}	Input pins
Input Low Voltage	V_{IL}			0.2	V_{DD}	Input pins
Input Hysteresis Width	V_{HYS}		1/3		V_{DD}	I/O, RSTP_N, Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)
Output source current	I_{OH}	50			μA	Output drive high*1, V_{OH} =2.0V
Output sink current	I_{OL1}	1.0			mA	Output drive low, V_{OL}= 0.4V
Input Low Current	I_{IL2}		100		μA	I/O, V_{IL}= GND, pull high Internally
Input Low Current	I_{IL1}		20		μA	RSTP_N, V_{IL}= GND, pull high Internally

1. The "Output source current" specification is applicable only to the Push-Pull I/O type.

18. Application Circuit
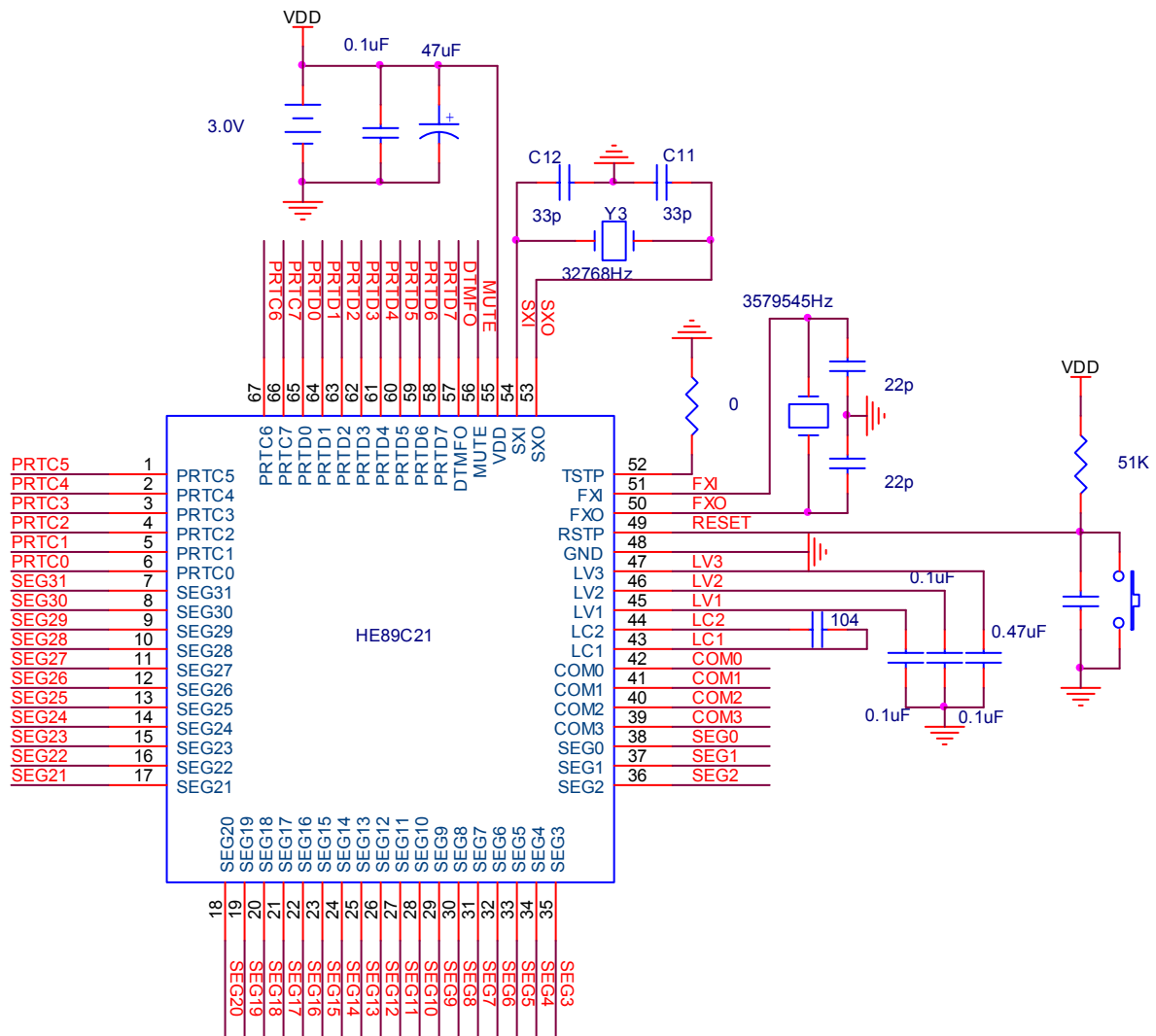
19. Important Note

1. Please bond the TSTP_P, RSTP_N and PRTD[7:0] with test points on PCB, which can be soldered and probed, and connect TSTP_P pin with zero ohm resistor to GND (or copper wire which can be cut easily on PCB) for good ESD protection. So that IC testing can be done on PCB, if necessary by removing the 0-ohm resistor and driving TSTP_P pin to high.LV3 must small than 9.0 Volt. Otherwise IC may breakdown.

20. Updated Record

Version	Date	Section	Original Content	New Content