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1. General Description

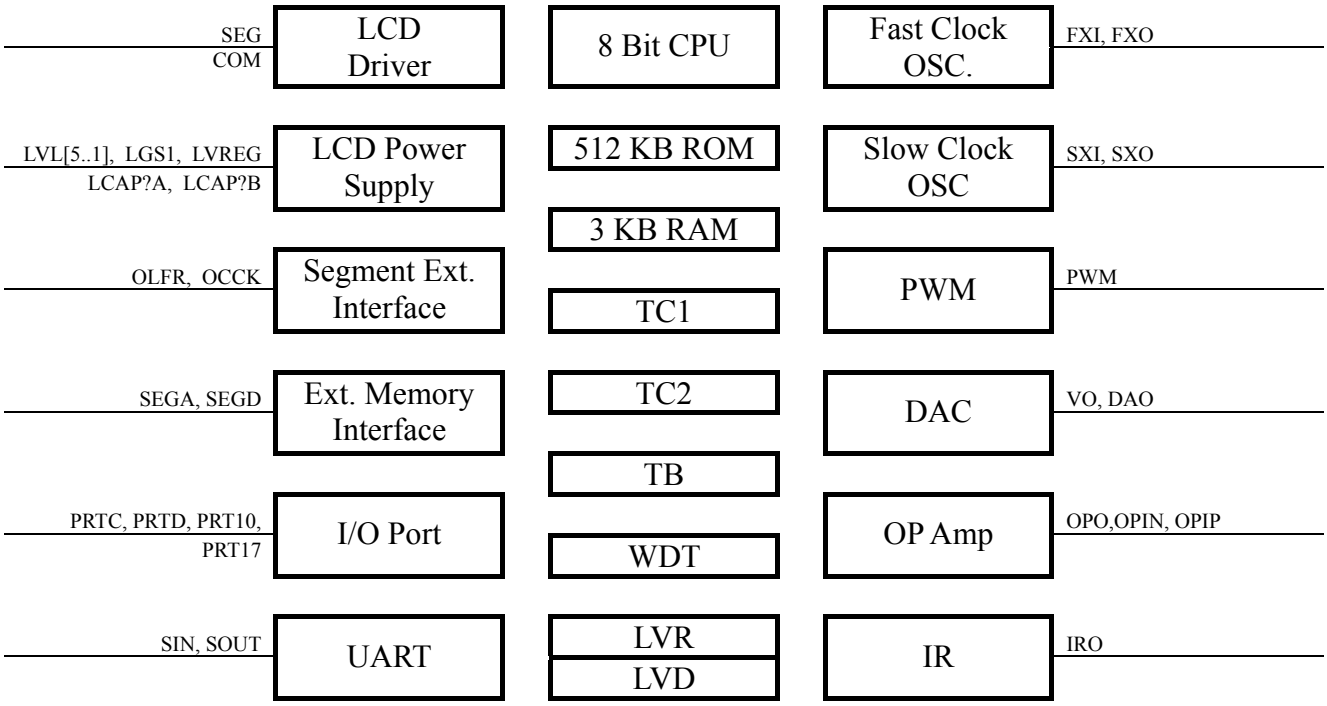
HE84G752B is a member of 8-bit Micro-controller series developed by King Billion Electronics. External address and data buses are provided to access external memory. This chip has 4096 pixel, 16 gray-scale LCD driver built-in with 4 different configurations, and up to 34-bit general purpose I/O ports. The built-in OP comparator can be used with light, voice, temperature and humility sensor or used to detect the battery low. The 7/8 bits current-type D/A converter and PWM driver output provides the complete speech output solutions. The 512K bytes ROM and 3K bytes RAM can be used for the storage of large speech data, image and text, etc. An UART is included to provide the serial communication capability. IR output makes it suitable for remote control applications.

The instruction sets of HE80000 series is easy to learn and simple to use. There are only thirty-two instructions and four addressing modes. Most of instructions take only 3 oscillator clocks to complete. The performance and low power consumption make it suitable for battery-powered applications such as translator, data bank, educational toy, digital voice recorder, etc.

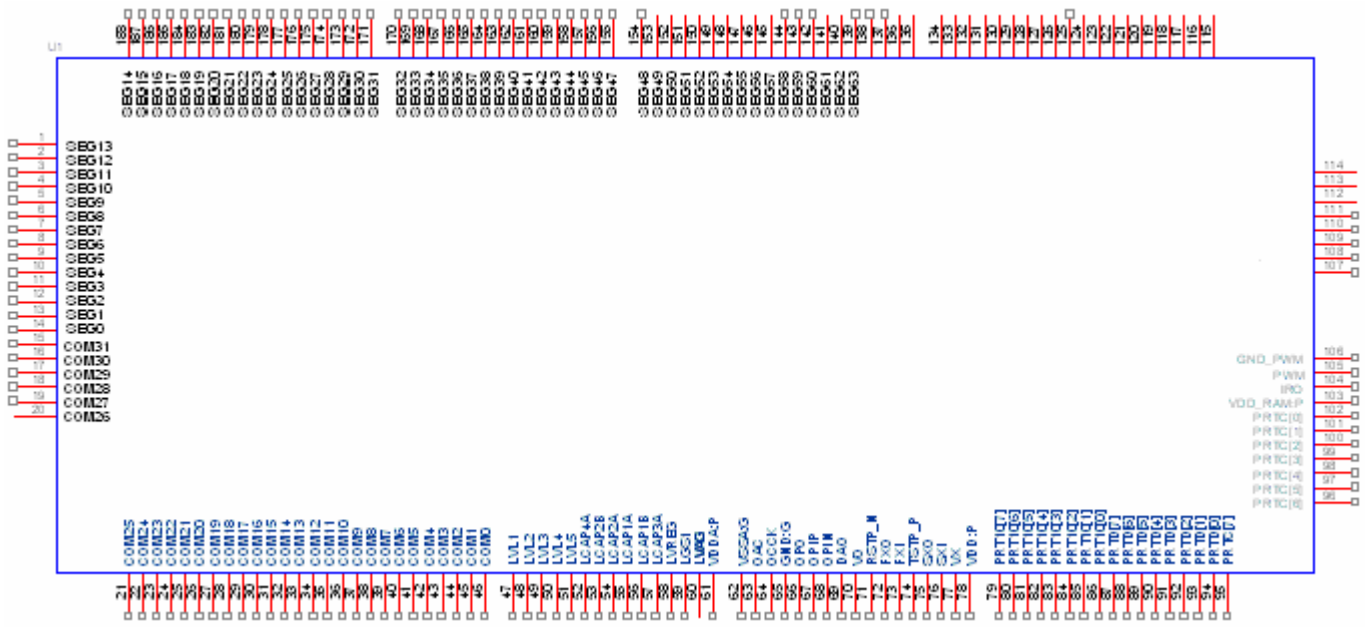
2. Features

- ✓ Operation Voltage: 2.4V ~ 3.6V
- ✓ Dual Clock System: Fast clock 32768 Hz ~ 8 MHz
  Slow clock 32768 Hz
- ✓ Four operation modes: Fast, Slow, Idle, Sleep modes.
- ✓ Internal Program ROM: 256K bytes
- ✓ Internal Data ROM: 256K bytes
- ✓ Internal RAM: 3 K bytes (page0~page11)
- ✓ 24 bi-directional general-purpose I/O ports with push-pull or Open-Drain output type selectable for each I/O pin by mask option.
- ✓ Up to 2048 pixels 16, 4 gray-scale or Black/White LCD driver.
- ✓ Segment extender interface with KD83 and KD80.
- ✓ 4 LCD configurations (COM X SEG): 32 COM x 64 SEG.
- ✓ Built-in LCD power supply with regulator and 3, 4, and 5 times charge pump circuit.
- ✓ One 7/8-bit current-type D/A converter.
- ✓ One 7/8-bit PWM output.
- ✓ One built-in OP comparator.
- ✓ Built-in UART for serial communication.
- ✓ IR output.
- ✓ Low voltage reset: 2.2V
- ✓ Low voltage detection: 2.4V, 2.6V, 2.8V and 3.0V
- ✓ Two external interrupts, three internal timer interrupts and extension UART interrupt
- ✓ Watch dog timer to prevent deadlock condition.
- ✓ Two 16-bit timers and one time-base timer.
- ✓ Instruction set: 32 instructions, 4 addressing mode.

3. Functional Block Diagram



4. Pin Description



Pin Name	Pin #	I/O	Description
COM[31..0]	15~ 46	O	LCD COMMON Driver Pads.
SEG[63:0]	1~14 139~188	O	LCD SEGMENT Driver Pads
LVL1	47	P	LCD Bias Voltage 1.
LVL2	48	P	LCD Bias Voltage 2

Pin Name	Pin #	I/O	Description
LVL3	49	P	LCD Bias Voltage 3
LVL4	50	P	LCD Bias Voltage 4
LVL5	51	P	LCD Bias Voltage 5.
LCAP4A	52	O	Charge Pump Capacitor Pin.
LCAP2B	53	O	Charge Pump Capacitor Pin.
LCAP2A	54	O	Charge Pump Capacitor Pin.
LCAP1A	55	O	Charge Pump Capacitor Pin.
LCAP1B	56	O	Charge Pump Capacitor Pin.
LCAP3A	57	O	Charge Pump Capacitor Pin.
LVREG	58	O	Voltage Regulator Output. VDD is regulated to generate LVREG, which is in turns pumped to LVP. Adjust resistor between LGS1 and LVREG to set LVREG voltage.
LGS1	59	I	Regulator Voltage Setting
LVAG	60	O	Reference Voltage Output. Fixed 0.9 Volt DC reference voltage
VDD_LCD(VDDA)	61	P	Power supply for LCD charge-pump.
GND_LCD(VSSA)	62	P	LCD power system ground.
OAC	63	O	LCD frame signal for interfacing with LCD segment extender KD80.
OCCK	64	O	LCD data load pin for interfacing with LCD segment extender KD80.
GND	65	P	Power ground Input.
OPO	66	O	Output of OP Amp.
OPIP	67	I	Non-inverting input of OP Amp.
OPIN	68	I	Inverting input of OP Amp.
DAO	69	O	Alternate output of DAC.
VO	70	O	DAC Output.
RSTP_N	71	I	System Reset input pin. Level trigger, active low on this pin will put the chip in reset state.
FXO, FXI	72, 73	O, B	External fast clock pin. Two types of oscillator can be selected by MO_FXTAL (‘0’ for RC type and ‘1’ for crystal type). For RC type oscillator, one resistor needs to be connected between FXI and GND. For crystal oscillator, one crystal needs to be placed between FXI and FXO. Please refer to application circuit for details.
TSTP_P	74	I	Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
SXO, SXI	75, 76	O, I	External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base and other internal blocks. Both crystal and RC oscillator are provided. The slow clock type can be selected by mask option MO_SXTAL. Choose ‘0’ for RC type and ‘1’ for crystal oscillator.
VX	77	I	Input pin for x32 PLL circuit. Connect to external resistor and capacitors as shown in application circuit.
VDD	78	P	Positive power Input. A 0.1 µF decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect.
PRT10[7..0]	79~86	B	8-bit bi-directional I/O port 10. The output type of I/O pad can also be selected by mask option MO_10PP[7..0] (‘1’ for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O pad as input pad, “1” must be outputted before reading.
PRTD[7..2] PRTD[1]/SIN PRTD[0]/SOUT	87~94	B	8-bit bi-directional I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7..0] (‘1’ for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, ‘1’ must be outputted before reading the pin. PRTD[7..2] can be used as wake-up pins. PRTD[7..6] can be as external interrupt sources. PRTD[1] shares pad with UART Receiver SIN pin. PRTD[0] shares pad with UART transmitter SOUT pin.
PRTC[7:0]	95~102	B	8-bit bi-directional I/O port C. The output type of I/O pad can also be selected by mask option MO_CPP[7..0] (‘1’ for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, ‘1’ must be outputted before reading the pin.
VDD_RAM	103	P	Dedicated power input for RAM
IRO	104	O	The Infrared output.
PWM	105	O	The PWM output can drive speaker or buzzer directly. Using VDD & PWM to drive

Pin Name	Pin #	I/O	Description
			output device.
GND_PWM	106	P	Dedicated Ground for PWM output.
NC	107~138		

I: Input, O: Output, B: Bidirectional, P: Power.

5. Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate
1	SEG[13]	X= -4123.60	Y= 934.55
2	SEG[12]	X= -4123.60	Y= 834.55
3	SEG[11]	X= -4123.60	Y= 734.55
4	SEG[10]	X= -4123.60	Y= 634.55
5	SEG[9]	X= -4123.60	Y= 534.55
6	SEG[8]	X= -4123.60	Y= 434.55
7	SEG[7]	X= -4123.60	Y= 334.55
8	SEG[6]	X= -4123.60	Y= 234.55
9	SEG[5]	X= -4123.60	Y= 134.55
10	SEG[4]	X= -4123.60	Y= 34.55
11	SEG[3]	X= -4123.60	Y= -65.45
12	SEG[2]	X= -4123.60	Y= -165.45
13	SEG[1]	X= -4123.60	Y= -265.45
14	SEG[0]	X= -4123.60	Y= -365.45
15	COM[31]	X= -4123.60	Y= -465.45
16	COM[30]	X= -4123.60	Y= -565.45
17	COM[29]	X= -4123.60	Y= -665.45
18	COM[28]	X= -4123.60	Y= -765.45
19	COM[27]	X= -4123.60	Y= -865.45
20	COM[26]	X= -4123.60	Y= -965.45
21	COM[25]	X= -3930.50	Y= -1354.55
22	COM[24]	X= -3830.50	Y= -1354.55
23	COM[23]	X= -3730.50	Y= -1354.55
24	COM[22]	X= -3630.50	Y= -1354.55
25	COM[21]	X= -3530.50	Y= -1354.55
26	COM[20]	X= -3430.50	Y= -1354.55
27	COM[19]	X= -3330.50	Y= -1354.55
28	COM[18]	X= -3230.50	Y= -1354.55

29	COM[17]	X= -3130.50	Y= -1354.55
30	COM[16]	X= -3030.50	Y= -1354.55
31	COM[15]	X= -2930.50	Y= -1354.55
32	COM[14]	X= -2830.50	Y= -1354.55
33	COM[13]	X= -2730.50	Y= -1354.55
34	COM[12]	X= -2630.50	Y= -1354.55
35	COM[11]	X= -2530.50	Y= -1354.55
36	COM[10]	X= -2430.50	Y= -1354.55
37	COM[9]	X= -2330.50	Y= -1354.55
38	COM[8]	X= -2230.50	Y= -1354.55
39	COM[7]	X= -2130.50	Y= -1354.55
40	COM[6]	X= -2030.50	Y= -1354.55
41	COM[5]	X= -1930.50	Y= -1354.55
42	COM[4]	X= -1830.50	Y= -1354.55
43	COM[3]	X= -1730.50	Y= -1354.55
44	COM[2]	X= -1630.50	Y= -1354.55
45	COM[1]	X= -1530.50	Y= -1354.55
46	COM[0]	X= -1430.50	Y= -1354.55
47	LVL1	X= -1230.50	Y= -1354.55
48	LVL2	X= -1130.50	Y= -1354.55
49	LVL3	X= -1030.50	Y= -1354.55
50	LVL4	X= -930.50	Y= -1354.55
51	LVL5	X= -830.50	Y= -1354.55
52	LCAP4A	X= -730.50	Y= -1354.55
53	LCAP2B	X= -630.50	Y= -1354.55
54	LCAP2A	X= -530.50	Y= -1354.55
55	LCAP1A	X= -430.50	Y= -1354.55
56	LCAP1B	X= -330.50	Y= -1354.55
57	LCAP3A	X= -230.50	Y= -1354.55
58	LVREG	X= -130.50	Y= -1354.55
59	LGS1	X= -30.50	Y= -1354.55
60	LVAG	X= 69.50	Y= -1354.55
61	VDDA	X= 169.50	Y= -1354.55
62	VSSA	X= 369.50	Y= -1354.55
63	OAC	X= 469.50	Y= -1354.55
64	OCCK	X= 569.50	Y= -1354.55
65	GND	X= 669.50	Y= -1354.55
66	OPO	X= 769.50	Y= -1354.55
67	OPIP	X= 869.50	Y= -1354.55

68	OPIN	X= 969.50	Y= -1354.55
69	DAO	X= 1069.50	Y= -1354.55
70	VO	X= 1169.50	Y= -1354.55
71	RSTP_N	X= 1269.50	Y= -1354.55
72	FXO	X= 1369.50	Y= -1354.55
73	FXI	X= 1469.50	Y= -1354.55
74	TSTP_P	X= 1569.50	Y= -1354.55
75	SXO	X= 1669.50	Y= -1354.55
76	SXI	X= 1769.50	Y= -1354.55
77	VX	X= 1869.50	Y= -1354.55
78	VDD	X= 1969.50	Y= -1354.55
79	PRT10[7]	X= 2169.50	Y= -1354.55
80	PRT10[6]	X= 2269.50	Y= -1354.55
81	PRT10[5]	X= 2369.50	Y= -1354.55
82	PRT10[4]	X= 2469.50	Y= -1354.55
83	PRT10[3]	X= 2569.50	Y= -1354.55
84	PRT10[2]	X= 2669.50	Y= -1354.55
85	PRT10[1]	X= 2769.50	Y= -1354.55
86	PRT10[0]	X= 2869.50	Y= -1354.55
87	PRTD[7]	X= 2969.50	Y= -1354.55
88	PRTD[6]	X= 3069.50	Y= -1354.55
89	PRTD[5]	X= 3169.50	Y= -1354.55
90	PRTD[4]	X= 3269.50	Y= -1354.55
91	PRTD[3]	X= 3369.50	Y= -1354.55
92	PRTD[2]	X= 3469.50	Y= -1354.55
93	PRTD[1]	X= 3569.50	Y= -1354.55
94	PRTD[0]	X= 3669.50	Y= -1354.55
95	PRTC[7]	X= 3769.50	Y= -1354.55
96	PRTC[6]	X= 4122.00	Y= -1126.45
97	PRTC[5]	X= 4122.00	Y= -1026.45
98	PRTC[4]	X= 4122.00	Y= -926.45
99	PRTC[3]	X= 4122.00	Y= -826.45
100	PRTC[2]	X= 4122.00	Y= -726.45
101	PRTC[1]	X= 4122.00	Y= -626.45
102	PRTC[0]	X= 4122.00	Y= -526.45
103	VDD_RAM	X= 4122.00	Y= -426.45
104	IRO	X= 4122.00	Y= -326.45
105	PWM	X= 4122.00	Y= -226.45
106	GND_PWM	X= 4122.00	Y= -126.45

107	NC	X= 4122.00	Y= 473.55
108	NC	X= 4122.00	Y= 573.55
109	NC	X= 4122.00	Y= 673.55
110	NC	X= 4122.00	Y= 773.55
111	NC	X= 4122.00	Y= 873.55
112	NC	X= 4122.00	Y= 973.55
113	NC	X= 4122.00	Y= 1073.55
114	NC	X= 4122.00	Y= 1173.55
115	NC	X= 3668.40	Y= 1354.05
116	NC	X= 3568.40	Y= 1354.05
117	NC	X= 3468.40	Y= 1354.05
118	NC	X= 3368.40	Y= 1354.05
119	NC	X= 3268.40	Y= 1354.05
120	NC	X= 3168.40	Y= 1354.05
121	NC	X= 3068.40	Y= 1354.05
122	NC	X= 2968.40	Y= 1354.05
123	NC	X= 2868.40	Y= 1354.05
124	NC	X= 2768.40	Y= 1354.05
125	NC	X= 2668.40	Y= 1354.05
126	NC	X= 2568.40	Y= 1354.05
127	NC	X= 2468.40	Y= 1354.05
128	NC	X= 2368.40	Y= 1354.05
129	NC	X= 2268.40	Y= 1354.05
130	NC	X= 2168.40	Y= 1354.05
131	NC	X= 2068.40	Y= 1354.05
132	NC	X= 1968.40	Y= 1354.05
133	NC	X= 1868.40	Y= 1354.05
134	NC	X= 1768.40	Y= 1354.05
135	NC	X= 1568.40	Y= 1354.05
136	NC	X= 1468.40	Y= 1354.05
137	NC	X= 1368.40	Y= 1354.05
138	NC	X= 1268.40	Y= 1354.05
139	SEG[63]	X= 1168.40	Y= 1354.05
140	SEG[62]	X= 1068.40	Y= 1354.05
141	SEG[61]	X= 968.40	Y= 1354.05
142	SEG[60]	X= 868.40	Y= 1354.05
143	SEG[59]	X= 768.40	Y= 1354.05
144	SEG[58]	X= 668.40	Y= 1354.05
145	SEG[57]	X= 568.40	Y= 1354.05

146	SEG[56]	X= 468.40	Y= 1354.05
147	SEG[55]	X= 368.40	Y= 1354.05
148	SEG[54]	X= 268.40	Y= 1354.05
149	SEG[53]	X= 168.40	Y= 1354.05
150	SEG[52]	X= 68.40	Y= 1354.05
151	SEG[51]	X= -31.60	Y= 1354.05
152	SEG[50]	X= -131.60	Y= 1354.05
153	SEG[49]	X= -231.60	Y= 1354.05
154	SEG[48]	X= -331.60	Y= 1354.05
155	SEG[47]	X= -531.60	Y= 1354.05
156	SEG[46]	X= -631.60	Y= 1354.05
157	SEG[45]	X= -731.60	Y= 1354.05
158	SEG[44]	X= -831.60	Y= 1354.05
159	SEG[43]	X= -931.60	Y= 1354.05
160	SEG[42]	X= -1031.60	Y= 1354.05
161	SEG[41]	X= -1131.60	Y= 1354.05
162	SEG[40]	X= -1231.60	Y= 1354.05
163	SEG[39]	X= -1331.60	Y= 1354.05
164	SEG[38]	X= -1431.60	Y= 1354.05
165	SEG[37]	X= -1531.60	Y= 1354.05
166	SEG[36]	X= -1631.60	Y= 1354.05
167	SEG[35]	X= -1731.60	Y= 1354.05
168	SEG[34]	X= -1831.60	Y= 1354.05
169	SEG[33]	X= -1931.60	Y= 1354.05
170	SEG[32]	X= -2031.60	Y= 1354.05
171	SEG[31]	X= -2231.60	Y= 1354.05
172	SEG[30]	X= -2331.60	Y= 1354.05
173	SEG[29]	X= -2431.60	Y= 1354.05
174	SEG[28]	X= -2531.60	Y= 1354.05
175	SEG[27]	X= -2631.60	Y= 1354.05
176	SEG[26]	X= -2731.60	Y= 1354.05
177	SEG[25]	X= -2831.60	Y= 1354.05
178	SEG[24]	X= -2931.60	Y= 1354.05
179	SEG[23]	X= -3031.60	Y= 1354.05
180	SEG[22]	X= -3131.60	Y= 1354.05
181	SEG[21]	X= -3231.60	Y= 1354.05
182	SEG[20]	X= -3331.60	Y= 1354.05
183	SEG[19]	X= -3431.60	Y= 1354.05
184	SEG[18]	X= -3531.60	Y= 1354.05

185	SEG[17]	X= -3631.60	Y= 1354.05
186	SEG[16]	X= -3731.60	Y= 1354.05
187	SEG[15]	X= -3831.60	Y= 1354.05
188	SEG[14]	X= -3931.60	Y= 1354.05

6. ROM Map Configurations

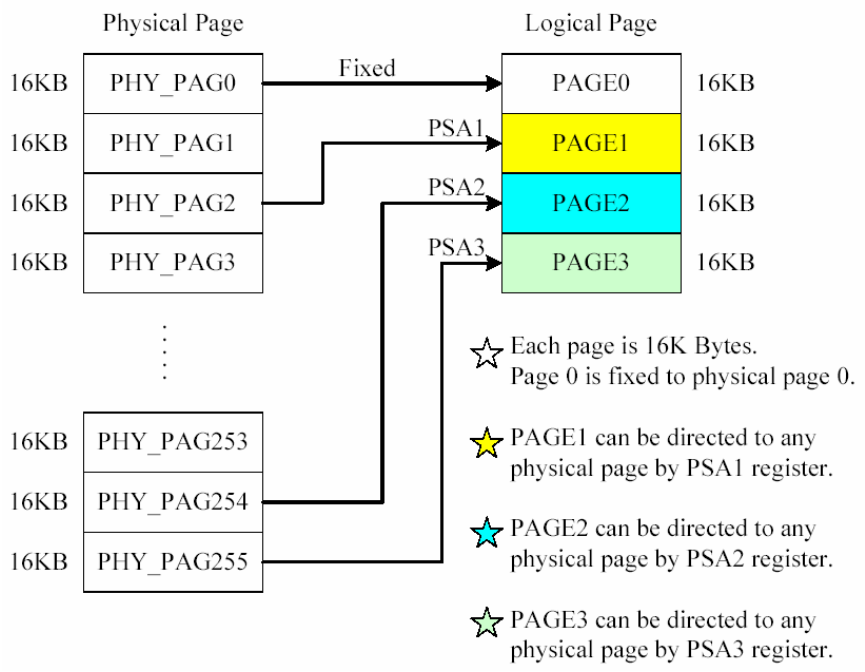
The chip has built-in 512K bytes internal ROM. In addition, address and data buses are provided to access External ROM. The MCU can access up to 4M bytes program ROM and up to 16M bytes data space through external buses. The SEG[47..40], SEG[39..16] pads are used as either data and address buses for external ROM or LCD segment driver pads depending on the mask option MO_EXMEM. When the external ROM mask option is selected, the MCU will retrieve the instructions and data from external ROM through the address and data buses.

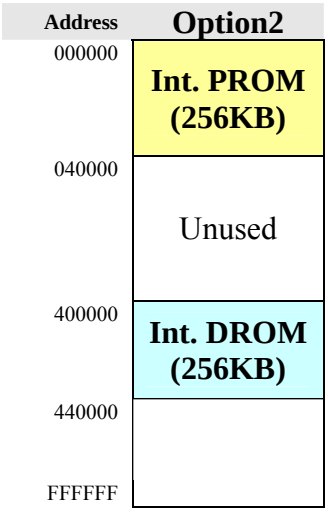
The bit 14 ~ 15 bit of 16-bit logical program address can be mapped to any one (16K bytes per page) of 256 pages through mapping registers PSA1, PSA2, PSA3. As logical page 0 can not be moved and is always physical page 0, the PSA1 ~ PSA3 contain the physical page addresses of logical pages 1 ~ 3.

Logical Address															
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Page Addr.		A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

A[15..14]	Logical Page	Physical Page Address	Physical Address
00	0	0	00A[13..0]
01	1	PSA1	PSA1+A[13..0]
10	2	PSA2	PSA2+A[13..0]
11	3	PSA3	PSA3+A[13..0]

Register	Address	Type	Bits Definition								Reset
PSA1	0x2C	R/W	A21	A20	A19	A18	A17	A16	A15	A14	0x01
PSA2	0x2D	R/W	A21	A20	A19	A18	A17	A16	A15	A14	0x02
PSA3	0x2E	R/W	A21	A20	A19	A18	A17	A16	A15	A14	0x03





7. LCD Display RAM Map

The gray-scale LCD driver can be configured to be a 16 gray-scale, 4 gray-scales or black and white display by mask option MO_GRAY_MODE.

MO_GRAY_MODE[1..0]	Gray levels
00	16

01	4
10	2 (B/W)
11	2 (B/W)

For 4 gray-scale display, 2-bit of RAM is required for each pixel and 4 bit for 16 gray-scale display, 1-bit for black and white display. For different LCD configuration, the LCD display RAM is arranged differently. The following figure shows one byte of RAM in different LCD configurations:

0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Black/White	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
4 Gray scales	SEG3		SEG2		SEG1		SEG0	
16 Gray scales	SEG1				SEG0			

The 16 Gray Scale register GRAY0 ~ GRAYF is the mapping register between the levels selected in RAM and the real gray scale. In other words, if the content of GRAY0 is 0x03, when value of a certain pixel is 0, the displayed effect will correspond to actual gray level 3. The 16 gray scale display use all 16 registers GRAY0 ~ GRAYF to select among 32 available gray levels to correspond to level 0 ~ 15, while 4 gray scale display utilizes registers GRAY0 ~ GRAY3 to select among 32 gray levels to correspond to level 0 ~ 3. Thus user can pick the gray levels which give the best and most linear effect.

16 Gray Scale registers share a common register address GRAY16. When writing is made to the register, it will step down to next register in order. The writing sequence can be reset by clearing bit 5 of LCDC register.

GRAY16	**Field**					
Seq.	Bit4	Bit3	Bit2	Bit1	Bit0	Reset
1	GRAY0					0x00
2	GRAY1					0x02
3	GRAY2					0x04
4	GRAY3					0x06
5	GRAY4					0x08
6	GRAY5					0x0A
7	GRAY6					0x0C
8	GRAY7					0x0E
9	GRAY8					0x10
10	GRAY9					0x12
11	GRAYA					0x14
12	GRAYB					0x16
13	GRAYC					0x18
14	GRAYD					0x1A
15	GRAYE					0x1C
16	GRAYF					0x1E

7.1. 16 Gray Scale LCD Display RAM Map

	Cnf	32 X 64	
Page	Loc.	F 0	
1	00	S31 ~ S00	COM0
	10	S63 ~ S32	
	20		
	30	*	
	40	S31 ~ S00	COM1
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM2
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM3
	D0	S63 ~ S32	
	E0		
	F0	*	
2	00	S31 ~ S00	COM4
	10	S63 ~ S32	
	20	*	
	30	*	
	40	S31 ~ S00	COM5
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM6
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM7
	D0	S63 ~ S32	
	E0	*	
	F0	*	
3	00	S31 ~ S00	COM8
	10	S63 ~ S32	
	20	*	
	30	*	
	40	S31 ~ S00	COM9
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM10
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM11
	D0	S63 ~ S32	
	E0	*	
	F0	*	
4	00	S31 ~ S00	COM12
	10		
	20	S95 ~ S64	
	30	*	

	Cnf	32 X 64	
Page	Loc.	F 0	
	40	S31 ~ S00	COM13
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM14
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM15
	D0	S63 ~ S32	
	E0	*	
	F0	*	
5	00	S31 ~ S00	COM16
	10	S63 ~ S32	
	20	*	
	30	*	
	40	S31 ~ S00	COM17
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM18
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM19
	D0	S63 ~ S32	
	E0	*	
	F0	*	
6	00	S31 ~ S00	COM20
	10	S63 ~ S32	
	20	*	
	30	*	
	40	S31 ~ S00	COM21
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM22
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM23
	D0	S63 ~ S32	
	E0	*	
	F0	*	
7	00	S31 ~ S00	COM24
	10	S63 ~ S32	
	20	S95 ~ S64	
	30	*	
	40	S31 ~ S00	COM25
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM26
	90	S63 ~ S32	
	A0	*	

	Cnf	32 X 64	
Page	Loc.	F 0	
	B0	*	
	C0	S31 ~ S00	COM27
	D0	S63 ~ S32	
	E0	*	
	F0	*	
8	00	S31 ~ S00	COM28
	10	S63 ~ S32	
	20	*	
	30	*	
	40	S31 ~ S00	COM29
	50	S63 ~ S32	
	60	*	
	70	*	
	80	S31 ~ S00	COM30
	90	S63 ~ S32	
	A0	*	
	B0	*	
	C0	S31 ~ S00	COM31
	D0	S63 ~ S32	
	E0	*	
	F0	*	

7.2. 4 Gray Scale LCD Display RAM Map

	Cnf	32x64		
Page	Loc.	F 0		
1	00	S63 ~ S00		COM0
	10	*	*	
	20	S63 ~ S00		COM1
	30	*	*	
	40	S63 ~ S00		COM2
	50	*	*	
	60	S63 ~ S00		COM3
	70	*	*	
	80	S63 ~ S00		COM4
	90	*	*	
	A0	S63 ~ S00		COM5
	B0	*	*	
	C0	S63 ~ S00		COM6
	D0	*	*	
	E0	S63 ~ S00		COM7
	F0	*	*	
2	00	S63 ~ S00		COM8
	10	*	*	
	20	S63 ~ S00		COM9
	30	*	*	
	40	S63 ~ S00		COM10
	50	*	*	
	60	S63 ~ S00		COM11
	70	*	*	
	80	S63 ~ S00		COM12
	90	*	*	
	A0	S63 ~ S00		COM13
	B0	*	*	

	Cnf	32x64		
Page	Loc.	F	0	
	C0	S63 ~ S00		COM14
	D0	*	*	
	E0	S63 ~ S00		COM15
	F0	*	*	
3	00	S63 ~ S00		COM16
	10	*	*	
	20	S63 ~ S00		COM17
	30	*	*	
	40	S63 ~ S00		COM18
	50	*	*	
	60	S63 ~ S00		COM19
	70	*	*	
	80	S63 ~ S00		COM20
	90	*	*	
	A0	S63 ~ S00		COM21
	B0	*	*	
	C0	S63 ~ S00		COM22
	D0	*	*	
	E0	S63 ~ S00		COM23
	F0	*	*	
4	00	S63 ~ S00		COM24
	10	*	*	
	20	S63 ~ S00		COM25
	30	*	*	
	40	S63 ~ S00		COM26
	50	*	*	
	60	S63 ~ S00		COM27
	70	*	*	
	80	S63 ~ S00		COM28
	90	*	*	
	A0	S63 ~ S00		COM29
	B0	*	*	
	C0	S63 ~ S00		COM30
	D0	*	*	
	E0	S63 ~ S00		COM31
	F0	*	*	

7.3. Black and White LCD Display RAM Map

	Cnf	32x64		
Page	Loc.	F	0	
1	00	*	S63 ~ S00	COM0
	10	*	S63 ~ S00	COM1
	20	*	S63 ~ S00	COM2
	30	*	S63 ~ S00	COM3
	40	*	S63 ~ S00	COM4
	50	*	S63 ~ S00	COM5
	60	*	S63 ~ S00	COM6
	70	*	S63 ~ S00	COM7
	80	*	S63 ~ S00	COM8
	90	*	S63 ~ S00	COM9
	A0	*	S63 ~ S00	COM10
	B0	*	S63 ~ S00	COM11
	C0	*	S63 ~ S00	COM12

	Cnf	32x64		
Page	Loc.	F	0	
	D0	*	S63 ~ S00	COM13
	E0	*	S63 ~ S00	COM14
	F0	*	S63 ~ S00	COM15
2	00	*	S63 ~ S00	COM16
	10	*	S63 ~ S00	COM17
	20	*	S63 ~ S00	COM18
	30	*	S63 ~ S00	COM19
	40	*	S63 ~ S00	COM20
	50	*	S63 ~ S00	COM21
	60	*	S63 ~ S00	COM22
	70	*	S63 ~ S00	COM23
	80	*	S63 ~ S00	COM24
	90	*	S63 ~ S00	COM25
	A0	*	S63 ~ S00	COM26
	B0	*	S63 ~ S00	COM27
	C0	*	S63 ~ S00	COM28
	D0	*	S63 ~ S00	COM29
	E0	*	S63 ~ S00	COM30
	F0	*	S63 ~ S00	COM31

8. LCD Power Supply

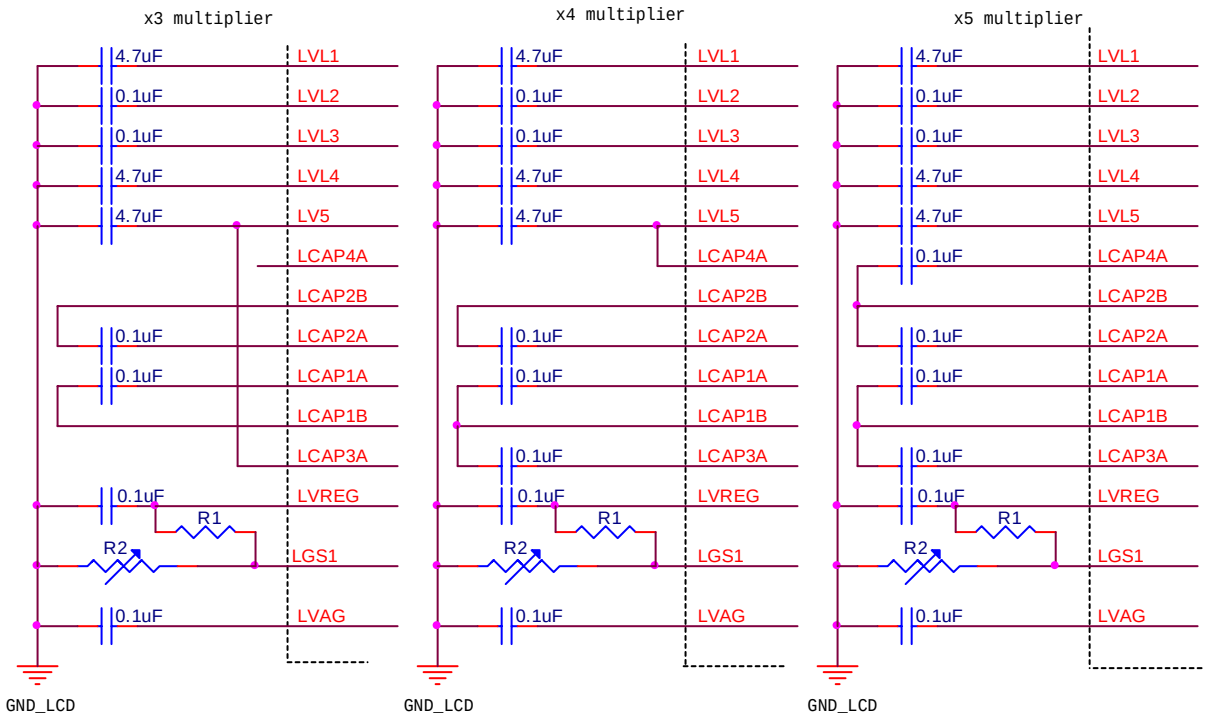
The built-in LCD power supply is equipped with input voltage regulator, voltage multiplier and bias voltage generating circuit with active buffer instead of passive resistor voltage dividing network. If the external LCD power is provided, the internal LCD power system shall be disabled. The following table shows the relationship of the LCD power system

LCDE(LCDC BIT0)	MO_PSMODE[1:0]	Function
1	00	Internal voltage multiplier and Bias voltage generating circuit are enable to supply the LCD display power.
1	01	Internal voltage multiplier is enabled, but the Bias voltage generating circuit is disabled,and the external power sources are applied LV4~LV1.
1	10	Internal voltage multiplier is disabled, but the Bias voltage generating circuit is enabled. The single external power is applied to LV5, and internal bias circuit will generate the LV4~LV1 voltages.
1	11	Internal voltage multiplier and Bias voltage generating circuit are disabled, and the external power sources are applied to LV5~LV1.
0	00	The lcd power system is disable,but the LV5~ LV1 is applied to VDD .
0	01	The lcd power system is disable,but the LV5 is applied to VDD and LV4~LV1 is applied to hight impedance.
0	10	The lcd power system is disable, LV5 is applied to hight impedance,and the LV4~LV1 Applied to LV5.
0	11	The lcd power system is disable, LV5~LV1 is applied to hight impedance.

when the internal LCD power system is used by internal voltage multiplier . The input voltage is regulated to LVREG using the internally by resistor between LGS1 and LVREG generated LVAG as reference voltage. LVREG can be adjusted

LVREG adjustment guideline: First, the level of VDD must be 0.3 volt higher than LVREG even at the end of battery life for the regulator to function properly. For example, if the VDD is expected to drop to 2.2 volts when battery is low, then the level of LVREG can only be set at 1.9 volts max. Secondly, the higher the level of LVREG, the less multiples it requires pumping LV5 to same level. For example, to pump the 2.25 volts to 9 volts requires 4 times multiplier; to pump the 3 volts to 9 volts requires only 3 time multiplier which consumes less power. So it is advisable not to adjust the LVREG to an unnecessary low level.

Voltage multiplication: The LVREG is then multiplied by 3, 4, or 5 times, depending on external capacitors configurations as shown below, to generate LV5. Please note that LV5 must be lower than 8.5 volts to prevent chip from breaking down.



Different duties require different bias settings. There is some theoretical correspondence between the Duty and Bias Setting. However, it is better to use it as starting point and adjust it with real LCD panel connected to it to determine the final setting. The theoretic relationship between the duty and bias setting as following:

Duty Cycle	Normal Bias	Alternative Bias
32 duty	1/7	1/7.5
48 duty	1/8	1/7.5, 1/8.5
64 duty	1/9	1/8.5, 1/9.5
80 duty	1/10	1/9.5, 1/10.5

The bias setting is made by mask option MO_LBSR[2..0].

MO_LBSR[2..0]	Bias Setting
000	1/7
001	1/7.5
010	1/8
011	1/8.5
100	1/9
101	1/9.5
110	1/10
111	**1/5**

9. LCDC Control register

LCD Control Register LCDC controls the functions of LCD driver.

LCDC	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	-	-	CLR_GP	GRAY			BLANK	LCDE
Mode	-	-	W	W			W	W
Reset	-	-	1	xxx			1	0

Field	Value	Function
CLR_GP	0	Reset GRAY palette register pointer by write ‘0’ to CLR_GP bit.
	1	No effect on GRAY palette register pointer.
GRAY	000	LCD is darkest.
	⋮	LCD display contrast adjustment.
	111	LCD is lightest.

Field	Value	Function
BLANK	0	Normal display.
	1	LCD display blanked. The COM signals of LCD driver output inactive levels (LVL4 and LVL1) while SEG signals output normal display patterns.
LCDE	0	LCD driver disabled, LCD driver has no output signal and applied to VDD
	1	LCD driver Enabled.

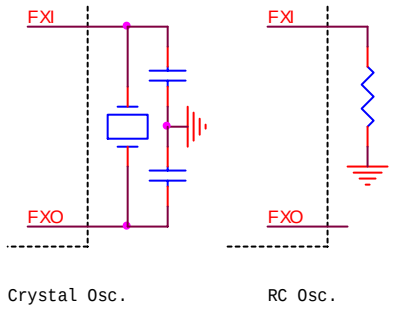
Please note that LCD driver must be turned off before the system goes into "sleep" mode. That means user must clear the bit 0 of LCDC to turn off LCD driving circuit before setting bit6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed.

Please note that LCD driver uses slow clock as clock source. The LCD display will not display normally if it works in Fast clock only mode because the LCD refresh action is too fast.

10. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. The system designer can select oscillator types based on the cost target, timing accuracy requirements etc. Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.



The RC oscillator has a built-in capacitor. An external resistor is needed to connect from FXI to GND to determine the oscillation frequency. The capacitance of internal RC oscillator is selected by mask option MO_RCAP[2..0].

MO_RCAP[2:0]	Internal RC Cap. (pF)
000	2
001	4
010	7
011	14
100	20
101	40

110	50
111	60

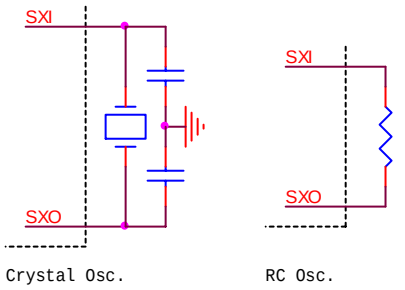
The following table shows the combinations of R and C, and the resulting frequency. Please note that oscillation frequency in the table only represents oscillation frequencies of certain samples. The actual oscillation frequency may vary up to ±15% from lot to lot due to process parameter variations. User must take this into consideration when using this chip in applications.

Ring Oscillator Frequency Table

R (KΩ) \ C (pF)	**40**	**20**	**14**	**7**	**4**	**2**	
30.20	0.8	1.5	2.0	3.0	4.0	5.0	MHz
19.92	1.2	2.2	2.8	4.4	5.6	7.0	MHz
9.98	2.3	4.0	5.1	7.5	**9.4**	**11.4**	MHz

Two types of oscillator, crystal and RC, can be used as slow clock selectable by mask option MO_SXTAL. If used time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to reduce cost.

MO_SXTAL	Slow clock type
0	R/C oscillator
1	Crystal oscillator



With two clock sources available, the system can switch among operation modes of Normal, Slow, Idle, and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as high speed or low power, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	W	W	W	W

Reset	0	-	-	0	-	-	-	-

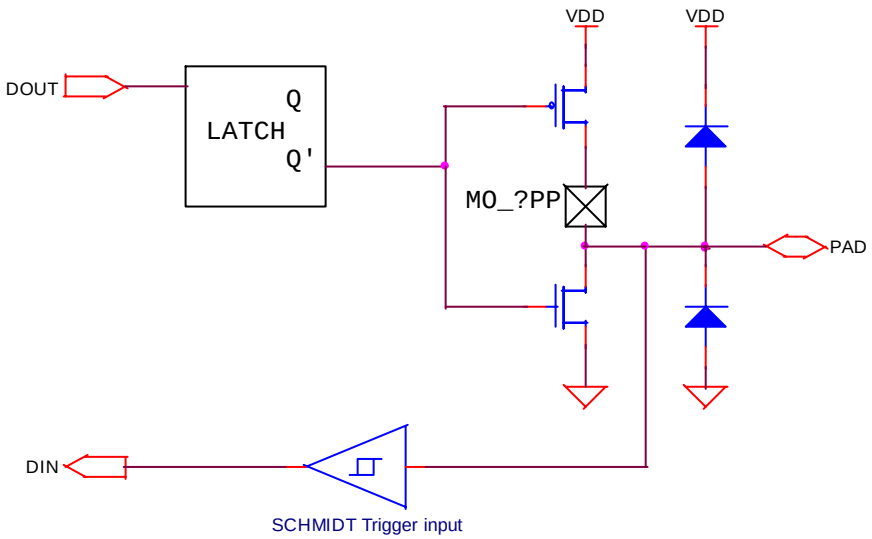
If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

11. General Purpose I/O

There are three dedicated general purpose I/O port, PRTC, PRTD and PRT10, while PRT15[1..0] and PRT17 are multiplexed with LCD segment driver pins. All the I/O Ports are bi-directional and of non-tri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. The hysteresis level of Schmidt trigger is 1/3 VDD.



As pads of PRT15 and PRT17 are shared with LCD segment driver, the function of the pad is determined by mask options. Following table is the setting for MO_LIO?[...] and MO_?PP[...] and others related to LCD display setting and pin assignment features.

MO_LIO?[…]	MO_?PP[...]	I/O Port	LCD Pin
0	0	Open-drain output	--
0	1	Push-pull output	--
1	0	--	xx
1	1	--	LCD Display

--: Function not available.

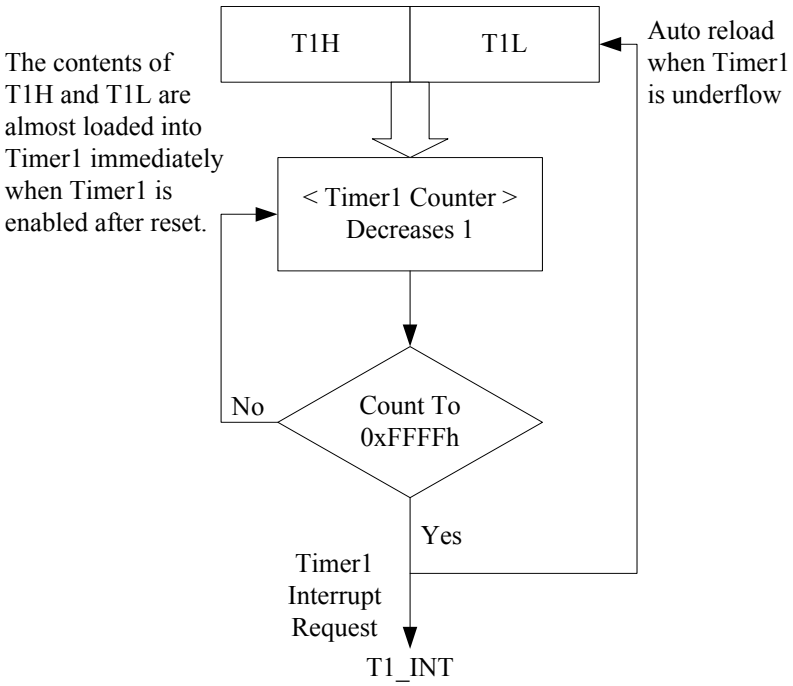
xx: Display enable, but may have abnormal leakage current, do not use.

12. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock "SCK" at dual clock or slow clock only mode. And it comes from the fast clock "FCK" at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

13. Timer2

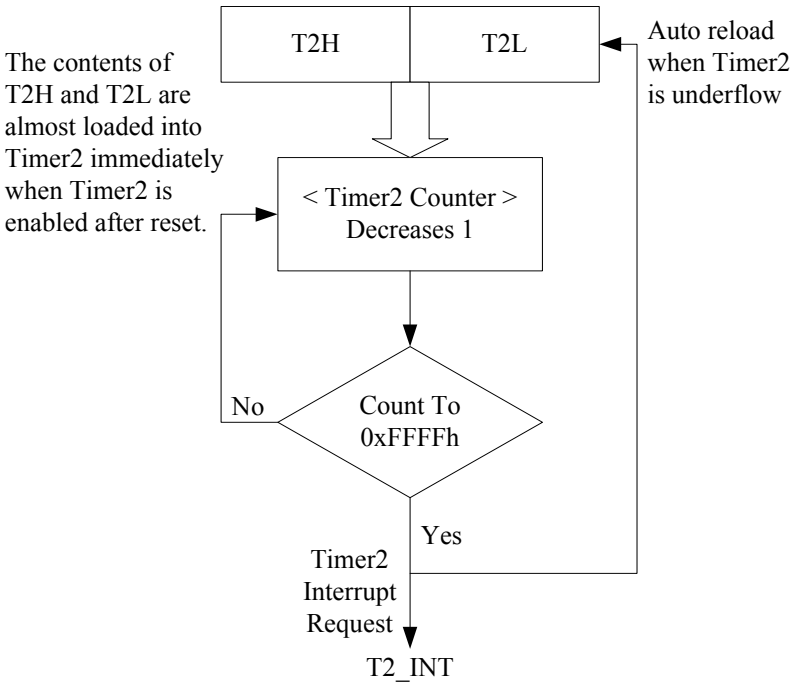
Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.

The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.



14. Time Base

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3..0]. TBE (Time Base Enable) bit controls enable or disable of the circuit.

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	-	-	0	-	-	-	-

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz

TBS[3..0]	Interrupt Frequency
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

15. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically and prevents system dead lock caused by abnormal hardware activities or program execution. The WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

Using the WDT function, the "CLRWDT" instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated to reset the system.

The WDT clock source is the same as TC1 (Timer1 clock), and the WDT reset signal is generated when the counter had counted 32768 clock. The WDT can function in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

16. Voice Output

There are 7 or 8 bits DAC/PWM voice output available for user. The 7 bits DAC/PWM output format and configuration are the same as the previous IC of HE80000 series. The 8 bits DAC/PWM format and configuration are new designed and controlled by the VOC and PWMC registers. The selection of 7/8 bits DAC/PWM output is by mask option **MO_8BVOC.**

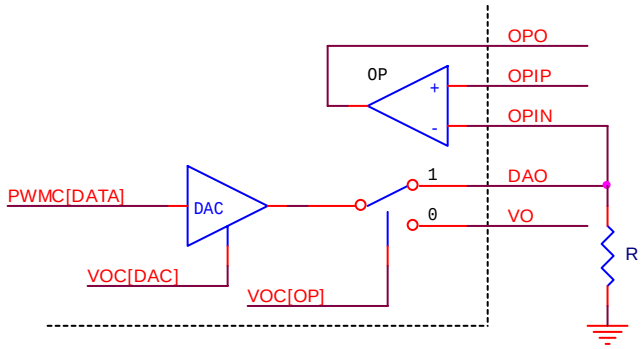
MO_8BVOC	Function
0	7-bit DAC/PWM output
1	8-bit DAC/PWM output

8-Bit DAC/PWM Output:

The Digital-to-Analog converter converts the 8-bit unsigned speech data which is written into PWMC data register to proportional current output.

PWMC	address	Reset	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	0x0E	--	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

There are two output paths for the DAC. Either VO or DAO can be selected as output port of DAC by VOC register when it is enabled. The VO output is primarily intended for speech generation, although it is not necessary so, while the DAO output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter as required in applications such as speech recording, speech recognition or sensor interfaces.

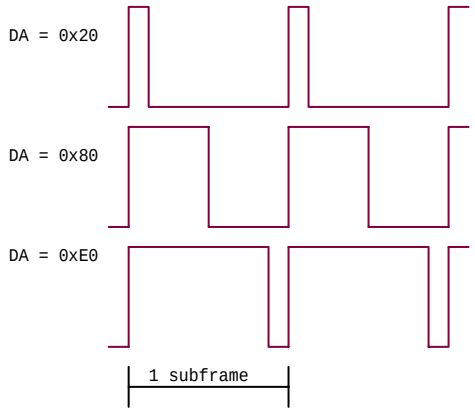


The DAC is enabled by DAC bit of VOC register. When DAC is enabled, the DAC output path can be selected to output to DAO or VO pin by OP bit of VOC register.

VOC	address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	0x13	-	PWM O/P driver			PWME	PWM	DAC	OP
Reset			0	0	0	0	0	0	0

Bit	Name	Value	Function description
VOC[3]	PWME	1	PWM Output Driver Enable
		0	PWM Output Driver Disable
VOC[2]	PWM	1	PWM Module Enable
		0	PWM Module Disable
VOC[1]	DAC	1	Digital-to-Analog Converter Enable
		0	Digital-to-Analog Converter Disable
VOC[0]	OP	1	DAC output to DAO pin
		0	DAC output to VO pin

The pulse-width modulator (PWM) converts 8-bit unsigned speech data which is written into PWMC data register to proportional duty cycle of PWM output. PWM module shares the same digital input register PWMC with Digit-to-Analog Converter. So PWM and DA output can exist at the same time. When PWM circuit is enabled, it generates signal with duty ratio in proportion to the value of PWMC register.



PWMC	address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	0x0E	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

VOC

VOC	address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	0x13	-	PWM O/P driver			PWME	PWM	DAC	OP
Reset			0	0	0	0	0	0	0

The PWM bit of VOC controls the enable/disable of the PWM circuit and output driver. When PWM bit of VOC is '0', PWME bit and output drivers are both cleared. To use PWM as voice output, PWM bit has to be set to '1' first, then set PWME bit and enable output driver by setting the driver number. If PWM bit is disabled and enabled again, the setting for driver and PWME bit will be clear.

The Fast Clock is gated through PWME bit of VOC register to provide the clock source of PWM circuit when it is enabled. As PWM needs higher frequency to operate, it cannot generate correct PWM signal in Slow clock only mode.

When the program enters into sleep mode or idle mode, it will automatically turn off all voice outputs by

clearing VOC[6:0] to ”0000000”. To activate voice output again when returning to normal mode, the VOC register needs to be set again.

The PWM output volume can be adjusted by command register VOC[6..4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM output driver selection

VOC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

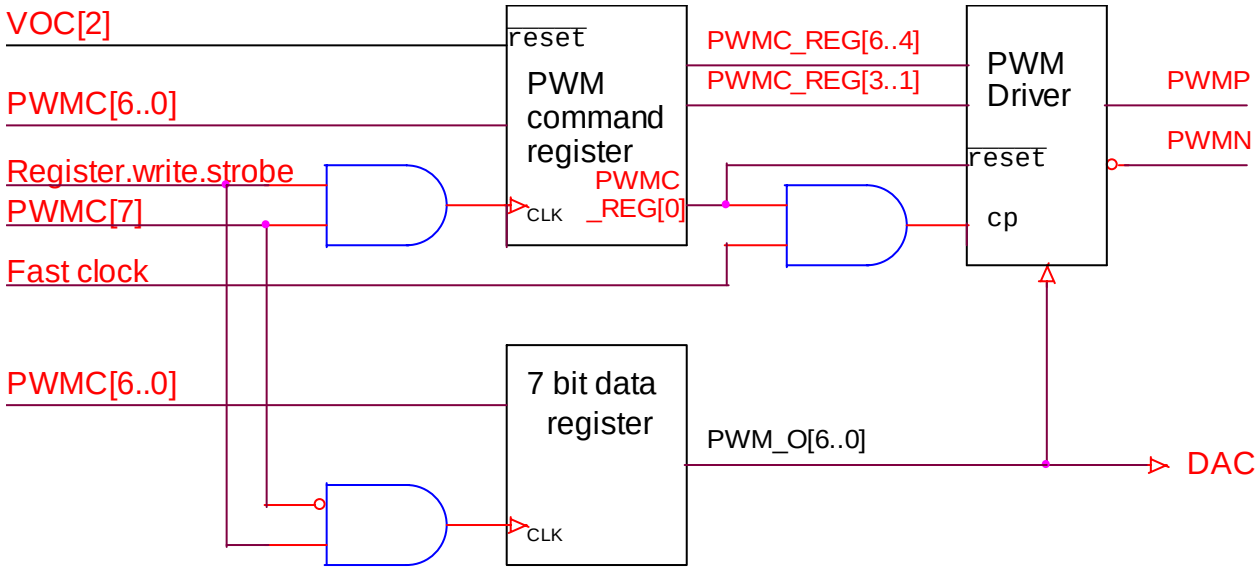
7-Bit DAC/PWM Output:

The 7-bit DAC/PWM voice generator is another scenario and the definitions of PWMC and VOC registers are different from the 8-bit DAC/PWM format. These register are described as following.

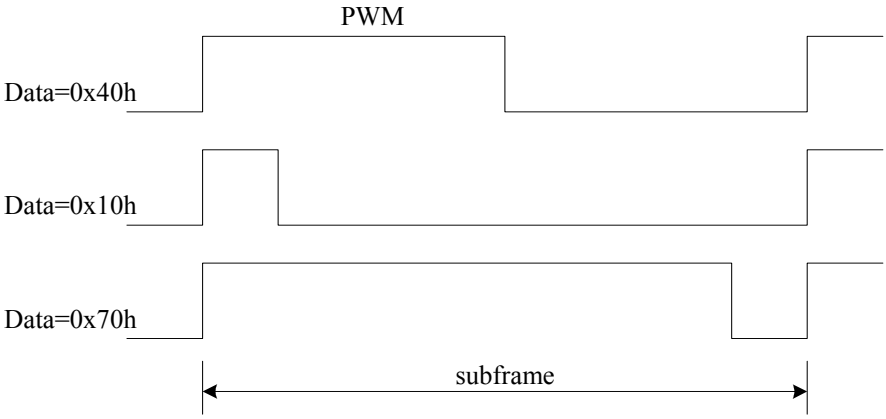
The 7-bit voice output is controlled by PWMC and VOC register, and the PWMC is a command/data register which is determined by PWMC[7] bit.

PWMC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA & PWM Data	0	DA and PWM output value						
Control	1	PWM O/P driver			Reserved			PWME

When users write data into the PWMC register, the PWMC[7] bit will determines the data written into PWM command register or 7-bit data register and the data register is also sent to the DA converter shown as the below diagram. The definitions of “PWME” bit and “PWM O/P driver” bits are the same as VOC register definition of 8-bit output mode.

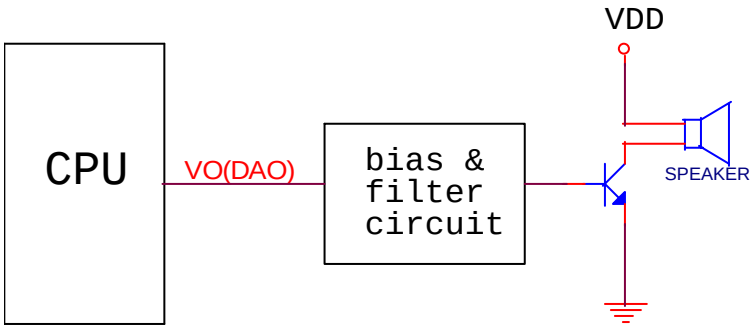


The fast clock is used to provide as PWM driver time base, and user shall set the PWMC[7]='1' and VOC[2]='1' to enable the PWM output. When the system enters into sleep or idle mode, it will automatically turn off the voice device by clearing VOC[2:0] to "000". In order to activate voice output again when the system returns and enter into normal mode, the related bits of VOC register need to be set again.



When the DAC is used as sound generator, the bias & filter circuit is used for bias voltage setting and waveform filter regulation and the DAC is output to the VO (Voice Output) pin and please see application notes for detailed calculation example and application. The driving capability of DAC is shown below.

	Condition	Min.	Typ.	Max.	Unit
VO/DAO	V_{DD}=3V;VO=0~2V;Data=7Fh	2.5	3		mA



The **VOC** is a three bit voice control register in the 7-bit mode.

VOC	address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	0x13	-	-	-	-	-	PWM	DAC	OP
Reset	-	-	-	-	-	-	0	0	0
PWM: '1' PWM output enabled; '0' PWM output disabled. DAC: '1' DAC enabled; '0' DAC disabled. OP: '1' DAC uses DAO pin as output pin; '0' DAC uses VO pin as output pin.									

17. Low Voltage Detection/Reset

The low voltage detection is used to detect low battery or low power condition. There are 4 options on the detection level selectable by mask option MO_DLVL. The low voltage detection circuit can be turned off by clearing LVDE bit, and the status of supply power can be read out at bit LVDO of LVDC register (extension register 0x17h).

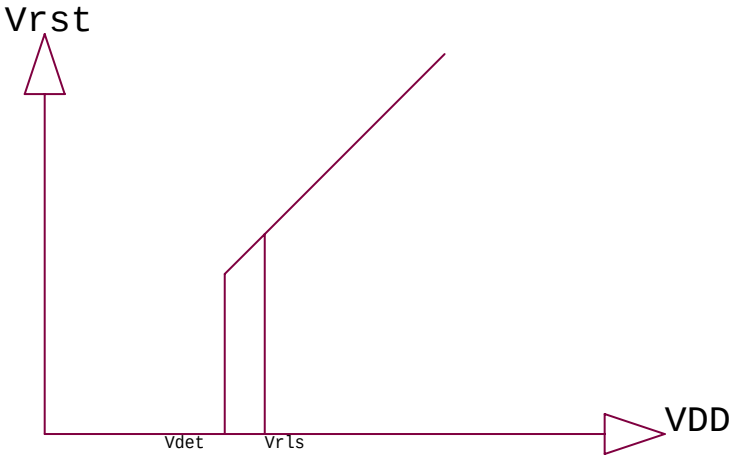
MO_DLVL	Detection voltage
00	2.4 volts
01	2.6 volts
10	2.8 volts
11	3.0 volts

LVDC	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	LVDO	-	-	-	-	-	-	LVDE
Mode	R	-	-	-	-	-	-	W
Reset	-	-	-	-	-	-	-	0
LVDO: '0' → Battery level low; '1' → Battery level high LVDE: '0' → Disable voltage Detection; '1' → Enable voltage Detection								

Low voltage reset circuit prevents the CPU from operating below its physical limit. When the supply voltage drops below V_{DET} (2.2Volt), the CPU will be held in reset state until the supply voltage rises to V_{RLS}. Then CPU will be released from reset state. V_{RLS} will be higher than V_{DET} by 5% to provide hysteresis and prevent CPU from bouncing back and forth between reset and operating state. The low voltage reset function can be enabled or disabled by mask option MO_LVRE.

MO_LVRE	Function
0	Disable LVR
1	Enable LVR

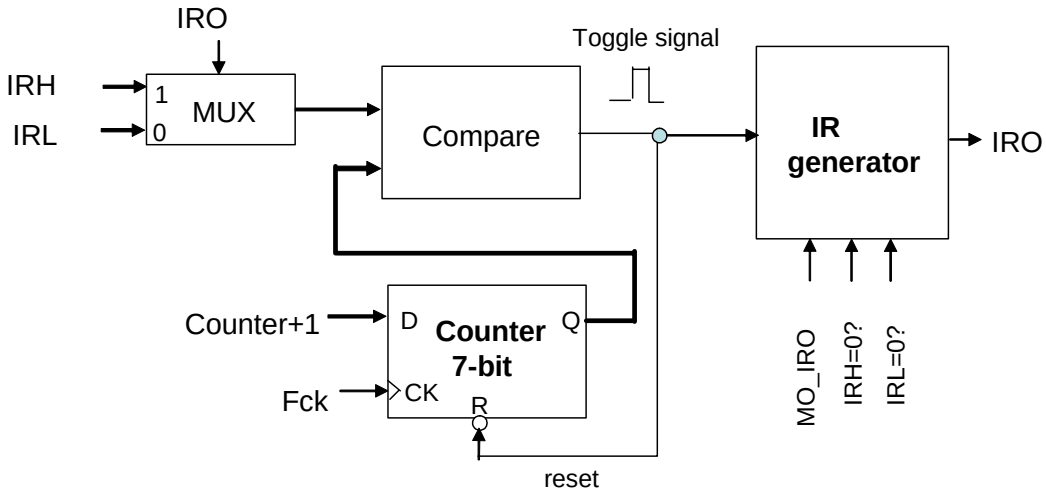
The voltage detection circuit is temperature compensated to prevent the detection voltage from drifting with temperature variation.



18. Infrared output

To achieve an IR output with programmable frequency and duty cycle, two 7-bit registers are employed here. The IRH register represents the period (on FCK clock number) of output high, while IRL register represents the period of output low. With this mechanism, the output IR frequency is equal to FCK/(IRH+IRL), and the high duty cycle ratio is equal to IRH/(IRH+IRL). To make the IRO as output pin alone, either IRH or IRL can be set as 0. When IRH is 0, the IRO output is a DC low. On the contrary, if IRL is 0, the output is a DC high. Special care in hardware implementation is also taken according to the MO_IRO (mask option to determine the default state of the IRO) to avoid glitch when PWM output is disabled.

IRO



To avoid unexpected IR output, users should firstly load the content of IRH and IRL before turn on IR by set IROE bits to '1'.

The access of all the registers of IR is through the extension register. They are list as below:

Extension register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Mode	Reset value
0x15h	IRL*	IROE	IR PWM LOW DURATION							R/W	0xxx xxxx
0x16h	IRH	-	IR PWM HIGH DURATION							W	-xxx xxxx

* IRL[7] is read/write, and IRL[6..0] is write only.

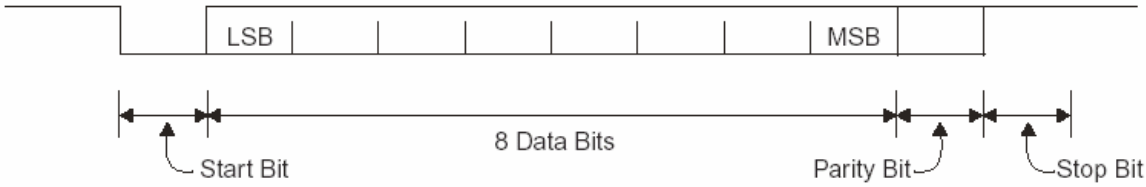
IROE: '0' → IR is disabled (default); '1' → IR is enabled.

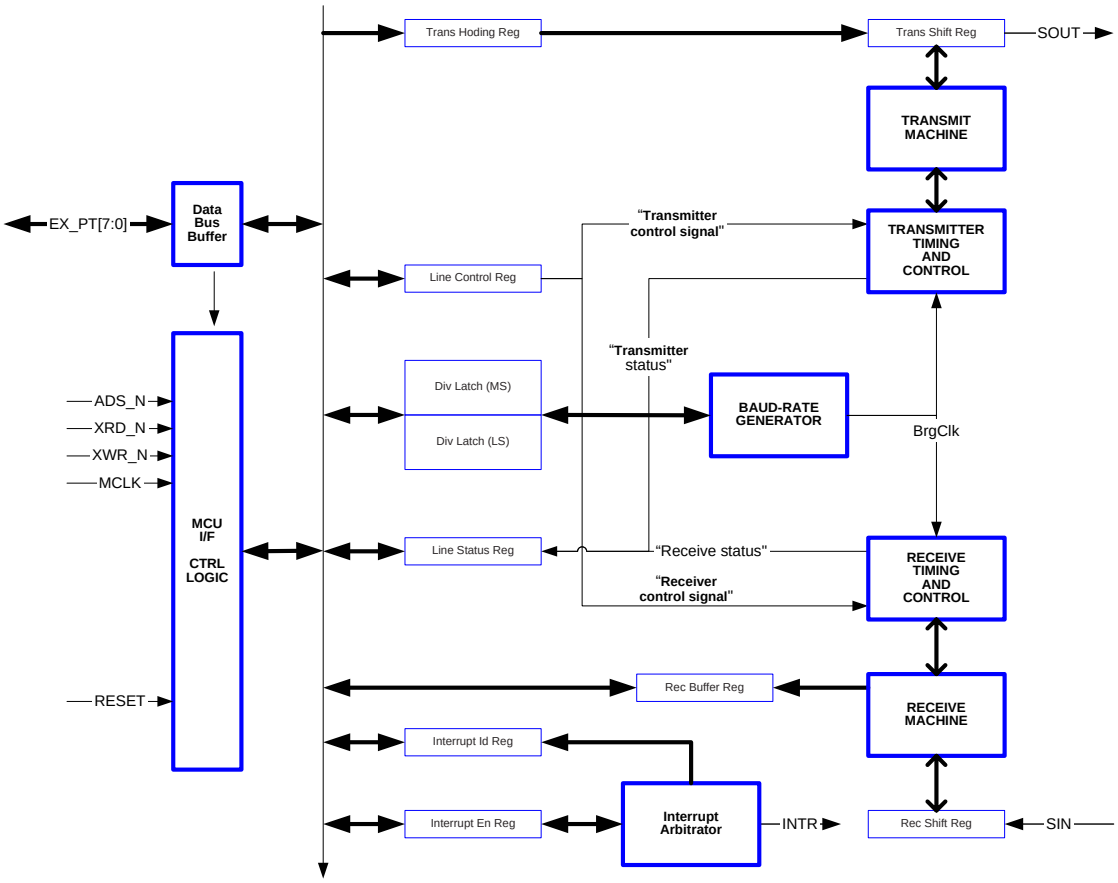
19. Universal Asynchronous Receiver/Transmitter

The UART (Universal Asynchronous Receiver/Transmitter) interface provides serial communication capabilities with other devices such as PC. Features include:

- ✓ Full duplex Asynchronous communication
- ✓ Programmable transmission rate with internal baud rate generator with selectable bit rates
- ✓ Double buffered Transmitter and Receiver.
- ✓ Programmable Data length (from 5 to 8 bits)
- ✓ Programmable stop bits (1, 1.5 or 2-stop bit) generation and detection
- ✓ Programmable parity type (odd, even or no parity)
- ✓ Error (parity, overrun and framing errors) detection
- ✓ Fully prioritized interrupt system control
- ✓ Line break generation and detection.

Example – 8-bit UART Frame Format: (1 Start Bit, 8 Data Bits, 1 Parity Bit, 1 Stop Bit)





19.1. Interface Registers

Addressable extension register used to interface with MCU

Address	Name	Function								Mode	RESET
00H	RBR	UART RECEIVER BUFFER								R	0000 0000
01H	THR	UART TRANSMITTER HOLDING REGISTER								R/W	0000 0000
02H	IEIR	0	RLSI	THRI	RBRI	0	ID2	ID1	ID0	R/W	0000 0000
03H	LCR	BRGE	SB	SP	EPS	PEN	STB	WLS1	WLS0	R/W	0000 0000
04H	BRL	UART LSB of Baud Rate Register								R/W	0000 0000
05H	BRH	UART MSB of Baud Rate Register								R/W	0000 0000
06H	LSR	0	TEMT	THRE	BI	FE	PE	OE	DR	R	0110 0000

IEIR: Interrupt enable/disable identification register.

LCR: Line control register.

LSR: Line status register.

19.2.Baud Rate Configuration Register

The BRH and BRL registers hold the upper and lower bytes of 16 bit baud rate divisor and which are readable/writable. The baud rate of UART is calculated as following:

$$BAUD\_RATE\_DIVISOR = \frac{FCK}{16 * BAUD\_RATE}, (FCK: fast\ clock\ of\ system)$$

The contents of BRH and BRL are calculated by the following two formulas:

$$BRL = BAUD\_RATE\_DIVISOR \ \% 256$$

$$BRH = (BAUD\_RATE\_DIVISOR - BRL) / 256$$

The "%" symbol is the modulus operation (reminder of division). For example, if the FCK is 1.8432M Hz and the desired baud rate is 2400 baud, then

$$BAUD\_RATE\_DIVISOR = \frac{1843200}{16 * 2400} = 48$$

The BRL register shall be set to 0x30 and BRH set to 0x00. The setting of baud_rate_divisor is not updated until the BRH register is written. Thus user is strongly recommended to write BRL first, then BRH.

In order to obtain good communication quality, the same time base shall be used in the both sides of transmitting and receiving. The following table shows the most common baud rate setting used in the PC UART communication.

BRL and BRH: Baud Rate Control Registers

FCK(Hz)	Baud Rate (bps)	Divisor	BRL	BRH
1.8432M	50	2304	0x00	0x09
1.8432M	300	384	0x80	0x01
1.8432M	1200	96	0x60	0x00
1.8432M	2400	48	0x30	0x00
1.8432M	4800	24	0x18	0x00
1.8432M	9600	12	0x0C	0x00
1.8432M	19200	6	0x06	0x00
1.8432M	38400	3	0x03	0x00
1.8432M	57600	2	0x02	0x00
1.8432M	115200	1	0x01	0x00

19.3. Interrupt & Identification Register

This high nibble of IEIR register allows to enable/disable interrupt generation by the UART, the low nibble ID[2..0] of IEIR register is used to identify the source of interrupts.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
0x02h	**IEIR**	0	RLSI	THRI	RBRI	0	ID2	ID1	ID0	"0000_0000"
		-	R/W	R/W	R/W	-	R	R	R	

RBRI: Receiver Buffer Register Interrupt (1 = Enable, 0 = Disable), related to ID[1] bit.
THRI: Transmitter Hold Register Interrupt (1 = Enable, 0 = Disable), related to ID[0] bit.
RLSI: Receiver Line Status Interrupt (1 = Enable, 0 = Disable), related to ID[2] bit.

The following table shows the related interrupt sources, user can read the ID[2:0] to retrieve what is the current highest priority of pending interrupts. The ID[2:0] bits will be cleared when user read the related registers. For example, when an interrupt happened and the content of ID[2:0] is "101", this means that LRS error and THR empty happen; user can read the LSR register to clear the ID[2] bit and ID[0] bit can also be cleared by reading the IEIR or writing data into THR register.

Level	IEIR Bit [2:0]	Source of Interrupt	Interrupt Reset Control
None	0 0 0	None	None
Highest	1 0 0	LSR error flags (OE/PE/FE/BI)	Reading LSR register to clear ID[2]
Second	0 1 0	LSR receiver data ready flag (DR)	Reading RBR register to clear ID[1]
Third	0 0 1	LSR flag THR Empty (THRE)	Reading IEIR register or Writing THR register to clear ID[0]

19.4.Line Control Register

The line control register allows user to configure the asynchronous data transfer format and set the UART function. Reading from the register is allowed to check the current settings of the communication.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRGE	SB	SP	EPS	PEN	STB	WLS1	WLS0

Name	Description
WLS[1..0]	**Word Length Select** "00": word length = 5 "01": word length = 6 "10": word length = 7 "11": word length = 8
STB	**Stop Bit Length** '0': Stop bit length = 1 '1': Stop bit length = 1.5 when WLS[1..0]="00" '1' Stop bit length = 2 when WLS[1..0]="01","10","11"
[SP, EPS, PEN]	**Parity Selection** "xx0": No Parity "001": odd Parity "011": even Parity "101": Stick Parity 1 "111": Stick parity 0
SB	**Set Break** When enable the break control bit causes a break condition to be transmitted (SOUT is forced to a logic 0 state). This condition exists until disabled by resetting this bit to logic 0. '0': disable break; '1': enable break
BRGE	**Baud Rate Generator** '0': disable baud rate clock generator '1': enable baud rate clock generator

19.5.Line Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TEMT	THRE	BI	FE	PE	OE	DR

Name	Description
DR	**Receiver Data Ready** DR indicates status of RBR. It will be set to logic 1 when RBR data is valid and will be reset to logic 0 when RBR is empty. When line errors (OE/PE/FE/BI) happen, DR will also be set to logic 1 and RBR will be updated to reflect the Data bits portion of the frame.
OE	**Overrun Error** This bit will be set when the next character is transferred into RBR before the previous RBR data is read by the CPU. Even though DR will still be 1 when OE is set to logic 1, the previous frame data stored in RBR which is not read by the CPU is trashed and can‘t be recovered.
PE	**Parity Error** This bit will be set to logic 1 only when the Parity is enabled and the Parity bit is not at the logic state it should be. For Even Parity, the Parity bit should be 1 if an odd number of 1s in the Data bits is received; otherwise, the Parity bit should be 0. For Odd Parity, the Parity bit should be 1 if an even number of 1s in the Data bits is received; otherwise, the Parity bit should be 0. For Stick Parity '1', the Parity bit should be 1. For Stick Parity '0', the Parity bit should be 0.
FE	**Framing Error** FE will be reset to logic 0 whenever SIN is sampled high at the center of the first Stop bit, regardless of how many Stop bits the UART is configured to.
BI	**Break Interrupt** BI will be set to logic 1 whenever SIN is low for longer than the whole frame (the time of Start bit + Data bits + Parity bit + Stop bits), not at the SIN rising edge where Break is negated. If SIN is still low after BI is reset to logic 0 by reading LSR, BI will not be set to logic 1 again. Since Break is also a Framing error, FE will also be set to 1 when BI is set.
THRE	**THR Empty** THRE will be set to logic 1 whenever THR is empty which indicates that the transmitter is ready to accept new data to transmit.
TEMT	**Both THR and TSR are Empty** This bit will be set to logic 1 when THRE is set to 1 and the last Data bit in the TSR is shifted out through SOUT.

* The four error flags (OE, PE, FE and BI) of LSR will be reset to logic 0 after a LSR read.

Since the SIN and SOUT of UART pins are shared with PRTD[1..0], users can use the mask option to enable the UART function and select PRTD[1..0] function.

MO_UART	0	PRTD[1:0] = I/O Pin
	1	PRTD[1:0] = UART Pin

20. Extension Register Access

The extension registers can be accessed through the extension port control registers EXTAS and EXTDA. User can read/write the extension register easily and the control timing is generated by hardware automatically. The following code shows how to access the extension registers.

Read Extension Register:

```
LDA     #0x00h   ; load #0x00h data to A Register
STA     EXTAS    ; store A register data to the extension port address register.
LDA     EXTDA    ; store the extension register (0x00h) data to A Register.
```

Write Extension Register:

```
LDA     #0x03h   ; load #0x03h data to A Register
STA     EXTAS    ; store A register data to the extension port address register.
LDA     #0x18h   ; load #0x18h data to A Register
STA     EXTDA    ; store A register data to the extension port data register.
```

21. Summary of Registers and Mask Options

All the registers and mask options used in this chip are listed in the following tables.

Address	NAME	Field								Mode	RESET
00H	**TPL**	Table pointer low byte								R/W	xxxx xxxx
01H	**TPH**	Table pointer high byte								R/W	xxxx xxxx
02H	**IER**	-	-	INT_EX	TB	INT1	T1	T2	INT2	R/W	--00 0000
03H	**T1L**	Timer 1 low byte								W	xxxx xxxx
04H	**T1H**	Timer 1 high byte								W	xxxx xxxx
05H	**T2L**	Timer 2 low byte								W	xxxx xxxx
06H	**T2H**	Timer 2 high byte								W	xxxx xxxx
07H	**SP**	stack pointer								R/W	1111 1111
08H	**DP**	data RAM pointer								R/W	xxxx xxxx
09H	**OP1**	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C	R/W	1000 00xx
0AH	**OP2**	IDLE	PNWK	TCWK	TBE	TBS[3..0]				R/W	0xx- ----
0BH	**PP**	RAM page pointer								R/W	0000 0000
0CH	**PRTC**	I/O port C								R/W	1111 1111
0DH	**PRTD**	I/O port D								R/W	1111 1111
0EH	**PWMC***	PWM data								W	0000 0000
0FH	**LCDC**	-	-	CLR_GP	GRAY			BLANK	LCDE	W	xx1x xx10
10H	**PRT10**	I/O port 10								R/W	1111 1111
11H	PRT11	**Reserved**								R/W	xxxx xxxx
12H	DTMF	**Reserved**								R/W	xxxx xxxx
13H	**VOC***	-	PWM O/P driver			PWME	PWM	DAC	OP	W	x000 0000
14H	PRT14	**Reserved**								R/W	xxxx xxxx
15H	**PRT15**	I/O port 15								R/W	---- --11
16H	**TPP**	ROM table page pointer								R/W	0000 0000

Address	NAME	Field	Mode	RESET
17H	**PRT17**	I/O port 17	R/W	1111 1111
18~1FH		**Reserved**	R/W	xxxx xxxx
20H	**EXTAS**	Extension port address register	R/W	xxxx xxxx
21H	**EXTDA**	Extension port data register	R/W	xxxx xxxx
22~2AH		**Reserved**	R/W	xxxx xxxx
2BH	**GRAY16**	32 to 16 Gray Level Palette Register	w	
	GRAY0	Gray level 0 mapping register	W	xxx0 0000
	GRAY1	Gray level 1 mapping register	W	xxx0 0010
	GRAY2	Gray level 2 mapping register	W	xxx0 0100
	GRAY3	Gray level 3 mapping register	W	xxx0 0110
	GRAY4	Gray level 4 mapping register	W	xxx0 1000
	GRAY5	Gray level 5 mapping register	W	xxx0 1010
	GRAY6	Gray level 6 mapping register	W	xxx0 1100
	GRAY7	Gray level 7 mapping register	W	xxx0 1110
	GRAY8	Gray level 8 mapping register	W	xxx1 0000
	GRAY9	Gray level 9 mapping register	W	xxx1 0010
	GRAYA	Gray level A mapping register	W	xxx1 0100
	GRAYB	Gray level B mapping register	W	xxx1 0110
	GRAYC	Gray level C mapping register	W	xxx1 1000
	GRAYD	Gray level D mapping register	W	xxx1 1010
	GRAYE	Gray level E mapping register	W	xxx1 1100
	GRAYF	Gray level F mapping register	W	xxx1 1110
2CH	**PSA1**	Physical page address mapping register for logical page 1	R/W	0000 0001
2DH	**PSA2**	Physical page address mapping register for logical page 2	R/W	0000 0010
2EH	**PSA3**	Physical page address mapping register for logical page 3	R/W	0000 0011
2FH~3FH		**Reserved**	R/W	xxxx xxxx

* The definitions of PWMC and VOC are different for 7-bit and 8-bit voice output. Please refer to voice output section for the detailed description.

Extension registers:

Address	Name	Function								Mode	RESET
00H	**RBR**	UART RECEIVER BUFFER								R	0000 0000
01H	**THR**	UART TRANSMITTER HOLDING REGISTER								R/W	0000 0000
02H	**IEIR**	0	RLSI	THRI	RBRI	0	ID2	ID1	ID0	R/W	0000 0000
03H	**LCR**	BRGE	SB	SP	EPS	PEN	STB	WLS1	WLS0	R/W	0000 0000
04H	**BRL**	UART LSB of Baud Rate Register								R/W	0000 0000
05H	**BRH**	UART MSB of Baud Rate Register								R/W	0000 0000
06H	**LSR**	0	TEMT	THRE	BI	FE	PE	OE	DR	R	0110 0000
15H	**IRL**	IROE	IR PWM LOW DURATION							R/W	0xxx xxxx
16H	**IRH**	-	IR PWM HIGH DURATION							W	-xxx xxxx
17H	**LVDC**	LVDO	-	-	-	-	-	-	LVDE	R/W	x--- ---0

Mask Options:

NAME	VALUE	NOTE
MO_LVRE	0	low voltage reset disable
	1	low voltage reset enable
MO_FXTAL	0	R/C oscillator For fast clock
	1	Crystal oscillator For fast clock
MO_SXTAL	0	R/C oscillator For 32k clock
	1	Crystal oscillator For 32k clock
MO_FCK/SCKN	00	slow clock only
	01	illegal

NAME	VALUE	NOTE
	10	dual clock
	11	fast clock only
MO_WDTE	0	WDT disable
	1	WDT enable
MO_CPP[7:0]	0	open-drain output
	1	push-pull output
MO_DPP[7:0]	0	open-drain output
	1	push-pull output
MO_10PP[7:0]	0	open-drain output
	1	push-pull output
MO_15PP[1:0]	0	open-drain output
	1	push-pull output
MO_17PP[7:0]	0	open-drain output
	1	push-pull output
MO_LIO15[1:0]	0	IO pin
	1	LCD pin
MO_LIO17[7:0]	0	IO pin
	1	LCD pin
MO_COM[1:0]	Fixed to "00"	
MO_LBSR[2:0]	000	1/7 bias
	001	1/7.5 bias
	010	1/8 bias
	011	1/8.5 bias
	100	1/9 bias
	101	1/9.5 bias
	110	1/10 bias
	111	**1/5 bias**
MO_RCAP[2:0]	000	Ring-osc internal cap. Select C=2P
	001	Ring-osc internal cap. Select C=4P
	010	Ring-osc internal cap. Select C=7P
	011	Ring-osc internal cap. Select C=14P
	100	Ring-osc internal cap. Select C=20P
	101	Ring-osc internal cap. Select C=40P
	110	Ring-osc internal cap. Select C=50P
	111	Ring-osc internal cap. Select C=60P
MO_8BVOC	0	7-bit DAC/PWM output
	1	8-bit DAC/PWM output
MO_GRAY_MODE[1:0]	00	16 Gray Level
	01	4 Gray Level
	10	2 Level(B/W)
	11	2 Level(B/W)
MO_EXMEM	Fixed to "0"	
MO_DLVL[1:0]	00	LVD level voltage detect is 2.4V
	01	LVD level voltage detect is 2.6V
	10	LVD level voltage detect is 2.8V
	11	LVD level voltage detect is 3.0V
MO_IRO	0	Default State of the IRO is '0'
	1	Default State of the IRO is '1'
MO_PMODE[1:0]	Fixed to "00"	
MO_UART	0	PRTD[1:0] = I/O Pin
	1	PRTD[1:0] = UART Pin
MO_PSMODE[1:0]	00	**Internal Mode(**
	01	**Internal CP+External R String and Opamps**
	10	**External CP+Internal R String and Opamps**

NAME	VALUE	NOTE
	11	**External CP+External R String and Opamps**

22. Absolute Maximum Rating

Item	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.5V ~ 4.0V	
Input Voltage	V_{IN}	-0.5V ~ V_{DD}+0.5V	
Output Voltage	V_O	-0.5V ~ V_{DD}+0.5V	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

23. Recommended Operating Conditions

Item	Symbol	Rating	Condition
Supply Voltage	V_{DD}	2.4V ~ 3.6V	
Input Voltage	V_{IH}	0.9 V_{DD} ~ V_{DD}	
	V_{IL}	0.0V ~ 0.1V_{DD}	
Operating Frequency	$F_{MAX.}$	8M Hz	V_{DD} =3.0V
		6M Hz	V_{DD} =2.4V
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

24. AC/DC Characteristics

Testing Condition : TEMP=25℃, VDD=3V±10%

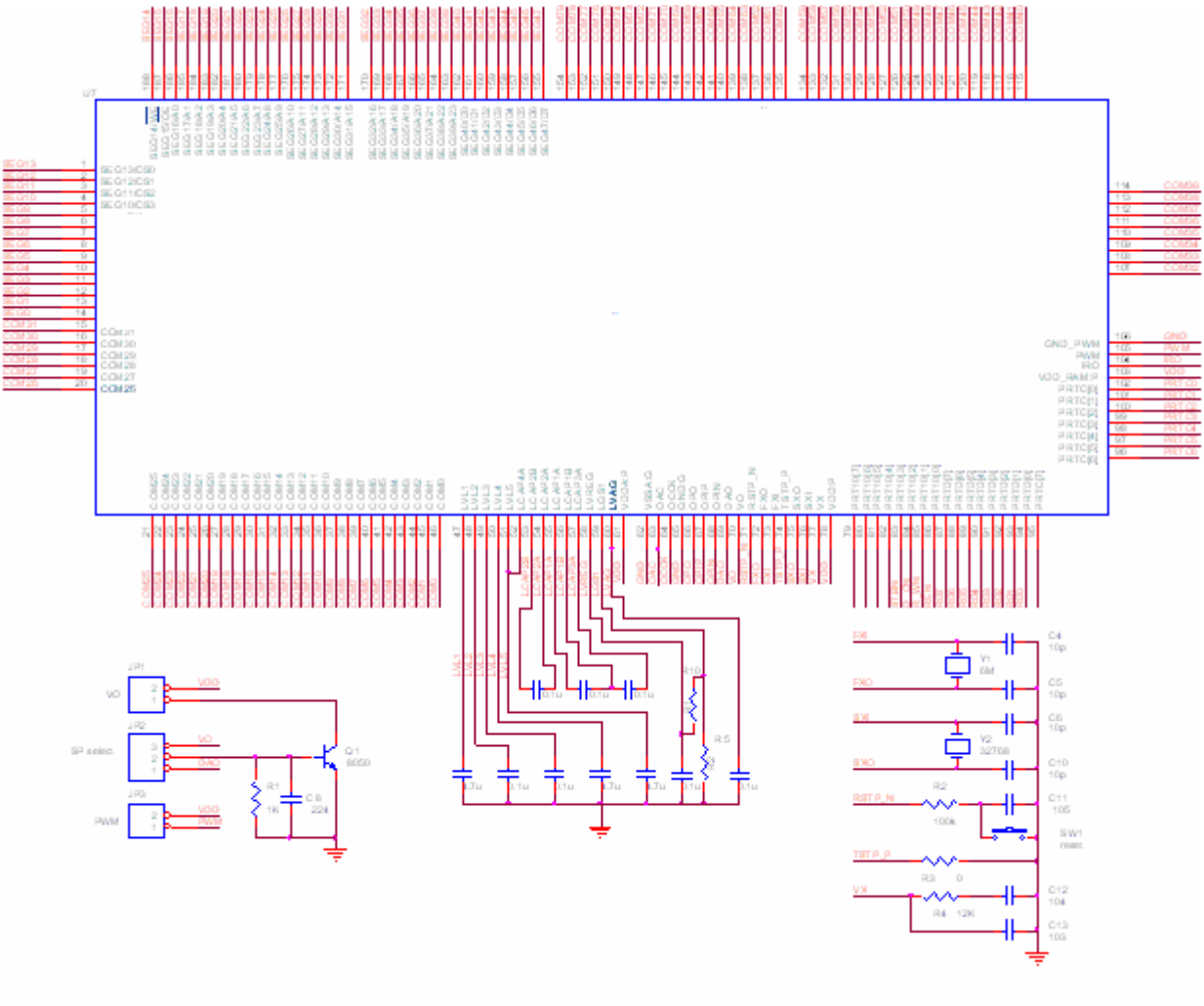
Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Power consumption						
NORMAL Mode Current	I_{FAST}		1	1.5	mA	2M external R/C fast clock
SLOW Mode Current	I_{SLOW}		15	25	µA	32768 Hz slow clock with LCD disabled
IDLE Mode Current	I_{IDLE}		10	20	µA	32768 Hz slow clock with LCD disabled
Sleep Mode Current	I_{SLEEP}			1	µA	
Additional Current if LCD ON	I_{LCD}		200	220	µA	LV5=3xLVREG
			250	275		LV5=4xLVREG
			300	330		LV5=5xLVREG
I/O specification						
Input High Voltage	V_{IH}	0.8			V_{DD}	Input Pins
Input Low Voltage	V_{IL}			0.2	V_{DD}	Input Pins
Input Hysteresis Width	V_{HYS}		1/3		V_{DD}	I/O, RSTP_N Threshold = 2/3 VDD (Input from low to high), Threshold = 1/3 VDD (Input from high to low)
Output Source Current	I_{OH}	50			µA	Output drive high[*1], V_{OH}=2.0V
Output Sink Current	I_{OL1}	1.0			mA	Output drive low, V_{OL}=0.4V
Input Low Current	I_{IL1}		20		µA	RSTP_N, V_{IL} = GND, Pull high Internally
Input Low Current	I_{IL2}		100		µA	I/O, V_{IL}=GND, if pull high Internally by user
PWM and DAC						

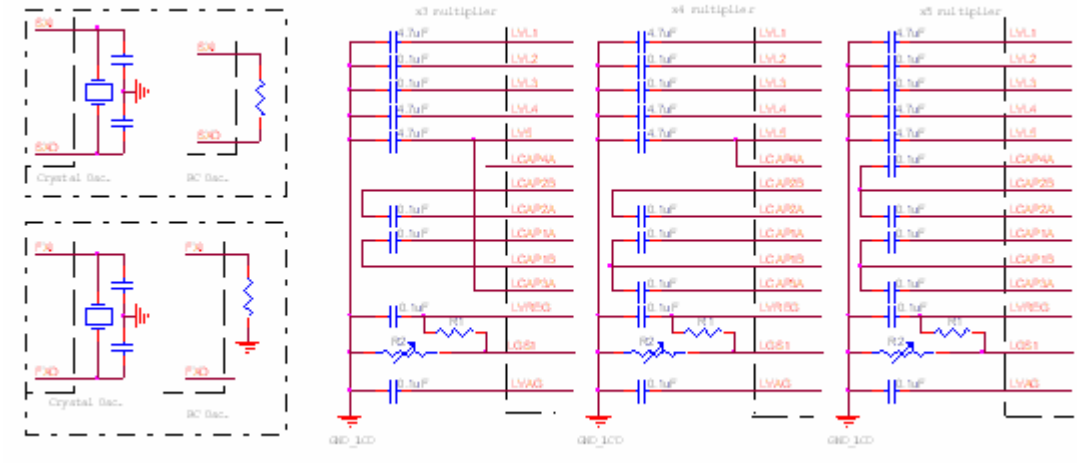
PWM Output Current	I_{PWM}	10	14		mA	PWM *2 With 32Ω Loading
		6	8		mA	With 64Ω Loading
		4	5		mA	With 100Ω Loading
DAC Output Current	I_{oVO}	2.5	3		mA	VO, DAO@ V_{DD}=3V,VO=0~2V, Data =FF
Low voltage Reset						
LVR detection voltage	V_{DET}		2.2		Volts	
LVR release voltage	V_{RLS}		2.31		Volts	

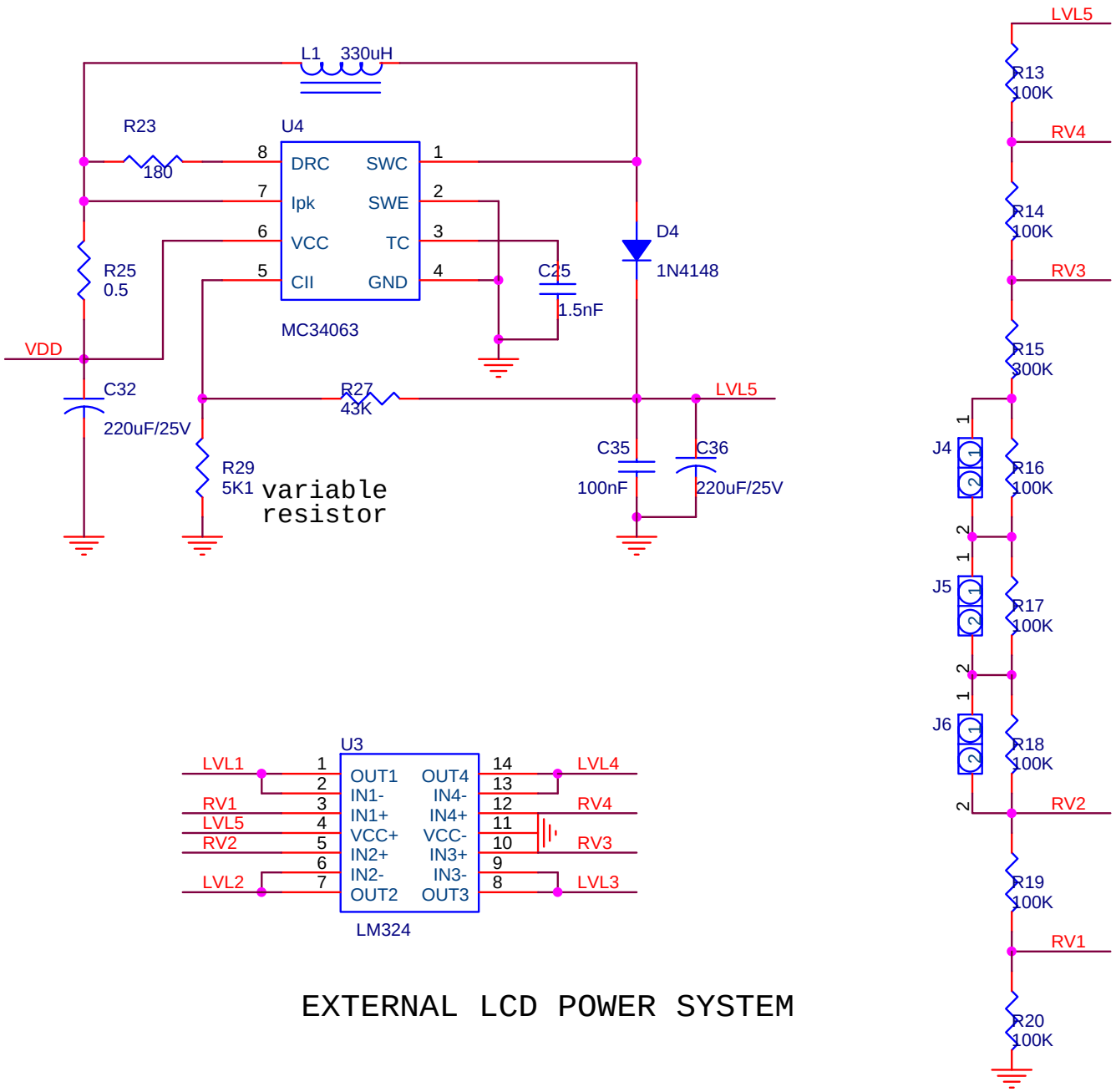
Notes:

1. The "Output Source Current" specification is applicable only to the Push-Pull I/O type.
2. This Specification indicates only one PWM driving capability, and there are totally five built-in drivers, user can multiply the actual number of driver to get the total amount of current. (I_{PWM} x N; N=0, 1, 2, 3, 4, 5)

25. Application Circuit







EXTERNAL LCD POWER SYSTEM

26. Important Note

1. Please note the ICE is a superset of HE80004 series IC. Each member of the family only has parts of all resources. Do not use any hardware resource that your target chip doesn't have, for example, RAM and register. KBIDS and compiler can't prevent user from using some hardware resources that don't exist in your target chip.
2. To access "Data ROM", users must update TPP first, TPH, and then TPL. Only follow this order, the pre-charge circuit of ROM will work correctly. The 5μs waiting is also necessary before LDV instruction is executed since Data ROM is a low speed ROM. User can't emulate this accessing process in ICE, so 5μs delay should be added by firmware.
3. LCD driving circuit must be turned off before the system goes into sleep mode.
4. Please bond the TSTP_P, RSTP_N and PRTD [7:0] with test points on PCB (can be soldered and probed) as you can, then some testing can be performed on PCB when it's necessary. The TSTP_P is suggested to connect to ground by a 0 ohm resistor.
5. The LV5 must be lower than 8.5 volts; otherwise permanent damages to the IC might be incurred.
6. ***The LCD voltage adjustment mechanism shall be reserved for LV5 voltage fine-tunes; since it's possible there is some variation in LV5 voltage due to IC manufacture process variation. User can use variable-resistor to adjust the LV5 voltage or use some tools to detect the LV5 and then select a proper resistor. Please refer to application note AN025 for the detailed description.***

27. Updated History

Version	Date	Update History
V0.92	2005/1/17	New Created. HE84G752 -> HE84G752B
V0.93	2005/1/21	Errata Correct