AT209S PCI Arbiter and Clock Buffer

■ General Description

The AT209S is an integrated device that contains a PCI Arbiter and a Clock Buffer. PCI Arbiter extends system PCI devices without piecing other circuit to simplify design complexity and increase systems stability.

PCI Arbiter also provides STOP# input pin with that extended PCI devices instruct the master to prematurely end the transaction on the current data phase same as one in PCI specification.

Clock Buffer is a high performance and low jitter zero delay buffer that provides synchronization between the input and output. The synchronization is established via CLKO feed back to the input of a build-in PLL.

PCICLKI is the clock input of the Clock Buffer. In the absence of PCICLKI input, will be in the power down mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

■ Features

- PCI Arbiter

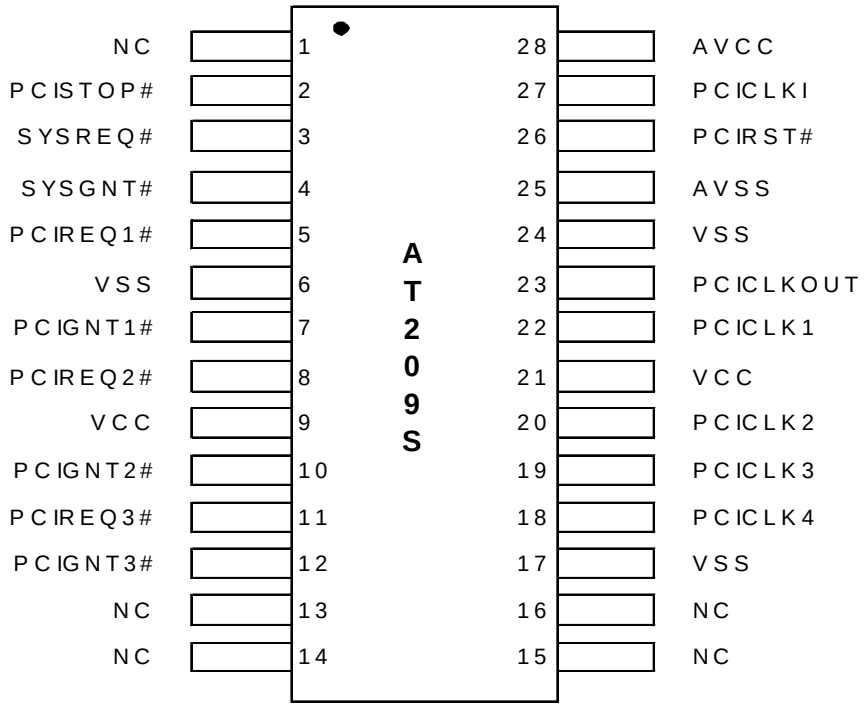
  Extend PCI Devices from One to Three
- PCI Clock Frequency

  Support PCI Clock range from 25MHz to 66MHz
- Zero delay buffer

  Generate four zero delay clock sources

  Support frequency range from 25MHz to 66MHz
- All AME's Lead Free Products Meet RoHS Standards

■ Pin Configuration



※ Ordering Information

AT209S- Commercial Standard

AT209SG- Green Device with Commercial Standard

■ Pin Description

I/O Type	Function
IN	Input Pin
OUT	Output Pin
PWR	Power Pin

Pin No.	Pin Name	I/O Type	Function
26	PCIRST#	IN	PCI bus reset#
2	PCISTOP#	IN	PCI bus stop# (Internal 47K pull-up resistor)
3	SYSREQ#	OUT	Request signal to chipset
4	SYSGNT#	IN	Grant signal from chipset (Internal 47K pull-up resistor)
5	PCIREQ1#	IN	Request signal from PCI bus (Internal 47K pull-up resistor)
7	PCIGNT1#	OUT	Grant signal to PCI bus
8	PCIREQ2#	IN	Request signal from PCI bus (Internal 47K pull-up resistor)
10	PCIGNT2#	OUT	Grant signal to PCI bus
11	PCIREQ3#	IN	Request signal from PCI bus (Internal 47K pull-up resistor)
12	PCIGNT3#	OUT	Grant signal to PCI bus

Table 1. PCI Arbiter FSM Group Signal, Power; Vcc3V (3.3V)

■ Pin Description

Pin No.	Pin Name	I/O Type	Function
18	PCICLK4	OUT	PCICLK output
19	PCICLK3	OUT	PCICLK output
20	PCICLK2	OUT	PCICLK output
22	PCICLK1	OUT	PCICLK output
23	PCICLKOUT	OUT	PLL feedback and Internal feedback on this pin
27	PCICLKI	IN	PCLCLK input reference frequency

Table 2. Clock Buffer Group Signal ---- Power: Vcc23 (2.5V or 3.3V)

Pin No.	Pin Name	I/O Type	Function
6	VSS	PWR	Ground
9	VCC	PWR	3.3V Power
17	VSS	PWR	Ground
21	VCC	PWR	3.3V Power
24	VSS	PWR	Ground
25	AVSS	PWR	Ground for PLL
28	AVCC	PWR	3.3V Power for PLL

Table 3. Power Signal

■ Quick Reference Data

GND = 0V; VCC = 3.3V; 0°C < Temp < 85°C

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
VCC	Power pin		3.15	3.3	3.45	V
VSS	Ground pin			0		V
AVCC	Power pin for PLL		3.15	3.3	3.45	V
AVSS	Ground pin for PLL			0		V

Table 4. Power/Ground Pin

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
Vil	Input low voltage				0.8	V
Vih	Input high voltage		2			V
Vol	Output low voltage	Iol=30mA; VCC3V=3.3V			0.4	V
Voh	Output high voltage	Ioh=30mA; VCC3V=3.3V	2.4			V
Duty1	Output duty cycle (0.5*VCC as a reference)	Input duty cycle=50%	45		55	%
Tr	Output rise time	Measure between 0.8v and 2V, CL=30P			2	nS
Tf	Output fall time	Measure between 0.8v and 2V, CL=30P			2	nS
Tpd	Propagation delay time	Measure at 0.5*Vin & Vout, CL=30P		250		nS
PCICLKI	Buffer input frequency		25M		50M	Hz

Table 5. Clock Buffer Block

■ Quick Reference Data

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
Vil	Input low voltage				0.8	V
Vih	Input high voltage		2.0			V
Vol	Output low voltage				0.4	V
Voh	Output high voltage		2.4			nS
Tdcko	Output delay from PCICLK rising edge to output valid			8	10	nS

Table 6. PCI Arbiter FSM

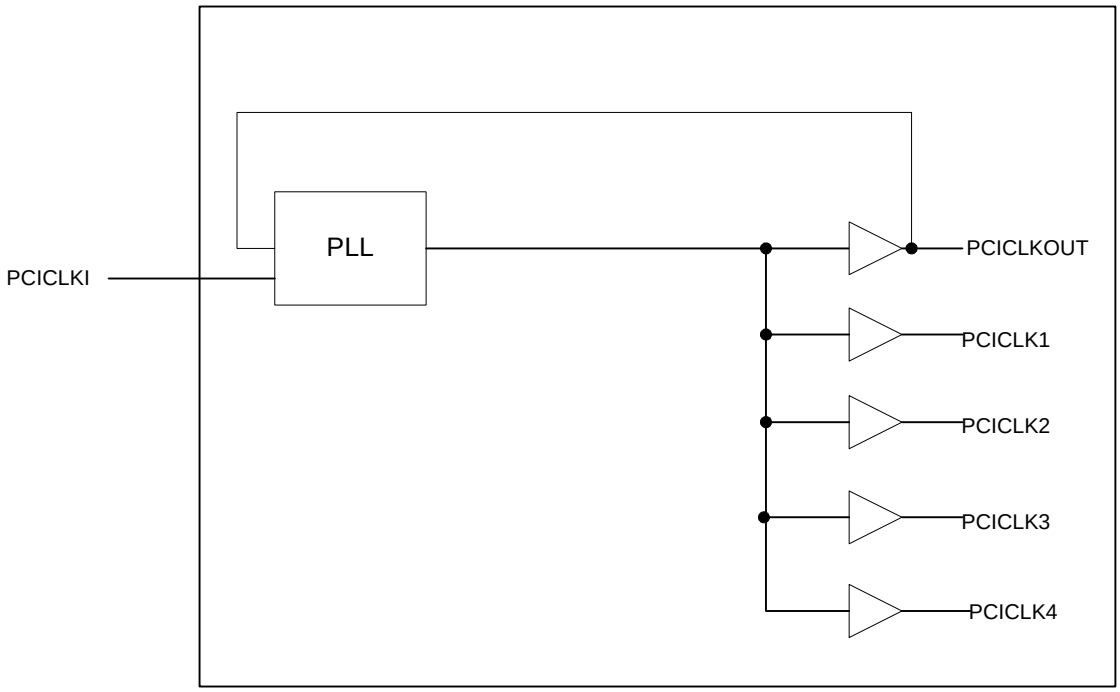


Figure 2. Clock Buffer Block Diagram

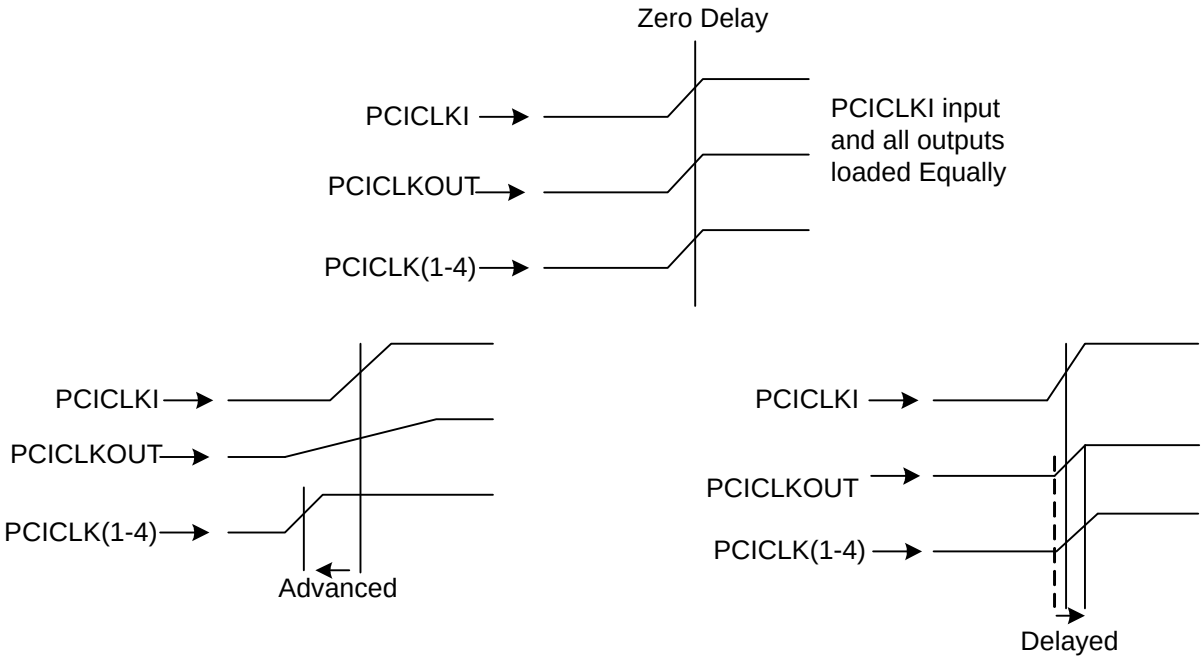
Output-to-Output Skew

Since the PCICLKOUT and the PCICLK(1-4) outputs are identical, they all start at the same time, but different loads cause them to have different rise times and different times crossing the measurement thresholds.

If all outputs are equally loaded, zero phase difference will maintained from PCICLKI to all outputs.

If applications requiring zero output-output skew, all the outputs must equally loaded.

If the PCICLK(1-4) outputs are less loaded than PCICLKOUT, PCICLK(1-4) outputs will lead it; and if the PCICLK(1-4) is more loaded than PCICLKOUT, PCICLK(1-4) will lag the PCICLKOUT.



PCICLKI input and PCICLK(1-4) outputs loaded equally, with PCICLKOUT loaded More.

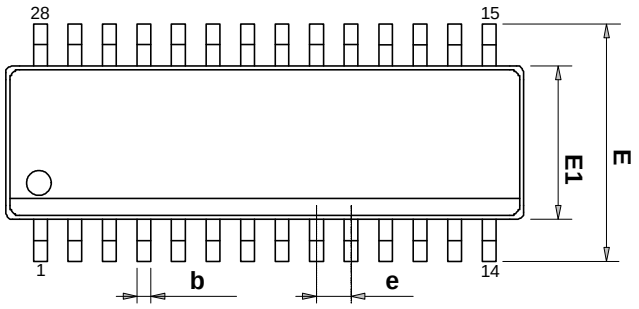
PCICLKI input and PCICLK(1-4) outputs loaded equally, with PCICLKOUT loaded Less.

Figure 3. Timing diagrams with different loading configurations

■ Package Dimension

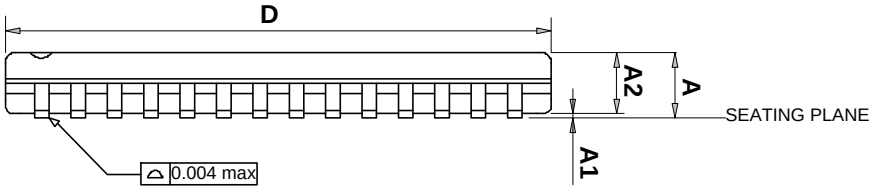
SSOP-28

TOP VIEW

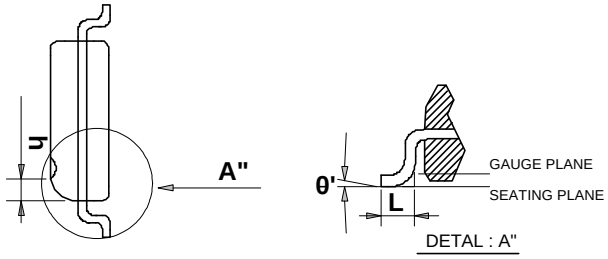


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	-	1.50	-	0.059
b	0.20	0.30	0.008	0.012
D	9.80	10.00	0.386	0.394
E1	3.81	4.00	0.150	0.157
e	0.635BASIC		0.025BASIC	
E	5.80	6.20	0.228	0.244
h	0.380BASIC		0.015BASIC	
L	0.41	1.27	0.016	0.500
q	0°	8°	0°	8°

FRONT VIEW



SIDE VIEW



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