# AKD4633-A
## AK4633 Evaluation board Rev.3

## GENERAL DESCRIPTION

AKD4633-A is an evaluation board for the AK4633VN, 16bit mono CODEC with MIC/SPK amplifier. The AKD4633-A can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). AKD4633-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

### ■ Ordering guide

AKD4633-A --- Evaluation board for AK4633VN
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

## FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

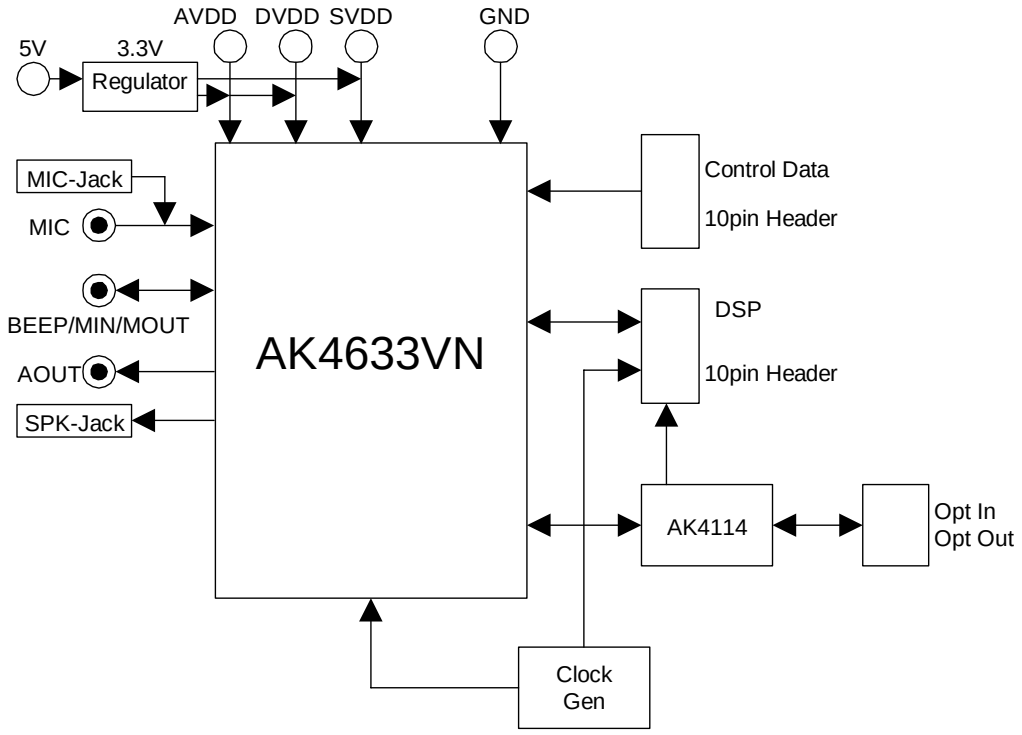



Figure 1. AKD4633-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

**Evaluation Board Manual**

## ■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD, DVDD, SVDD, and VCC are supplied from the regulator. (AVDD, DVDD, SVDD, and VCC jack should be open.). See "**Other jumper pins set up** (page 10)". <default>

| | | | |
|---|---|---|---|
| [REG] | (red ) | = 5V | |
| [AVDD] | (orange) | = open | : 3.3V is supplied to AVDD of AK4633VN from regulator. |
| [DVDD] | (orange) | = open | : 3.3V is supplied to DVDD of AK4633VN from regulator. |
| [SVDD] | (blue) | = open | : 3.3V is supplied to SVDD of AK4633VN from regulator. |
| [VCC] | (orenge) | = open | : 3.3V is supplied to logic block from regulator. |
| [AVSS] | (black) | = 0V | : for analog ground |
| [AGND] | (black) | = 0V | : for analog ground |
| [DGND] | (black) | = 0V | : for logic ground |

1-2) When AVDD, DVDD, SVDD, and VCC are not supplied from the regulator. (AVDD, DVDD, SVDD, and VCC jack should be junction.) See "**Other jumper pins set up** (page 10)".

| | | |
|---|---|---|
| [REG] | (red) | = "REG" jack should be open. |
| [AVDD] | (orange) | = 2.6 ~ 3.6V : for AVDD of AK4633VN (typ. 3.3V) |
| [DVDD] | (orange) | = 2.6 ~ 3.6V : for DVDD of AK4633VN (typ. 3.3V) |
| [SVDD] | (blue) | = 2.6 ~ 5.25V: for SVDD of AK4633VN (typ. 3.3V, 5.0V) |
| [VCC] | (orenge) | = 2.6 ~ 3.6V : for logic (typ. 3.3V) |
| [AVSS] | (black) | = 0V : for analog ground |
| [AGND] | (black) | = 0V : for analog ground |
| [DGND] | (black) | = 0V : for logic ground |

Each supply line should be distributed from the power supply unit.
AVDD and DVDD must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4633VN and AK4114 should be reset once bringing SW1, 2 "L" upon power-up.

## ■ Evaluation mode

**In case of AK4633VN evaluation using AK4114, it is necessary to correspond to audio interface format for AK4633VN and AK4114. About AK4633VN's audio interface format, refer to datasheet of AK4633VN. About AK4114's audio interface format, refer to Table 2 in this manual.**

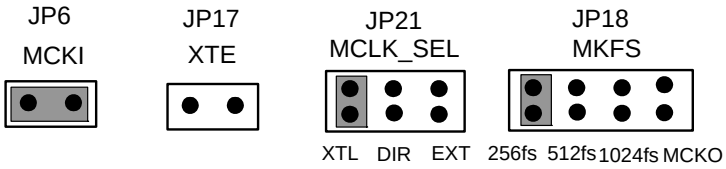
**Applicable Evaluation Mode**

**(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode**
**(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)**
**(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: BICK or FCK pin)**
**(4) Evaluation of using DIR of AK4114 (opt-connector) : EXT, Slave Mode**
**(5) Evaluation of using DIT of AK4114 (opt-connector) : EXT, Slave Mode**

**(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode**

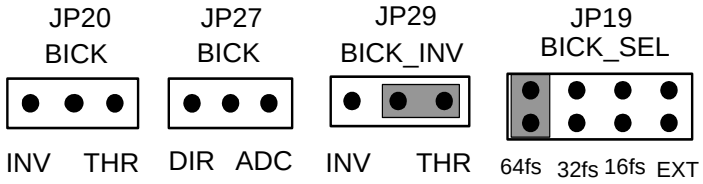
a) Set up jumper pins of MCKI clock

X'tal of 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz can be set in X2. X'tal of 12.288MHz (Default) is set on the AKD4633VN. Set "No.8 of SW3" to "H".
When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz) through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

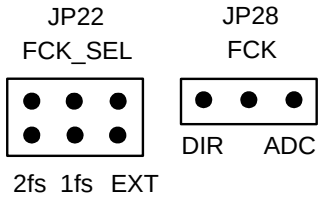



b) Set up jumper pins of BICK clock

Output frequency (16fs/32fs/64fs) of BICK should be set by "BCKO1-0 bit" in the AK4633VN.
There is no necessity for set up JP19.

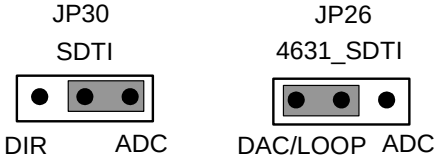



c) Set up jumper pins of FCK clock




d) Set up jumper pins of DATA

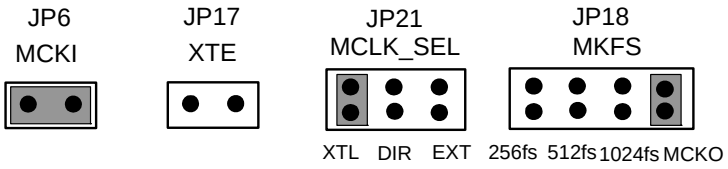
When the AK4633VN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



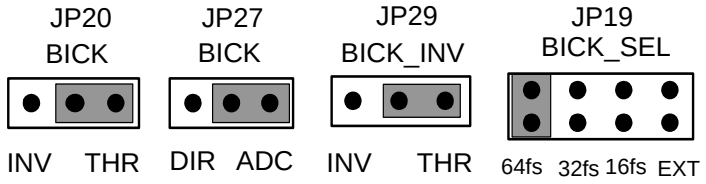
**(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)**

a) Set up jumper pins of MCKI clock

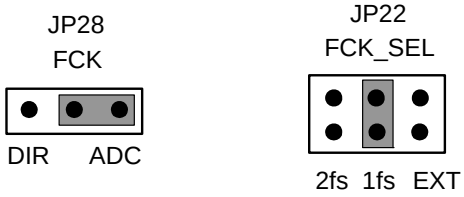
X'tal of 12.288MHz (Default) is set on the AKD4633-A. In this case, the AK4633VN corresponds to PLL reference clock of 12.288MHz. In this evaluation mode, the output clock from MCKO-pin of the AK4633VN is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Then "MCKO bit" in the AK4633VN should be set to "1". When an external clock through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to match the output impedance of the clock generator.




b) Set up jumper pins of BICK clock

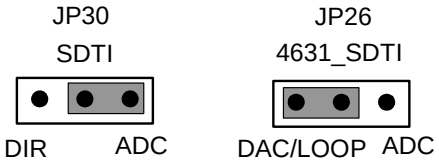



c) Set up jumper pins of FCK clock




d) Set up jumper pins of DATA

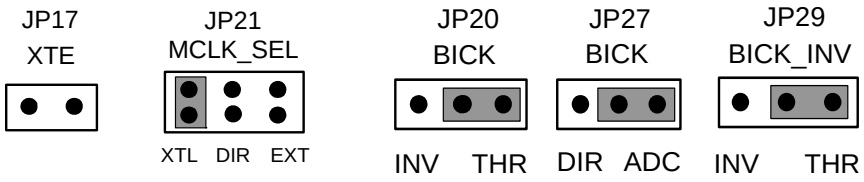
When the AK4633VN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



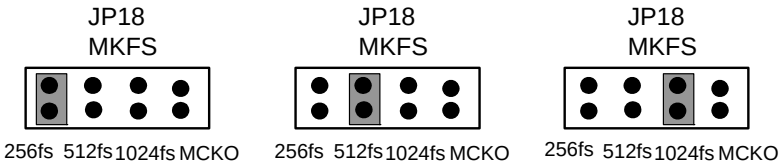
**(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: BICK or FCK pin)**

a) Set up jumper pins of BICK clock

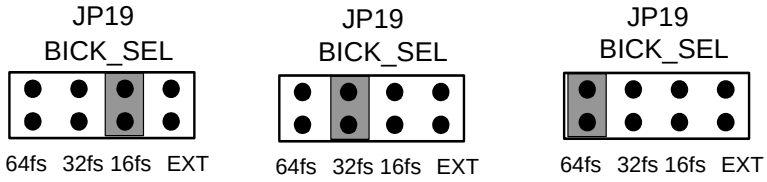
When an external clock through a RCA connector J8 (EXT/BICK) is supplied, select EXT on JP19 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to match the output impedance of the clock generator.




In this evaluation mode, the selected clock from JP21 (MCLK_SEL) is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Input frequency of master clock is set up in turn “256fs”, “512fs”, “1024fs” from left.

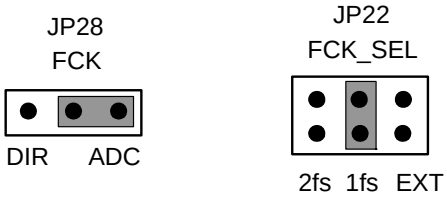



And input frequency of BICK is set up in turn “16fs”, “32fs”, “64fs” from left.



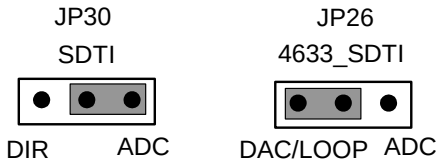
b) Set up jumper pins of FCK clock

When an external clock through a RCA connector J9 (FCK) is supplied, select EXT on JP22 (FCK_SEL). JP24 (EXT2) and R27 should be properly selected in order to match the output impedance of the clock generator.



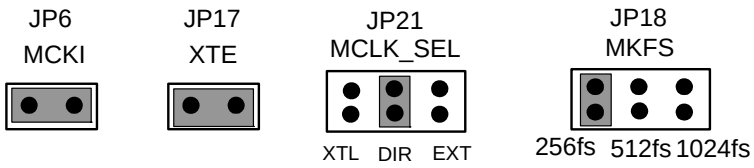

c) Set up jumper pins of DATA

When the AK4633VN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.

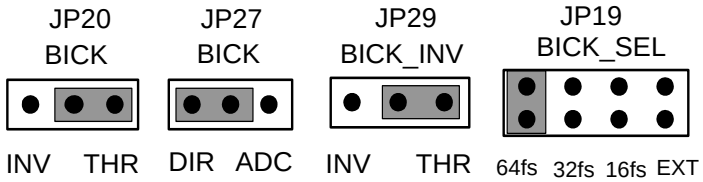


**(4) Evaluation of using DIR of AK4114 (opt-connector) : EXT, Slave Mode**

a) Set up jumper pins of MCKI clock

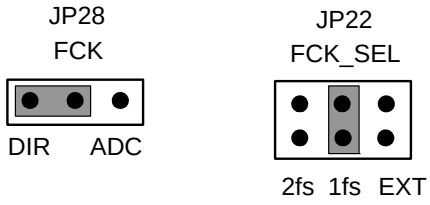



b) Set up jumper pins of BICK clock



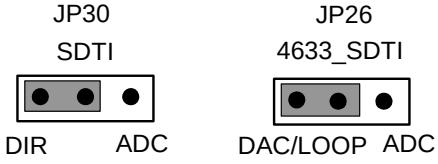

c) Set up jumper pins of FCK clock

JP24 (EXT2) and R27 should be properly selected in order to match the output impedance of the clock generator.



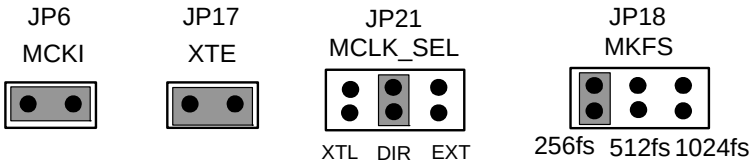

d) Set up jumper pins of DATA

When D/A converter of the AK4633VN is evaluated by using DIR of AK4114, the jumper pins should be set to the following.

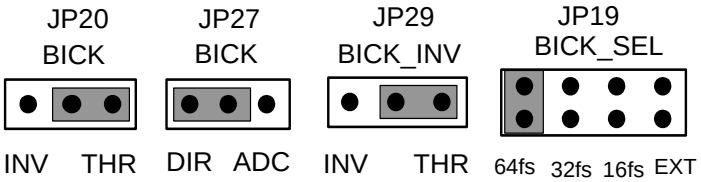


**(5) Evaluation of using DIT of AK4114 (opt-connector) : EXT, Slave Mode**

a) Set up jumper pins of MCKI clock

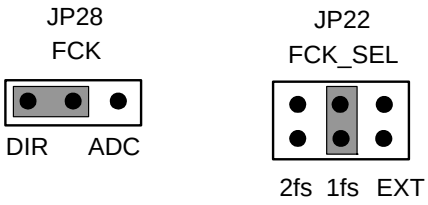



b) Set up jumper pins of BICK clock



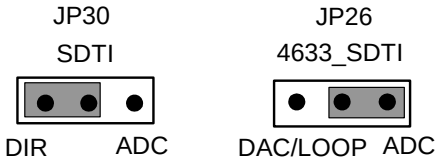

c) Set up jumper pins of FCK clock

JP24 (EXT2) and R27 should be properly selected in order to match the output impedance of the clock generator.




d) Set up jumper pins of DATA

When A/D converter of the AK4633VN is evaluated by using DIR of AK4114, the jumper pins should be set to the following.



## ■ DIP Switch set up

[SW3] (MODE) : Mode Setting of AK4633-VN and AK4114
ON is “H”, OFF is “L”.

| No. | Name | ON (“H”) | OFF (“L”) |
|---|---|---|---|
| 1 | DIF0 | AK4114 Audio Format Setting See Table 2 | |
| 2 | DIF1 | | |
| 3 | DIF2 | | |
| 4 | CM0 | Clock Operation Mode select See Table 3 | |
| 5 | CM1 | | |
| 6 | OCKS0 | Master Clock Frequency Select See Table 4 | |
| 7 | OCKS1 | | |
| 8 | M/S | Master mode | Slave mode |

Note. When the AK4633VN is evaluated Master mode, “No.8 of SW3” is set to “H”.
Table 1. Mode Setting for AK4633VN and AK4114

| Resistor setting for AK4633VN Audio Interface Format | | Setting for AK4114 Audio Interface Format | | | | | |
|---|---|---|---|---|---|---|---|
| DIF1 bit | DIF0 bit | DIF0 | DIF1 | DIF2 | DAUX | SDTO | |
| 0 | 1 | L | L | L | 24bit, Left justified | 16bit, Right justified | |
| 1 | 0 | L | L | H | 24bit, Left justified | 24bit, Left justified | Default |
| 1 | 1 | H | L | H | 24bit, $I^2S$ | 24bit, $I^2S$ | |

Note. When the AK4633VN is evaluated by using DIR/DIT of AK4114, “No.8 of SW3” is set to “L”.
Table 2. Setting for AK4114 Audio Interface Format

| Mode | CM1 | CM0 | UNLOCK | PLL | X'tal | Clock source | SDTO | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | - | ON | ON(Note) | PLL | RX | |
| 1 | 0 | 1 | - | OFF | ON | X'tal | DAUX | |
| 2 | 1 | 0 | 0 | ON | ON | PLL | RX | Default |
| | | | 1 | ON | ON | X'tal | DAUX | |
| 3 | 1 | 1 | - | ON | ON | X'tal | DAUX | |

ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note : When the X’tal is not used as clock comparison for fs detection (i.e. XTL1,0= “1,1”), the X’tal is off. Default setting is recommended.

Table 3. Clock Operation Mode select

| No. | OCKS1 | MCKO1 | MCKO2 | X’tal | |
|---|---|---|---|---|---|
| 0 | 0 | 256fs | 256fs | 256fs | Default |
| 2 | 1 | 512fs | 256fs | 512fs | |

Table 4. Master Clock Frequency Select (Stereo mode)

## ■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   - OPEN : Separated.
   - SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP2 (MICP) : Connection between MICP pin and BEEP pin of the AK4633VN.
   - MICP : MIC Differential input.
   - BEEP : BEEP input. <Default>

3. JP3 (AVDD_SEL) : AVDD of the AK4633VN
   - REG : AVDD is supplied from the regulator ("AVDD" jack should be open). < Default >
   - AVDD : AVDD is supplied from "AVDD " jack.

4. JP9 (DVDD_SEL) : DVDD of the AK4633VN
   - AVDD : DVDD is supplied from "AVDD". < Default >
   - DVDD : DVDD is supplied from "DVDD " jack.

5. JP10 (LVC_SEL) : Logic block of LVC is selected supply line.
   - DVDD : Logic block of LVC is supplied from "DVDD". < Default >
   - VCC : Logic block of LVC is supplied from "VCC " jack.

6. JP11 (VCC_SEL) : Logic block is selected supply line.
   - LVC : Logic is supplied from supply line of LVC. < Default >
   - VCC : Logic block of LVC is supplied from "VCC " jack.

7. JP4 (SVDD_SEL) : SVDD of the AK4633VN
   - REG : SVDD is supplied from the regulator ("SVDD" jack should be open). < Default >
   - SVDD : SVDD is supplied from "SVDD " jack.

8. JP8 (MCKO_SEL) : Master Clock Frequency is selected clock from MCKO1 or MCKO2 of the AK4114.
   - MCKO1 : The check from MCKO1 of AK4114 is provided to MCKI of the AK4633VN. < Default >
   - MCKO2 : The check from MCKO2 of AK4114 is provided to MCKI of the AK4633VN.

## ■ The function of the toggle SW

[SW1] (DIR) : Power control of AK4114. Keep “H” during normal operation.
Keep “L” when AK4114 is not used.

[SW2] (PDN) : Power control of AK4633VN. Keep “H” during normal operation.

## ■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

## ■ Serial Control

The AK4633VN can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CTRL) with PC by 10 wire flat cable packed with the AKD4633-A

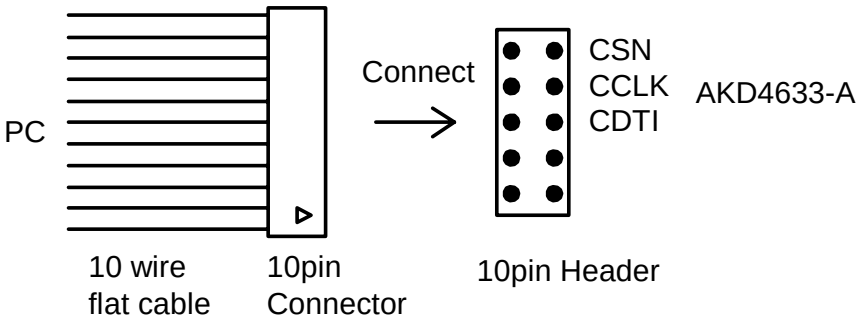



Figure 2. Connect of 10 wire flat cable

## ■ Analog Input / Output Circuits

(1) Input Circuits

a) MIC Input Circuit

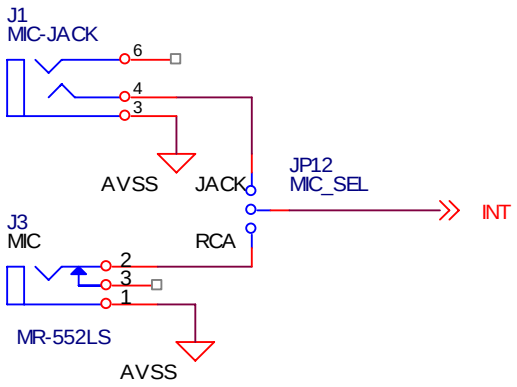
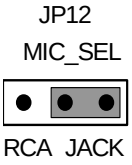
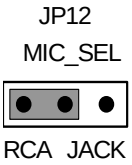



Figure 3. MIC Input Circuit

(a-1) Analog signal is input to MIC pin via J1 connector.




(a-2) Analog signal is input to MIC pin via J3 connector.




b) BEEP Input Circuit

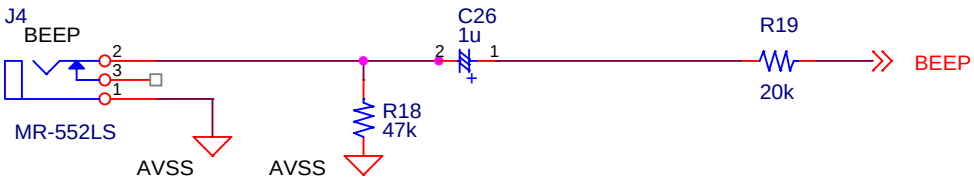



Figure 4. BEEP Input Circuit

(2) Output Circuits

a) AOUT Output Circuit

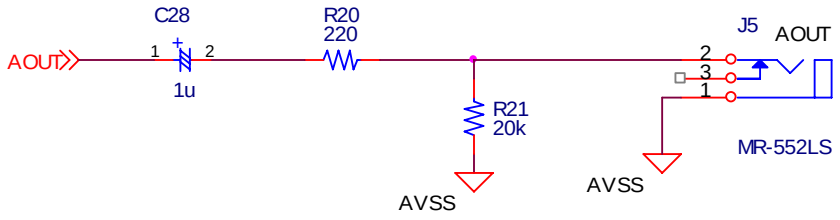



Figure 5. AOUT Output Circuit

b) SPK Output Circuit

Note. When mini-jack is inserted or pulled out J2 (SPK-JACK) connector, JP13 (SPP_SEL) and JP14 (SPN_SEL) should be open, or “PMSPK bit” in the AK4633VN should be set to “0”.

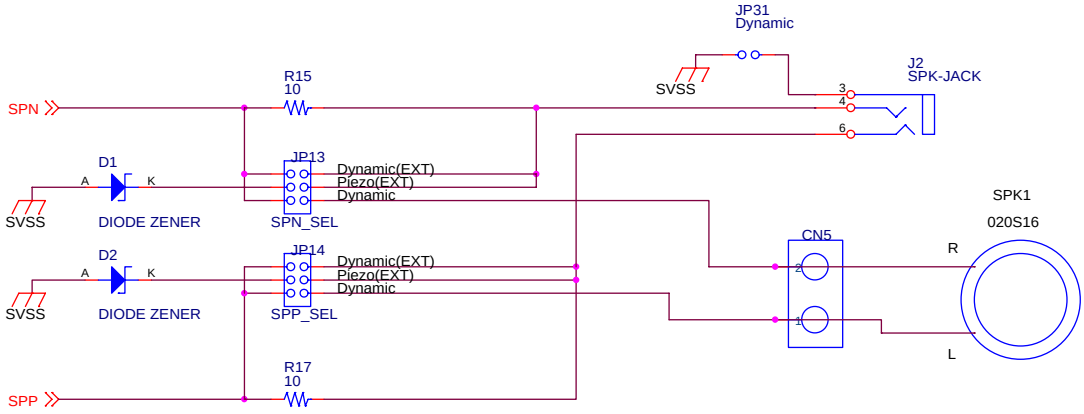
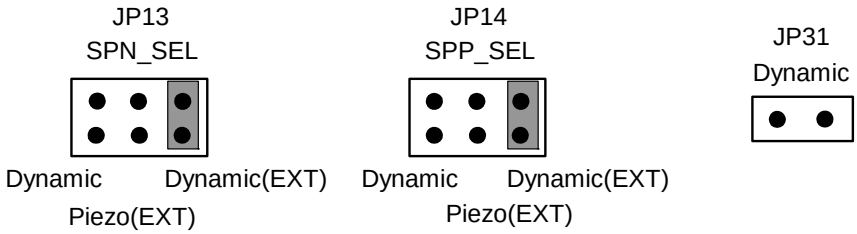
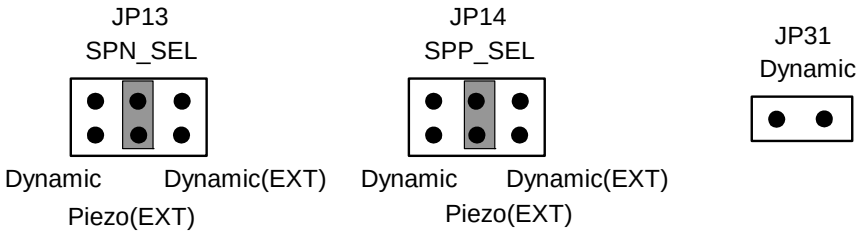



Figure 6. SPK Output Circuit

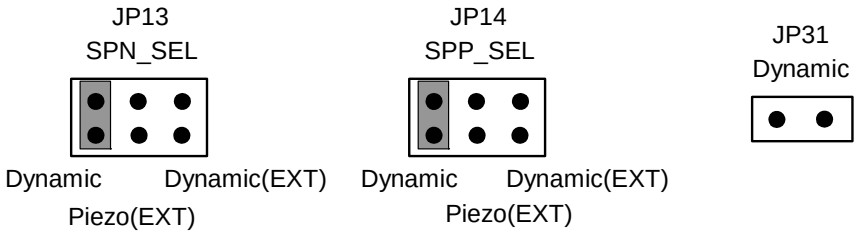
(b-1) An external dynamic speaker is evaluated by using J2 (SPK-JACK) connector.




(b-2) An external Piezo speaker is evaluated by using J2 (SPK-JACK) connector.




(b-3) Analog signal of SPP/SPN pins are output from "Dynamic Speaker" on the evaluation (SPK1).




∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

## 2. Control Software Manual

### ■ Set-up of evaluation board and control software

1. Set up the AKD4633-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4633-A by 10-line type flat cable (packed with AKD4633-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AK4633VN Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4633.exe” to set up the control program.

5. Then please evaluate according to the follows.

### ■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.

### ■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) .
2. [Write default] : Initialize the register of AK4633VN.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to write data by keyboard operation.
6. [Function3] : The sequence of register setting can be set and executed.
7. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE] : Save the current register setting.
10. [OPEN] : Write the saved values to all register.
11. [Write] : Dialog to write data by mouse operation.

### ■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

## ■ Explanation of each dialog

**1. [Write Dialog]**: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4633VN, click [OK] button. If not, click [Cancel] button.

**2. [Function1 Dialog]** : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4633VN, click [OK] button. If not, click [Cancel] button.

**3. [Function2 Dialog]** : Dialog to evaluate IVOL and DVOL

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4633VN by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4633VN, click [OK] button. If not, click [Cancel] button.

## 4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4633VN. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

### 5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is “aks”.

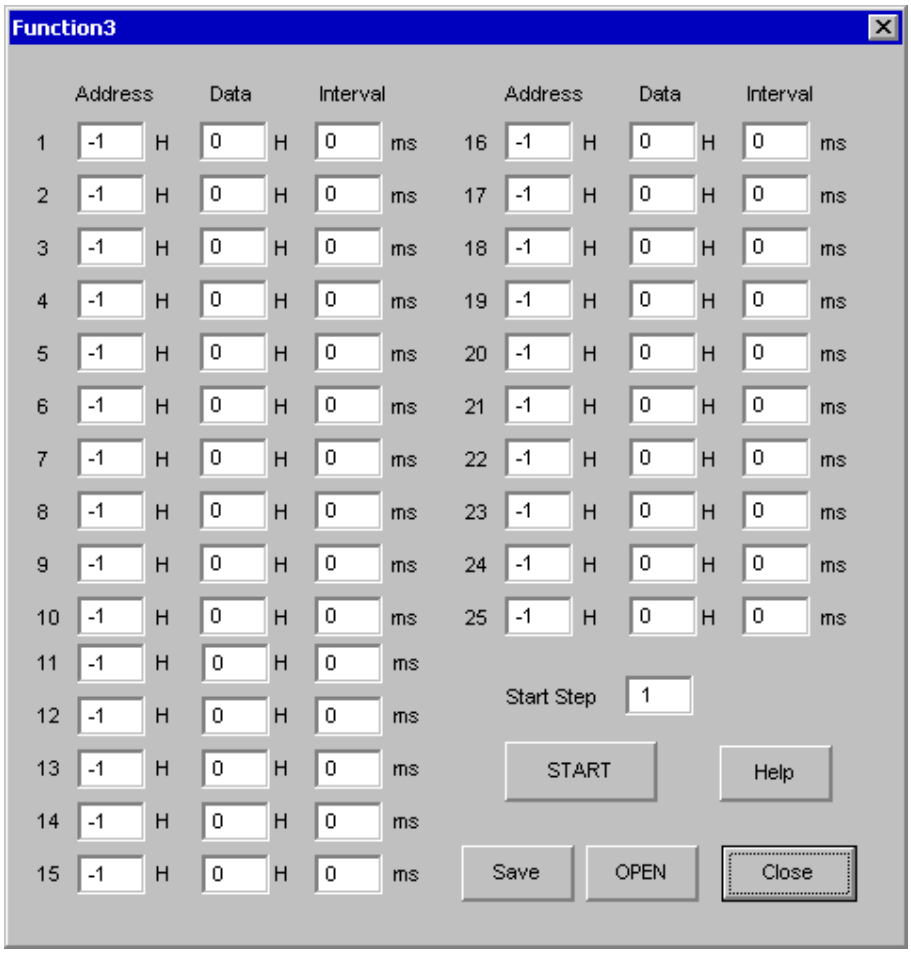



**Figure 1. Window of [F3]**

### 6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

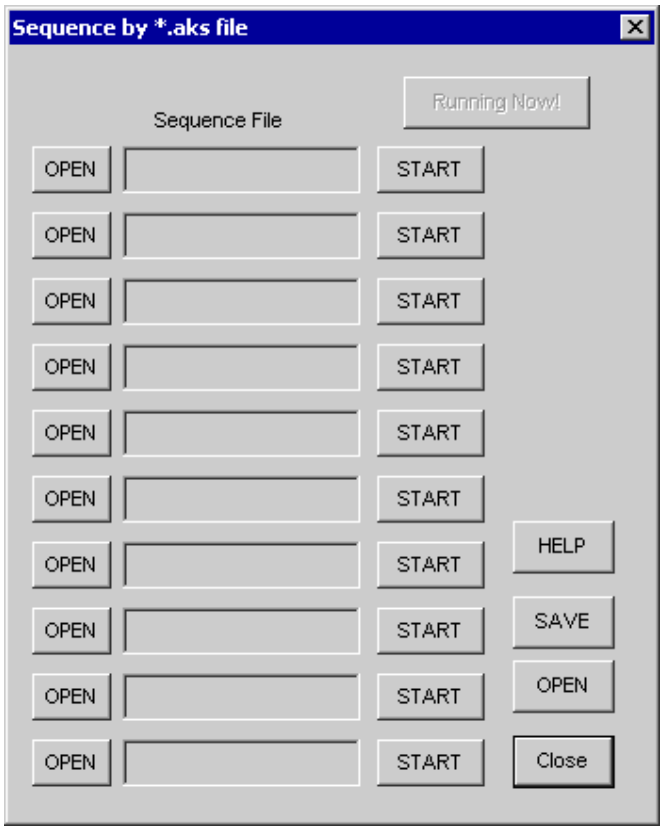



**Figure 2. [F4] window**

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 3.

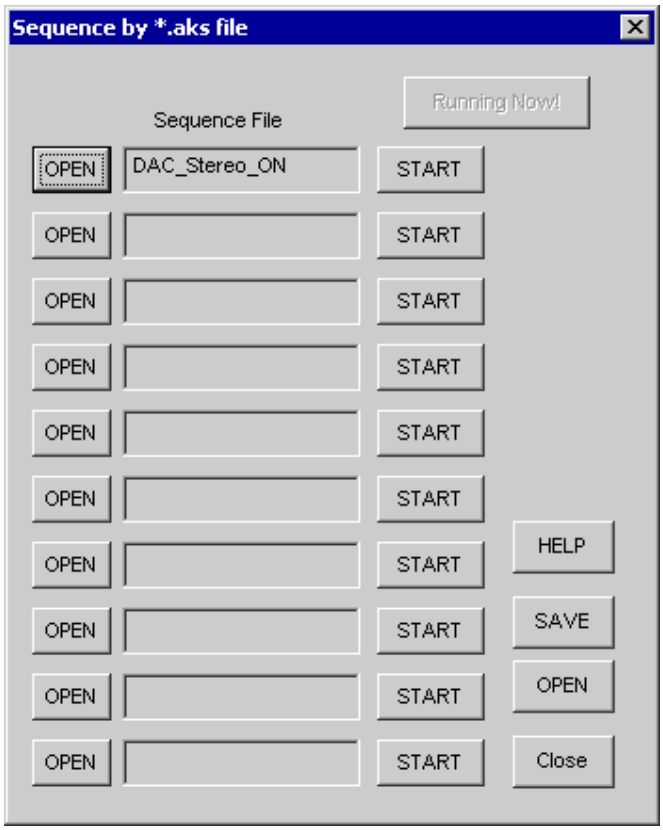



**Figure 3. [F4] window(2)**

(2) Click [START] button, then the sequence is executed.

3-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

3-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

## 7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 4 opens.

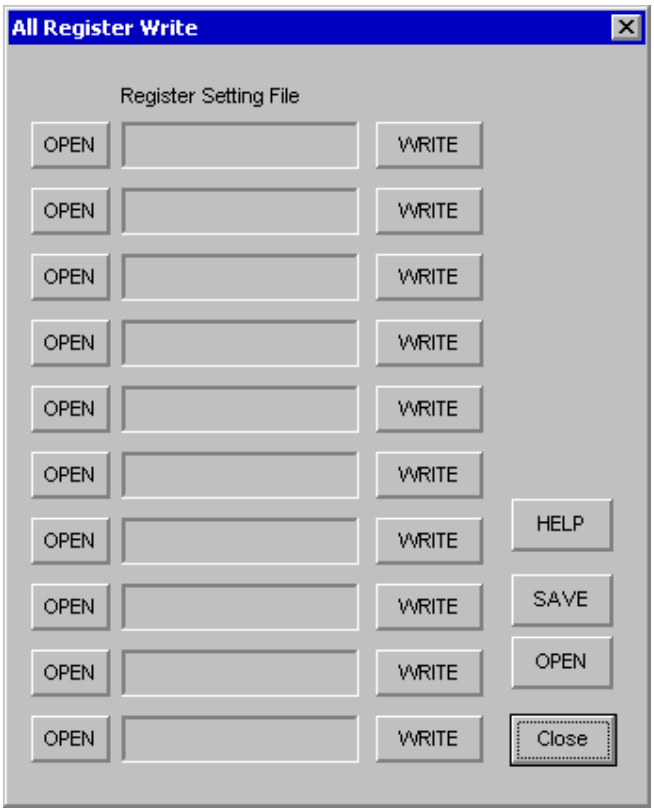



**Figure 4. [F5] window**

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 5.

(2) Click [WRITE] button, then the register setting is executed.

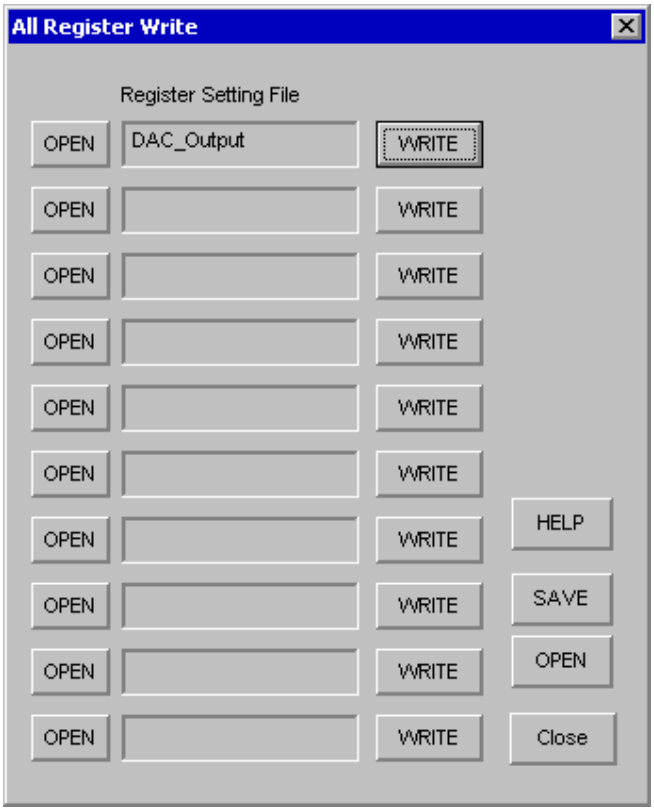



**Figure 5. [F5] windows(2)**

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

## 8. [Filter Dialog]

It is possible to calculate the coefficients of HPF and EQ filters, write these coefficients to registers and confirm the frequency response of these filters. Click [Filter] button, then the window as shown in Figure 6 opens.

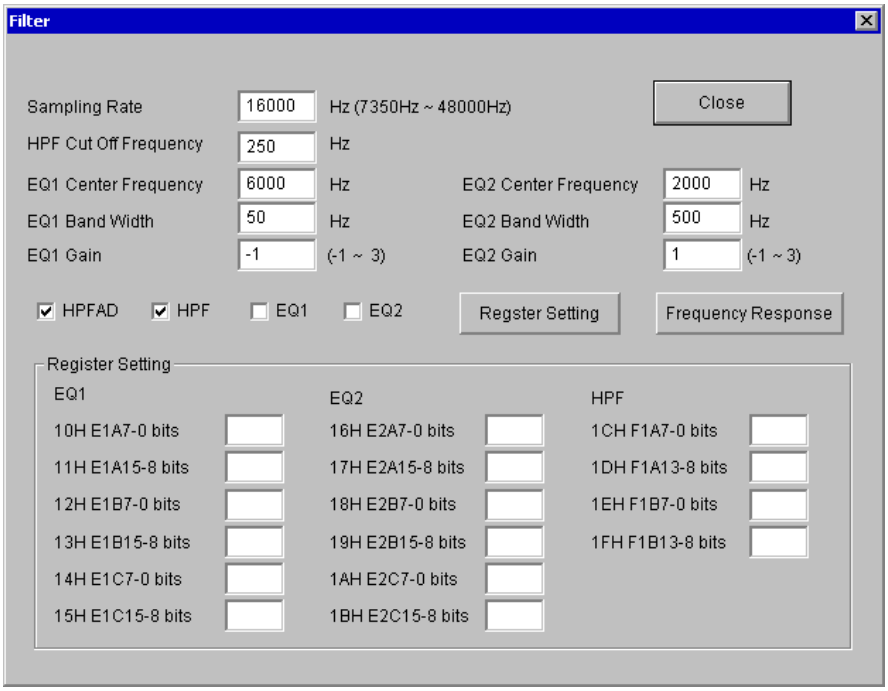



**Figure 6. [Filter] Window**

### (1) Setup the Parameters

Set up the parameters of HPF and EQ filters.

| Parameter | Contents | Setup range |
|---|---|---|
| Sampling Rate | Sampling Frequency (fs) | 48000Hz ≥ fs ≥ 7350Hz |
| HPF Cut Off Frequency | High Pass Filter Cut Off Frequency | (fs/2 – 1) ≥ fc > fs/10000 |
| EQ1 Center Frequency | EQ1 Center Frequency | fs/2 ≥ EQ1 > 0Hz |
| EQ1 Band Width | EQ1 Band Width (Note 1) | fs/2 ≥ EQ1 >1Hz |
| EQ1 Gain | EQ1 Gain (Note 2) | 3 > EQ1 ≥- 1 |
| EQ2 Center Frequency | EQ2 Center Frequency | fs/2 ≥ EQ2 > 0Hz |
| EQ2 Band Width | EQ2 Band Width (Note 1) | fs/2 ≥ EQ2 >1Hz |
| EQ2 Gain | EQ2 Gain (Note 2) | 3 > EQ2 ≥- 1 |

Note 1. Band width of 3dB gain difference from center frequency
Note 2. This filter is notch filter when this gain is -1.

### (2) Filter ON/OFF

Set up the ON or OFF of filters by the check button of "HPFAD", "HPF", "EQ1" and "EQ2". The filter is ON when the button is checked.


**Figure 7. Filter ON/OFF check button**

(3) Calculation of Register Setting

When [Register Setting] is clicked, the register setting of filters are displayed in "Register Setting" area. At the same this, these setting are written to HPFAD bit, HPF bit, EQ1 bit, EQ2 bit and 10H-1FH registers. If the parameter is out of range, then the error message is displayed and these writing to register aren't executed.

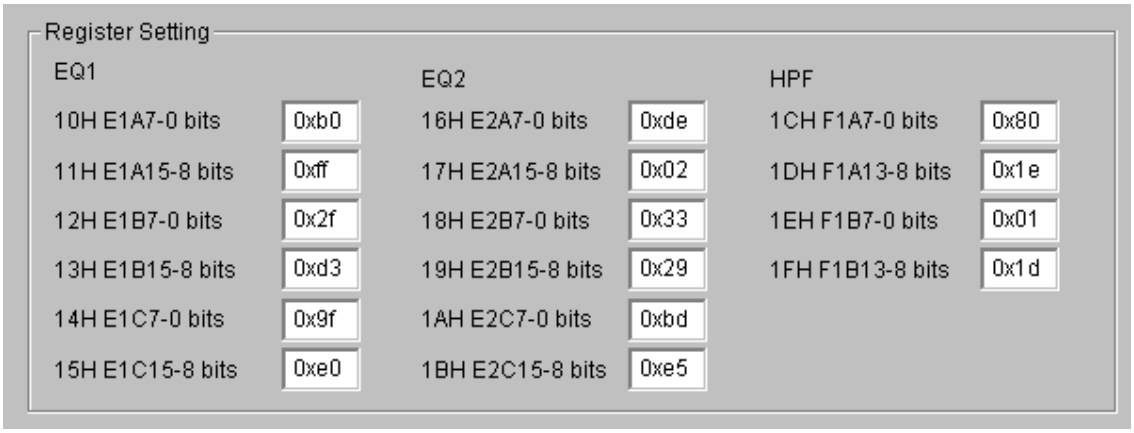



**Figure 8. Calculation result to register parameters**

(4) Frequency Response

When [Register Setting] is clicked, the frequency response is displayed. At the same this, these setting are written to HPFAD bit, HPF bit, EQ1 bit, EQ2 bit and 10H-1FH registers. If [UpDate] button is clicked after setting the frequency range, the display of frequency response is updated.

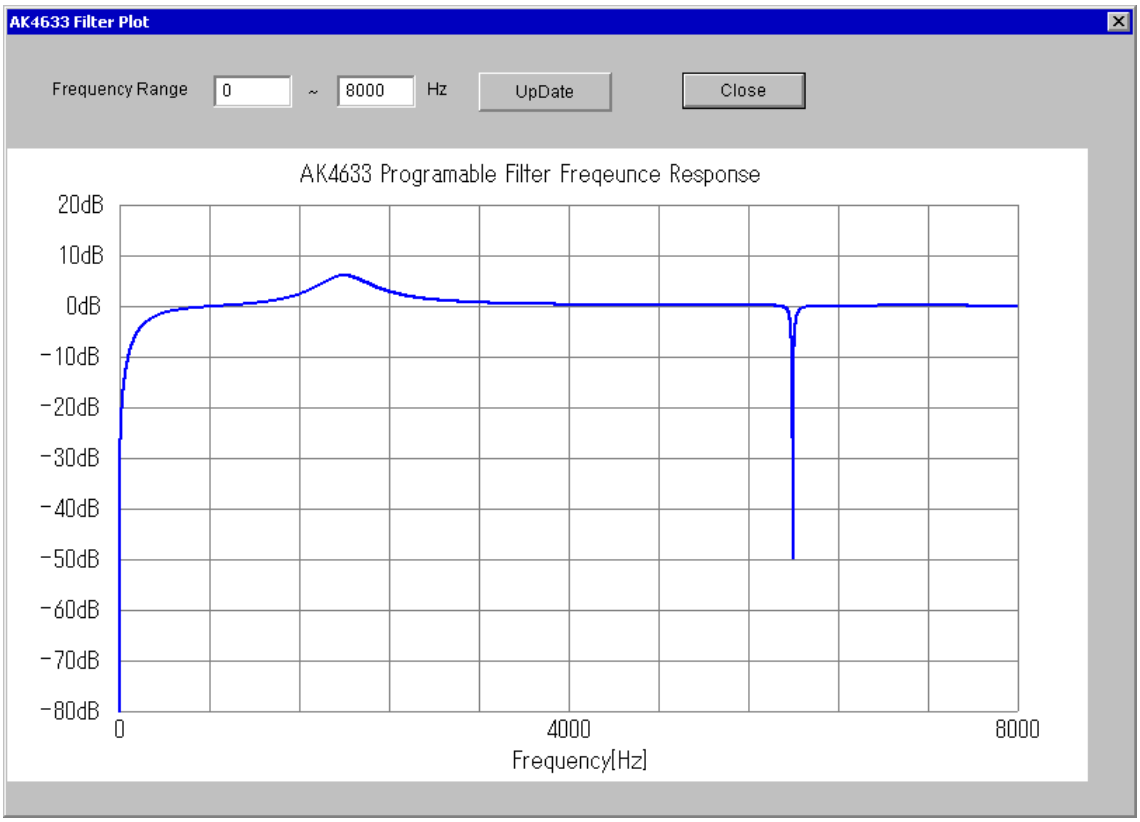
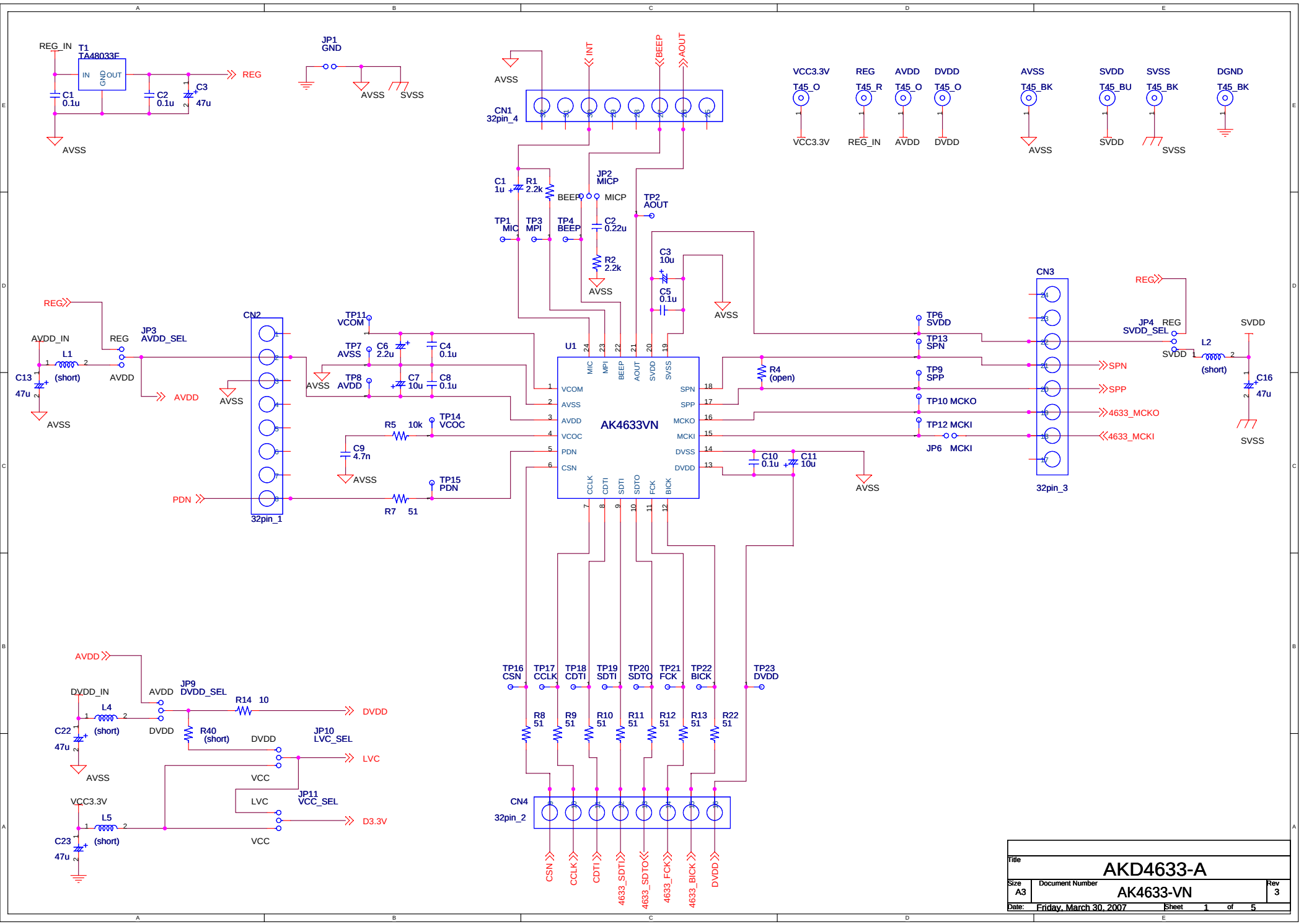



**Figure 9. Frequency characteristic indicates result**

## Revision History

| Date | Manual Revision | Board Revision | Reason | Contents |
|---|---|---|---|---|
| 05/07/14 | KM079400 | 0 | First Edition | |
| 05/08/23 | KM079401 | 1 | Update | Change of a figure & circuit |
| 05/09/16 | KM079402 | 1 | Error Correct | Port Numbers are corrected in circuit. |
| 05/10/21 | KM079403 | 2 | Update | Device revision of AK4633 is changed to “Rev.B”. |
| 06/04/14 | KM079404 | 2 | Update | Part change in LOGIC circuit diagram.<br>U9: 74LVC541→74HC541 |
| 07/02/15 | KM079405 | 3 | Error Correct | Port number was corrected in both silkscreen printing and circuit diagram. JP1(MICP) → JP2 (MICP) |
| 07/04/02 | KM079406 | 3 | Error Correct | Port number was corrected in both silkscreen printing and circuit diagram.<br>Silkscreen printing: JP2 (MCKI) → JP6 (MCKI)<br>Circuit diagram: JP5 (MCKI) → JP6 (MCKI) |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T1
TA48033F
IN
GND
OUT
REG
C1
0.1u
C2
0.1u
C3
47u
AVSS
JP1
GND
AVSS
SVSS
AVSS
INT
BEEP
AOUT
CN1
32pin_4
VCC3.3V
T45_O
REG
T45_R
AVDD
T45_O
DVDD
T45_O
AVSS
T45_BK
SVDD
T45_BU
SVSS
T45_BK
DGND
T45_BK
C1
1u
R1
2.2k
BEEP
JP2
MICP
MICP
TP2
AOUT
TP1
MIC
TP3
MPI
TP4
BEEP
C2
0.22u
R2
2.2k
AVSS
C3
10u
C5
0.1u
AVSS
REG
AVDD_IN
JP3
AVDD_SEL
REG
L1
(short)
AVDD
C13
47u
AVSS
AVDD
AVSS
CN2
TP11
VCOM
TP7
AVSS
C6
2.2u
C4
0.1u
TP8
AVDD
C7
10u
C8
0.1u
AVSS
R5
10k
TP14
VCOC
C9
4.7n
AVSS
PDN
TP15
PDN
R7
51
32pin_1
U1
AK4633VN
MIC
MPI
BEEP
AOUT
SVDD
SVSS
VCOM
AVSS
AVDD
VCOC
PDN
CSN
SPN
SPP
MCKO
MCKI
DVSS
DVDD
CCLK
CDTI
SDTI
SDTO
FCK
BICK
R4
(open)
C10
0.1u
C11
10u
AVSS
TP6
SVDD
TP13
SPN
TP9
SPP
TP10
MCKO
TP12
MCKI
JP6
MCKI
CN3
SPN
SPP
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4633_MCKI
32pin_3
REG
JP4
SVDD_SEL
REG
SVDD
L2
(short)
SVDD
C16
47u
SVSS
AVDD
DVDD_IN
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DVDD_SEL
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10
DVDD
L4
(short)
C22
47u
AVSS
DVDD
R40
(short)
DVDD
JP10
LVC_SEL
LVC
VCC
JP11
VCC_SEL
VCC3.3V
LVC
D3.3V
L5
(short)
C23
47u
AVSS
VCC
TP16
CSN
TP17
CCLK
TP18
CDTI
TP19
SDTI
TP20
SDTO
TP21
FCK
TP22
BICK
TP23
DVDD
R8
51
R9
51
R10
51
R11
51
R12
51
R13
51
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Date:
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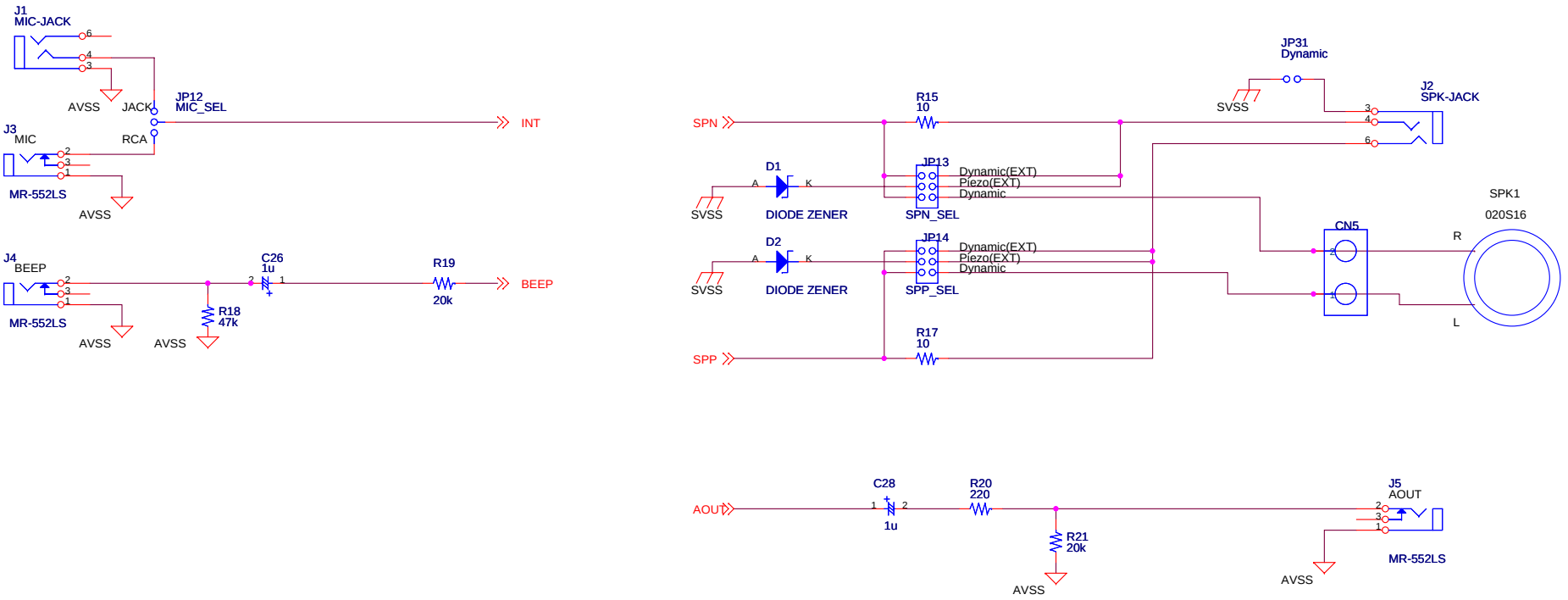


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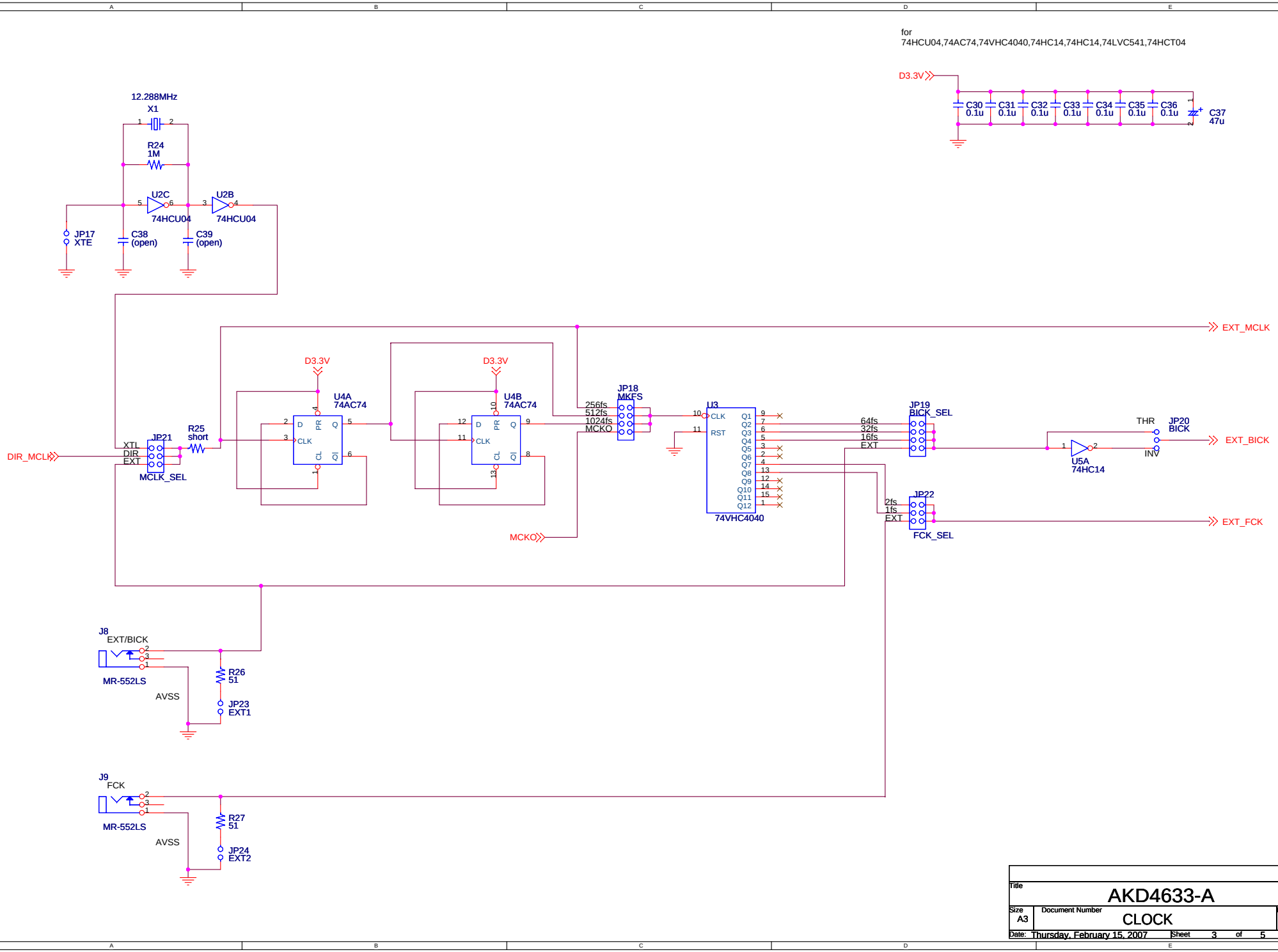
| Date: Thursday, February 15, 2007 | Sheet 2 of 5 | |


for
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D3.3V
C30 0.1u
C31 0.1u
C32 0.1u
C33 0.1u
C34 0.1u
C35 0.1u
C36 0.1u
C37 47u
12.288MHz
X1
R24 1M
U2C
74HCU04
U2B
74HCU04
JP17 XTE
C38 (open)
C39 (open)
EXT_MCLK
D3.3V
U4A 74AC74
D3.3V
U4B 74AC74
JP18 MKFS
256fs
512fs
1024fs
MCKO
U3
74VHC4040
JP19 BICK_SEL
64fs
32fs
16fs
EXT
THR
INV
JP20 BICK
EXT_BICK
U5A 74HC14
DIR_MCLK
JP21
XTL
DIR
EXT
MCLK_SEL
R25 short
MCKO
2fs
1fs
EXT
JP22
FCK_SEL
EXT_FCK
J8
EXT/BICK
MR-552LS
AVSS
R26 51
JP23 EXT1
J9
FCK
MR-552LS
AVSS
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Rev 3
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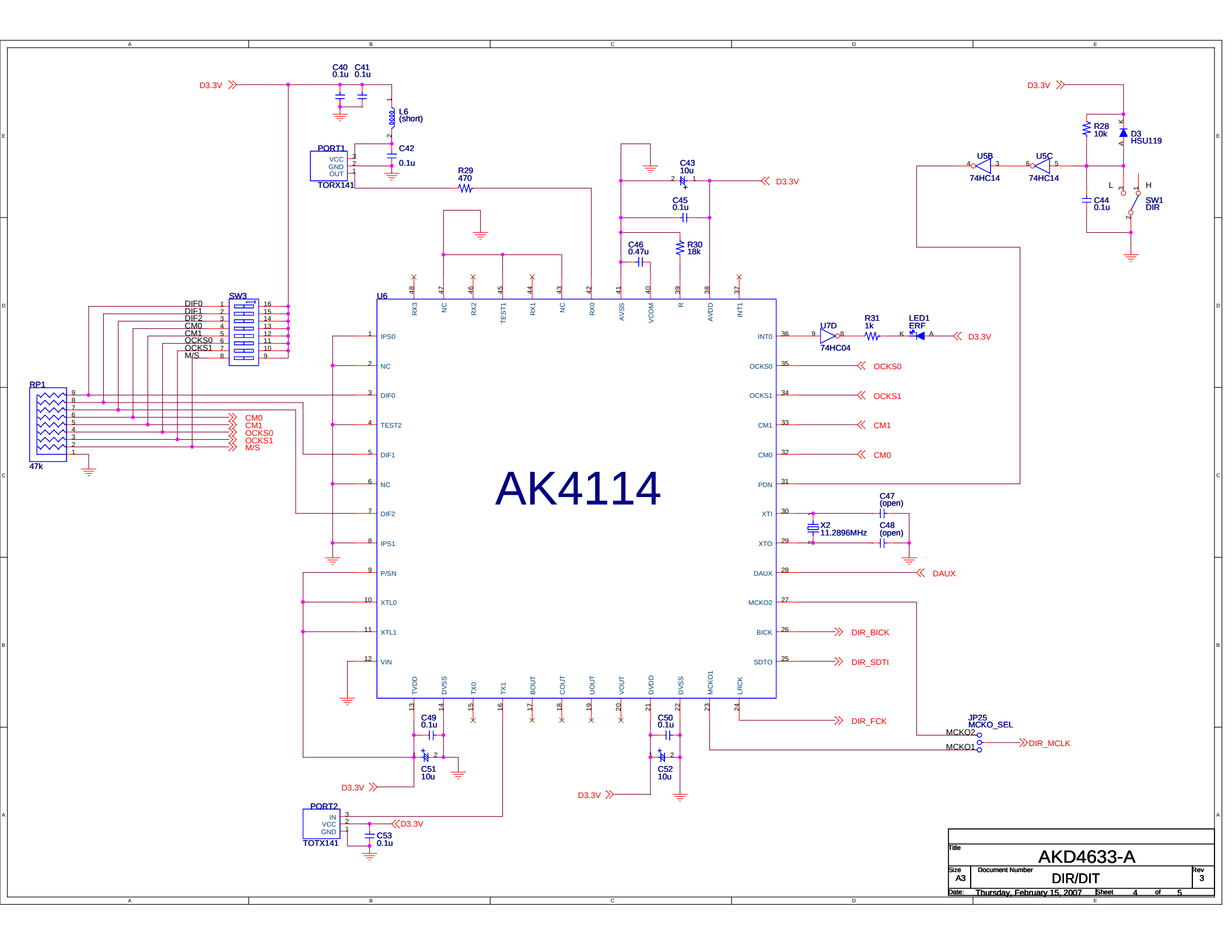


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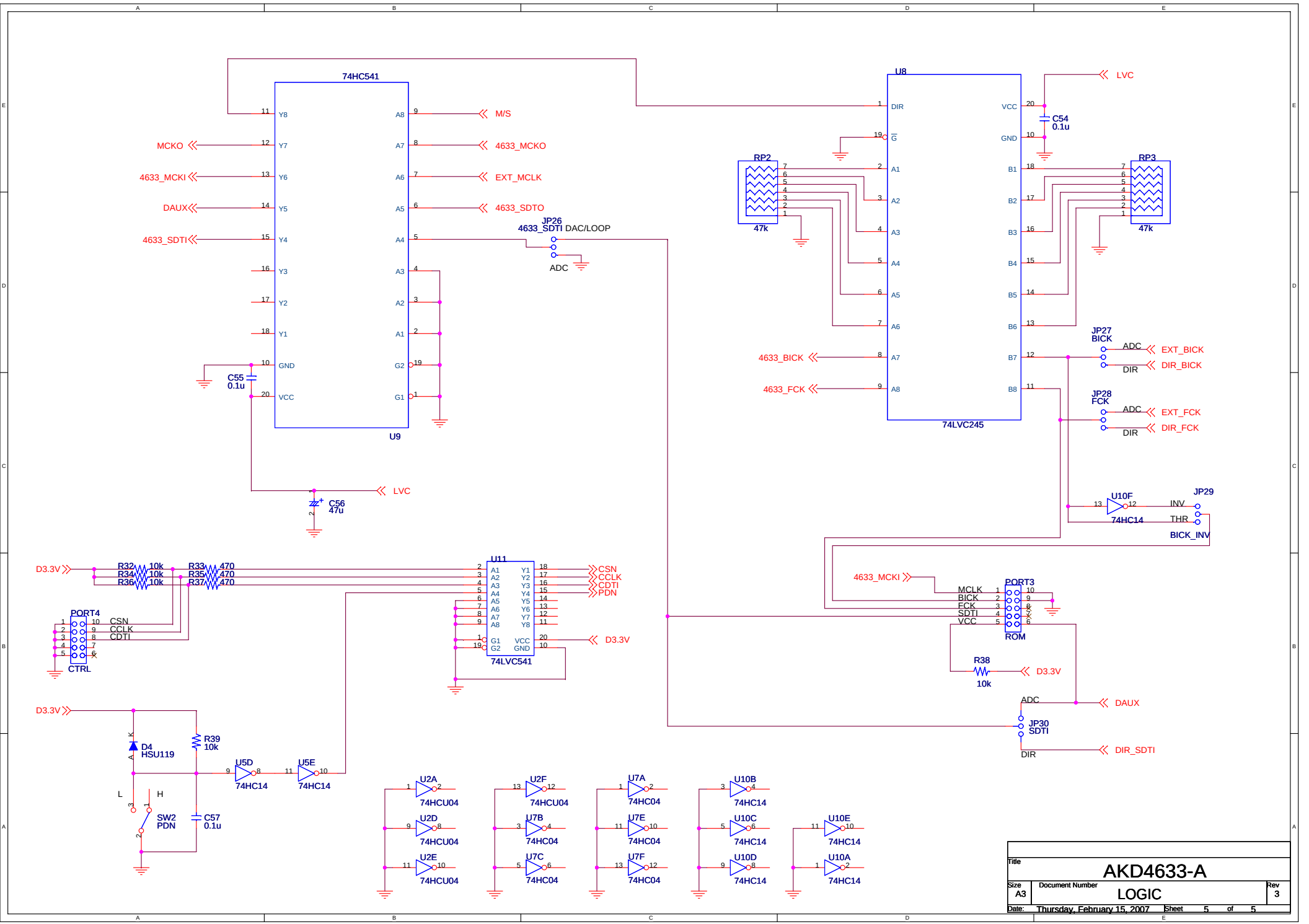
| Date: Thursday, February 15, 2007 | Sheet 4 of 5 | | |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Y7
Y6
Y5
Y4
Y3
Y2
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VCC
A8
A7
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A4
A3
A2
A1
G2
G1
MCKO
4633_MCKI
DAUX
4633_SDTI
M/S
4633_MCKO
EXT_MCLK
4633_SDTO
JP26
4633_SDTI DAC/LOOP
ADC
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0.1u
C56
47u
LVC
U8
74LVC245
DIR
G
VCC
GND
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
C54
0.1u
RP2
47k
RP3
47k
4633_BICK
4633_FCK
JP27
BICK
ADC
DIR
EXT_BICK
DIR_BICK
JP28
FCK
ADC
DIR
EXT_FCK
DIR_FCK
U10F
74HC14
INV
THR
JP29
BICK_INV
D3.3V
R32
R34
R36
10k
R33
R35
R37
470
PORT4
CTRL
CSN
CCLK
CDTI
U11
74LVC541
A1
A2
A3
A4
A5
A6
A7
A8
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
G1
G2
VCC
GND
CSN
CCLK
CDTI
PDN
D3.3V
4633_MCKI
PORT3
ROM
MCLK
BICK
FCK
SDTI
VCC
R38
10k
D3.3V
ADC
DAUX
JP30
SDTI
DIR
DIR_SDTI
D4
HSU119
R39
10k
U5D
74HC14
U5E
74HC14
L
H
SW2
PDN
C57
0.1u
U2A
U2D
U2E
74HCU04
U2F
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U7C
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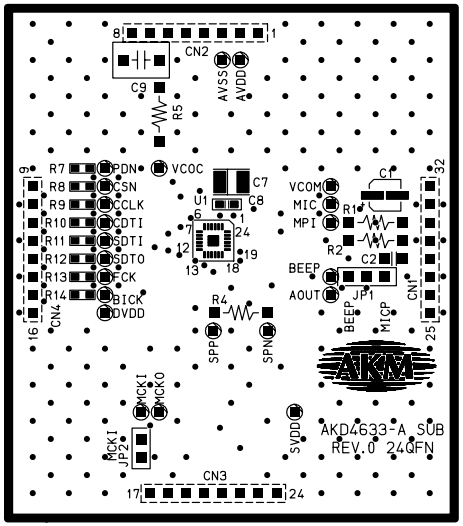
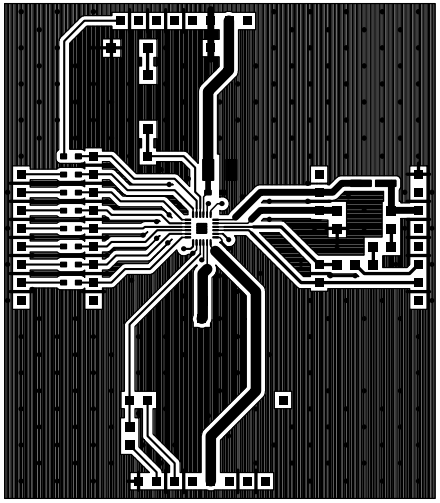


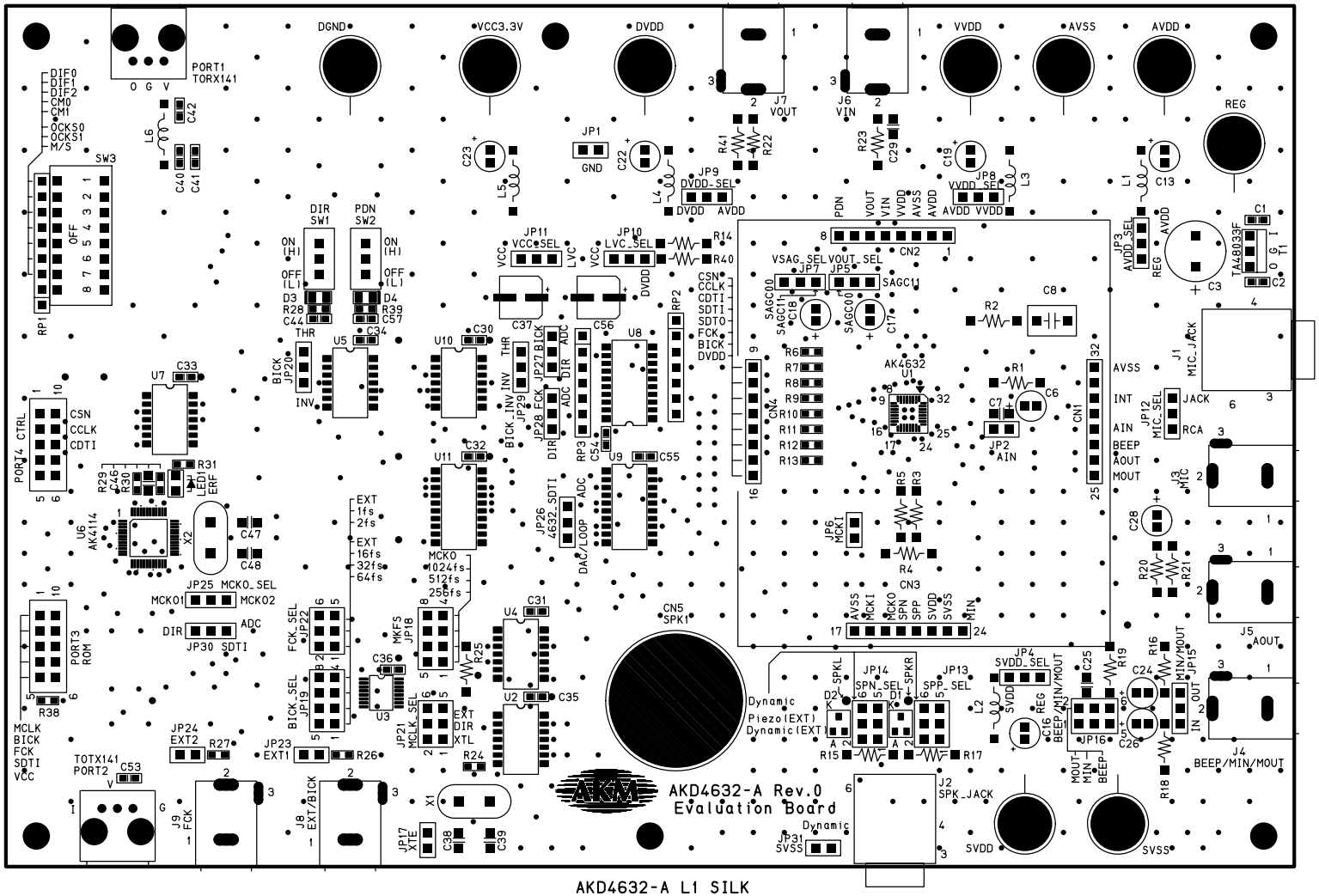

AKD4633-A SUB QFN L1 SILK

AKD6633-A SUB DFN L2 SILK



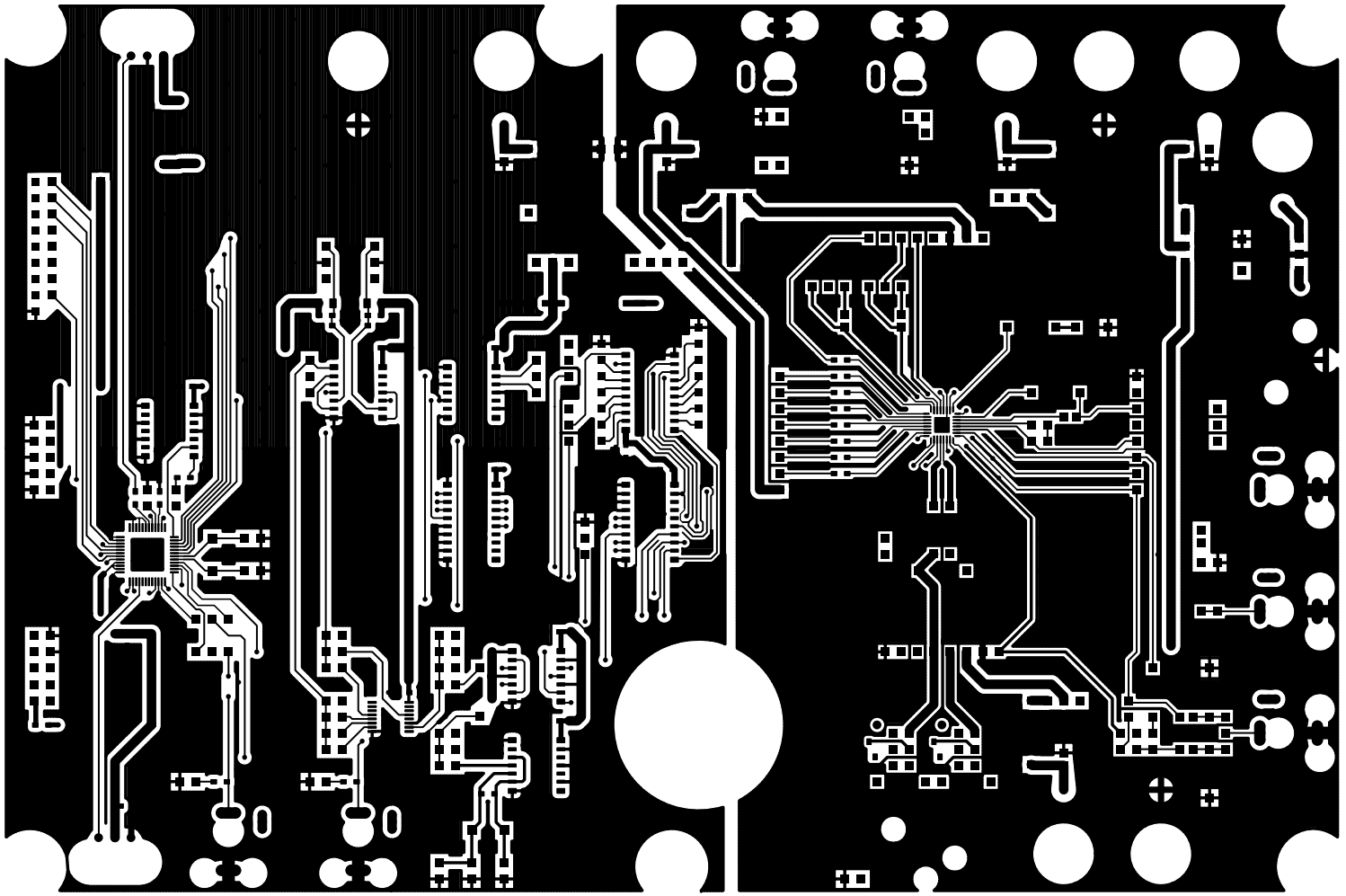
AKD4633-A SUB QFN L1

AKD4633-A SUB QFN L2




AKD4632-A L1 SILK

AKD4632-A L2 SILK



AKD4632-A L1

AKD4632-A L2