AKD4528
AK4528 Evaluation Board Rev.C

GENERAL DESCRIPTION

The AKD4528 is an evaluation board for the AK4528, the 24Bit A/D & D/A converter. The AKD4528 can evaluate A/D converter and D/A converter separately in addition to Loopback mode (A/D→D/A).
The AKD4528 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4528 --- AK4528 Evaluation Board
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This Control software does not operate on Windows NT.)

FUNCTION

☐ Digital interface
- DIT (AK4353), DIR (AK4112B) with optical output/input.
☐ 10pin header for serial control interface

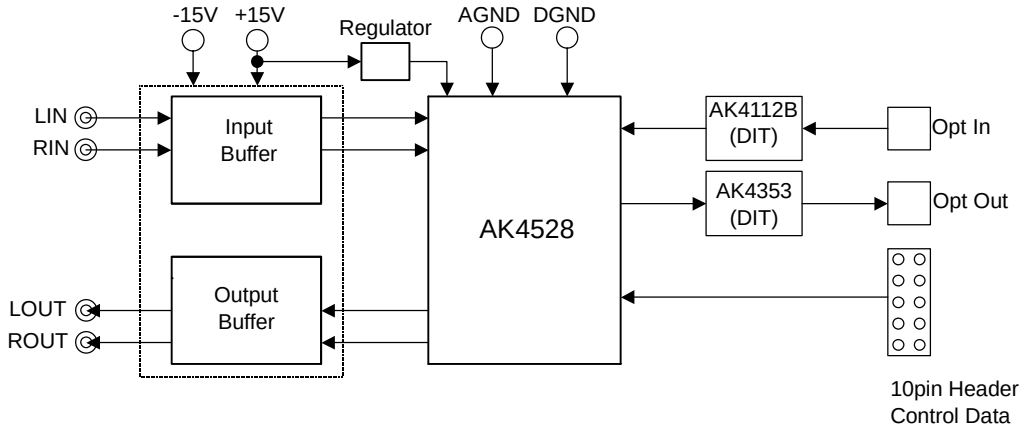


Figure 1. AKD4528 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

1. Analog Input Buffer Circuit

The ADC inputs are full differential and the input resistance is 27kΩ (typ. @fs=44.1kHz). The input signal range scales with the VREF voltage and nominally 0.56 x VREF Vpp. It is recommended that the input DC bias voltage is 2.9V(The bias is a voltage divided by resistors (3.3k and 4.7k) from VA in figure 2. The ADC output data format is 2's complement. The DC offset including ADC own DC offset removed by the internal HPF (fc=0.9Hz@fs=44.1kHz).
The AK4528 samples the analog inputs at 64fs. The digital filter rejects noise above the stopband except for multiples of 64fs. A simple RC filter may be used to attenuate any noise around 64fs though most audio signals do not have significant energy at 64fs. Figure 2 is an example of differential input circuit.

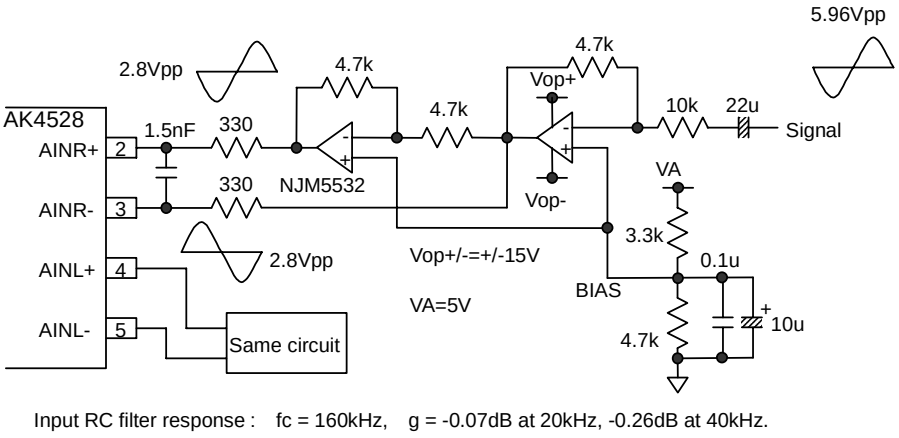


Figure 2. Differential Input Buffer Example

2.Analog Output Buffer Circuit

The 2nd-order LPF (fc=93.2kHz, Q=0.712) which adds differential output of AK4528 is implemented on the board. When the further attenuation of the out-band noise is needed, some additional LPF is required. NJM5532D is used for op-amp. Analog signal is output through BNC connectors (AOUTL, AOUTR) on board, and the output level of AK4528 is about 5.4Vp-p.

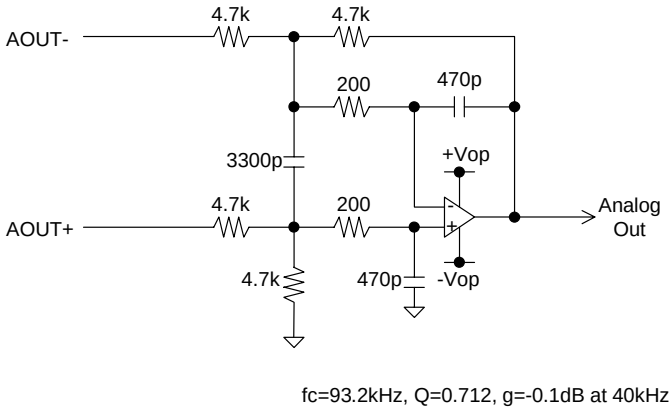


Figure 3. External 2nd order LPF Example (using dual supply op-amp)

1. Evaluation Board Manual

■ Operation sequence

1) Set up the power supply line

[+15V]	(Orange)	= +15V
[-15V]	(Green)	= -15V
[AGND]	(Black)	= 0V
[DGND]	(Black)	= 0V

Note: Power should be supplied after jumpers are set-ups properly.
Each supply line should be distributed from the power supply unit.

2) Set up the evaluation modes, jumper pins and DIP switch. (See the followings.)

3) Power on
The AK4528, AK4112B and AK4353 should be reset once bringing SW3 (PDN) "L" upon power-up.

■ Evaluation modes

Applicable evaluation modes

(1) Loopback mode (Default)
(2) Evaluation of ADC
(3) Evaluation of DAC

(1) Loopback mode (Default)
Clock mode of the AK4112B should be set to X'tal mode.

(2) Evaluation of ADC
TOTX176 is used for digital output. Clock mode of the AK4112B should be set to X'tal mode.

(3) Evaluation of DAC
TORX176 or COAX is used for digital input. Clock mode of the AK4112B should be set to PLL mode.

■ Set-up SW2

[SW2]: Set-up AK4112B. Upper is "ON"("H"), Lower is "OFF"("L")
(For further details, refer to the datasheet.)

No.	Name	Default	OFF	ON
1	OCKS0	OFF	Set-up the master clock frequency (Default: 256fs) (Refer to the datasheet.)	
2	OCKS1	OFF		
3	CM0	ON	Set-up the clock source (Default: X'tal) (Refer to the datasheet.)	
4	CM1	OFF		
5	DIF0	ON	Set–up the audio format (Default: 24bit, I^2S) (Refer to the datasheet.)	
6	DIF1	OFF		
7	DIF2	ON		

Table 1. Set up SW2

1. Set-up Master clock frequency

This master clock is generated by the AK4112B, and is supplied from MCKO1 pin of the AK4112B.

OCKS1 pin (SW2-2)	OCKS0 pin (SW2-1)	MCKO1	fs (kHz)	
0	0	256fs	32, 44.1, 48, 96	(Default)
0	1	256fs	32, 44.1, 48, 96	
1	0	512fs	32, 44.1, 48	

Table 2. Set up Master clock frequency

2. Set-up Clock source

CM1 pin (SW2-4)	CM0 pin (SW2-3)	PLL	X'tal	Clock source	Input data of DAC	
0	0	ON	OFF	PLL	Optical	
0	1	OFF	ON	X'tal	Output of ADC	(Default)

Table 3. Set up Clock source
(Note) ON: Oscillation (Power-up), OFF: STOP (Power-down)

3. Set–up Audio interface format

DIF2 pin (SW2-7)	DIF1 pin (SW2-6)	DIF0 pin (SW2-5)	ADC format at Loopback	Input format of DAC	LRCK	BICK	
0	0	0	24bit, Left justified	16bit, Right justified	H/L	64fs	
0	0	1	24bit, Left justified	18bit, Right justified	H/L	64fs	
0	1	0	24bit, Left justified	20bit, Right justified	H/L	64fs	
0	1	1	24bit, Left justified	24bit, Right justified	H/L	64fs	
1	0	0	24bit, Left justified	24bit, Left justified	H/L	64fs	
1	0	1	24bit, I^2S	24bit, I^2S	L/H	64fs	(Default)

Table 4. Set up Audio interface format

■ Set-up SW1

[SW1]: Set-up AK4528. Upper is "ON"("H"), Lower is "OFF"("L")
(For further details, refer to the datasheet.)

No.	Name	Default	OFF	ON
1	P/S	ON	Serial mode	Parallel mode (Default)
2	DEM1	OFF	Set up de-emphasis (Default: OFF) (Refer to the datasheet.)	
3	DEM0	ON		
4	DFS	OFF	Normal speed (Default)	Double speed
5	DIF	ON	MSB justified	I^2S (Default)
6	CKS1	OFF	Set up Master clock frequency in case of the parallel mode (Default: 256fs) (Refer to the datasheet.)	
7	CKS0	OFF		

Table 5. Set up SW1

■ Set up Registers and Device pins of AK4528

The register setting uses the control software. (For further details, refer to the datasheet.)

1. Set up Parallel/Serial mode control

When P/S= "H", the AK4528 becomes to the parallel mode. DIF pin selects the audio interface format, and DFS, CKS1, and CKS0 pins select the master clock frequency.
When P/S= "L", the AK4528 becomes to the serial mode. The CKS1, CKS0 and DIF pins are changed to CDTI, CCLK and CSN pins respectively. The DEM1, DEM0 and DFS are ORed between pins and register respectively, so those are able to control by pins even in serial mode. When all the functions are controlled by register, DEM1, DEM0 and DFS pins should be set to "L".

2. Set up Master clock frequency

(a) In case of serial mode

CMODE bit	CKS1 bit	CKS0 bit	MCLK Normal Speed (DFS bit = "0")	MCLK Double Speed (DFS bit = "1")	
0	0	0	256fs	N/A	(Default)
0	0	1	512fs	256fs	
0	1	0	1024fs	512fs	
1	0	0	384fs	N/A	
1	0	1	768fs	384fs	

Table 6. Set up Master clock frequency in case of serial mode

(b) In case of parallel mode

CKS1 Pin (SW1-6)	CKS0 Pin (SW1-7)	MCLK Normal Speed (DFS pin = "L")	MCLK Double Speed (DFS pin = "H")	
L	L	256fs	N/A	(Default)
L	H	512fs	256fs	
H	L	384fs	N/A	
H	H	1024fs	512fs	

Table 7. Set up Master clock frequency in case of parallel mode

3. Set up Audio interface format

(a) In case of the serial mode

Mode	DIF2 bit	DIF1 bit	DIF0 bit	SDTO	SDTI	LRCK	BICK	
0	0	0	0	24bit, MSB justified	16bit, LSB justified	H/L	≥ 32fs	
1	0	0	1	24bit, MSB justified	20bit, LSB justified	H/L	≥ 40fs	
2	0	1	0	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	(Default)
3	0	1	1	24bit, I^2S	24bit, I^2S	L/H	≥ 48fs	
4	1	0	0	24bit, MSB justified	24bit, LSB justified	H/L	≥ 48fs	

Table 8. Set up Audio interface format in case of serial mode

(b) In case of parallel mode

Mode	DIF Pin (SW1-5)	SDTO	SDTI	LRCK	BICK	
2	0	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	
3	1	24bit, I^2S	24bit, I^2S	L/H	≥ 48fs	(Default)

Table 9. Set up Audio interface format in case of parallel mode

■ Set up Registers of AK4353 (DIT).

The register setting uses the control software. (For further details, refer to the datasheet)

1. Set up Master clock frequency

CKS2 bit	CKS1 bit	CKS0 bit	DFS1, DFS0 bit		
			"1", "1" (Half speed)	"0", "0" (Normal speed)	"0", "1" (Double speed)
0	0	0	512fs	256fs (Default)	128fs
0	0	1	256fs	256fs	256fs
0	1	0	768fs	384fs	192fs
0	1	1	384fs	384fs	384fs
1	0	0	1024fs	512fs	256fs
1	0	1	512fs	512fs	N/A
1	1	0	1536fs	768fs	384fs
1	1	1	768fs	768fs	N/A

Table 10. Set up Master clock frequency
(Note) DFS1, DFS0="1", "0": Reserved (Not defined)

2. Set up Audio interface format

Mode	DIF2 bit	DIF1 bit	DIF0 bit	SDTI	L/R	BICK	
0	0	0	0	16bit, LSB justified	H/L	≥32fs	
1	0	0	1	18bit, LSB justified	H/L	≥36fs	
2	0	1	0	20bit, LSB justified	H/L	≥40fs	
3	0	1	1	24bit, LSB justified	H/L	≥48fs	
4	1	0	0	24bit, MSB justified	H/L	≥48fs	
5	1	0	1	I^2S	L/H	≥48fs	(Default)
6	1	1	0	Reserved			
7	1	1	1	Reserved			

Table 11. Set up Audio interface format

■ Set up Jumper pins

JP1 (RX): Selection of Optical connector or BNC connector
TORX176 (Default): Biphase signal is supplied to AK4112B by optical connector.
COAX : Biphase signal is supplied to AK4112B by BNC connector.

JP2 (GND): Separate/Connect AGND and DGND
Open : Separate AGND and DGND.
Short (Default) : Connect AGND and DGND.

■ The indication content for LED

[LE1] (ERF) : AK4112B unlock and parity error output.
[LE2] (FS96) : AK4112B 96kHz sampling detect.
[LE3] (AUTO): AK4112B AC-3/MPEG detects.
[LE4] (V) : Validity.

■ The function of the toggle SW

[SW3]: Resets the AK4528, AK4112B and AK4353. Keep “H” during normal operation.

■ Serial control mode

The AK4528 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CR-I/F) with PC by 10-wire flat cable packed with the AKD4528.

Take care of the direction of connector. There is a mark at pin#1.
The pin layout of PORT1 is as Figure 4.

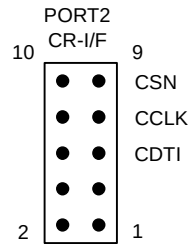


Figure 4. PORT2 pin layout

*AKM assumes no responsibility for the trouble when using the circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4528 according to previous term.

2. Connect IBM-AT compatible PC with AKD4528 by 10-line type flat cable (packed with AKD4528). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4528 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive, and double-click the icon of "akd4528.exe"and "akd4528_dit.exe", and set up the control program.
   akd4528.exe: AK4528 control program
   akd4528_dit.exe: AK4353 (DIT) control program

5. Then evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A).
2. [Write default]: Initialize the registers.
3. [All Write]: Write all registers data that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate ATT

This is a dialog corresponding to address: 04H, 05H of AK4528, and address: 03H, 04H of AK4353.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to register by this interval.
Step Box: Data changes by this step.
Mode Select Box:

With checking this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

Without checking this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data to the file. The extension of file name is “akr”.

(Operation flow)

(1) Click [Save] Button.

(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved to the file by [Save] is written to register. The file type is the same as [Save].

(Operation flow)

(1) Click [Open] Button.

(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

Set the control sequence.

Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step. This sequence can be saved and opened by [Save] and [Open] button on the [Function3] window. The extension of file name is “aks”.

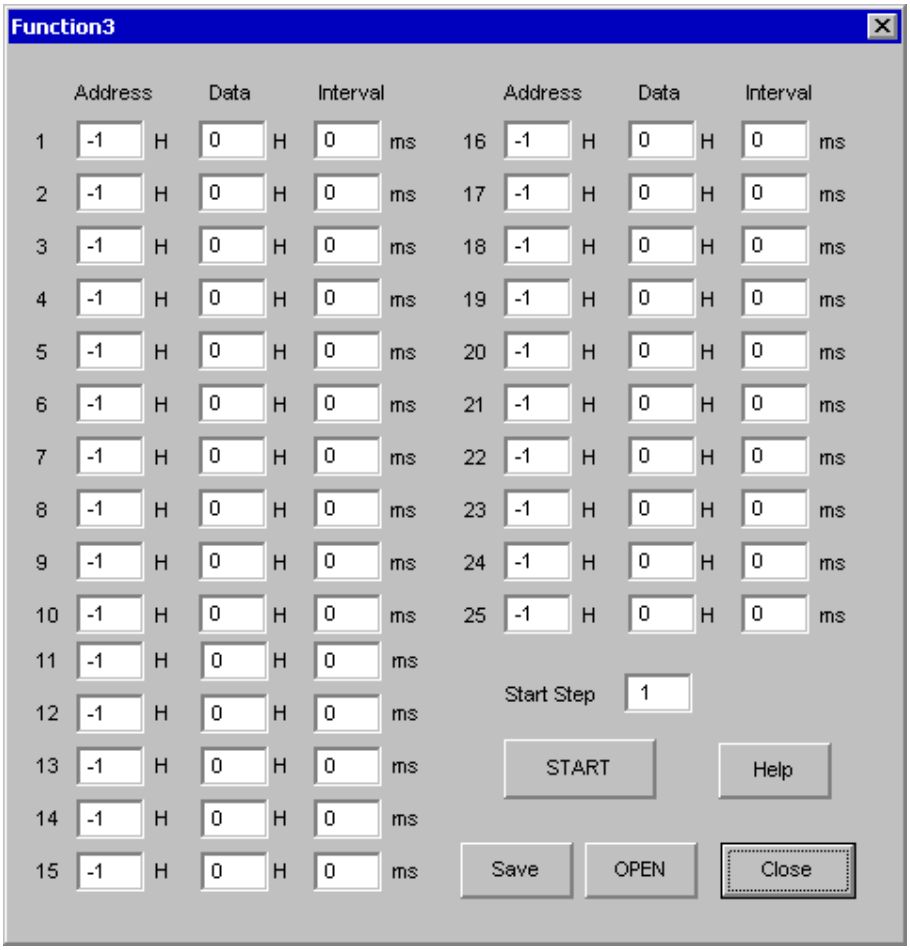


Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

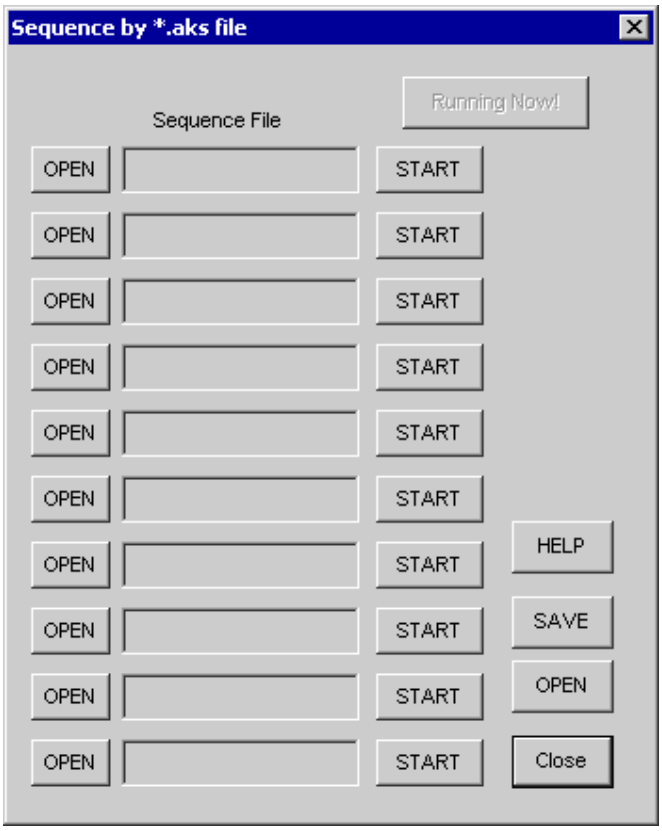


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 3.

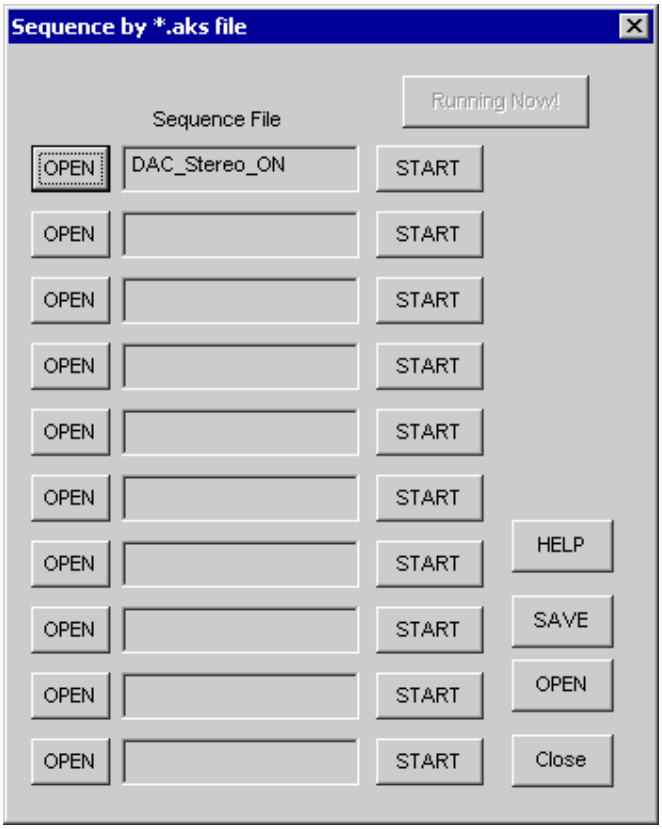


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The sequence file names can assign be saved. The file name is *.ak4.

[OPEN]: The sequence file names assign that are saved in *.ak4 are loaded.

6-3. Note

(1) [Function4] doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 4opens.

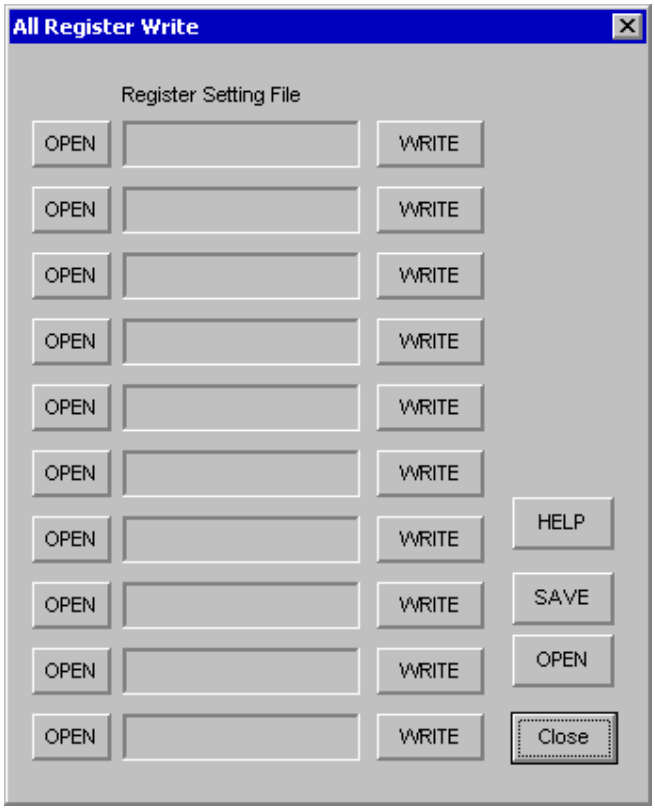


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The register setting file names assign can be saved. The file name is *.ak5.

[OPEN]: The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

AK4528 Measurement Results

Conditions:
Measurement unit: Audio Precision System Two Cascade
MCLK: 256fs
BICK: 64fs
LRCK: 44.1kHz(DIR or DIT), or 96kHz(DIR or DIT)
Power supply: VA=VD=VT=5.0V
Interface: DIT or DIR
Temperature: Room Temp.

1. ADC

1-1. fs = 44.1kHz

Parameter	Input signal	BW, filter	Results		unit
			Lch	Rch	
S/(N+D)	1kHz, -0.5dB	20kHz	98.4	98.2	dB
Dynamic range	1kHz, -60dB	20kHz	102.6	102.6	dB
		20kHz, A-weighted	107.4	107.5	dB
S/N	off	20kHz	102.8	102.8	dB
		20kHz, A-weighted	107.5	107.5	dB

1-2. fs=96kHz

Parameter	Input signal	BW, filter	Results		unit
			Lch	Rch	
S/(N+D)	1kHz, -0.5dB	fs/2	91.4	92.8	dB
Dynamic range	1kHz, -60dB	fs/2	99.8	99.9	dB
		fs/2, A-weighted	108.3	108.5	dB
S/N	off	fs/2	100.0	100.8	dB
		fs/2, A-weighted	108.9	109.0	dB

DAC

2-1. fs=44.1kHz

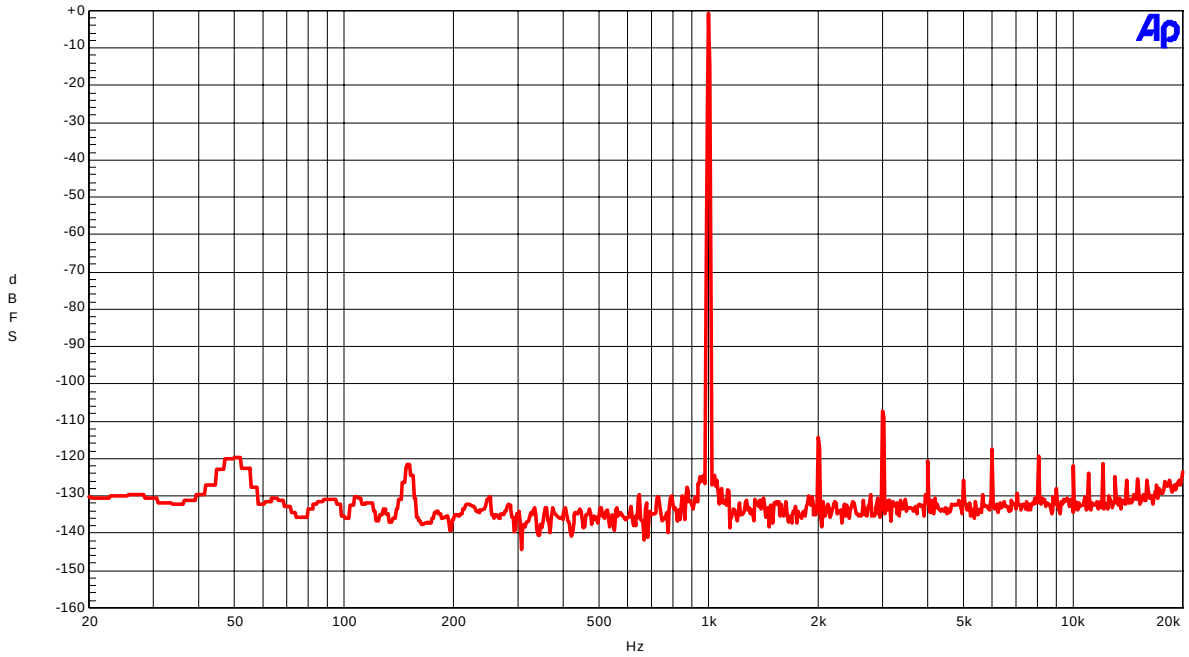
Parameter	Input signal	BW, filter	Results		unit
			Lch	Rch	
S/(D+N)	1kHz, 0dBFS	20kHz	93.7	94.5	dB
Dynamic range	1kHz, -60dBFS	20kHz	108.0	108.0	dB
		22kHz, A-weighted	110.7	110.6	dB
S/N	"0" data	20kHz	108.2	108.0	dB
		22kHz, A-weighted	110.9	110.7	dB

2-2. fs=96kHz

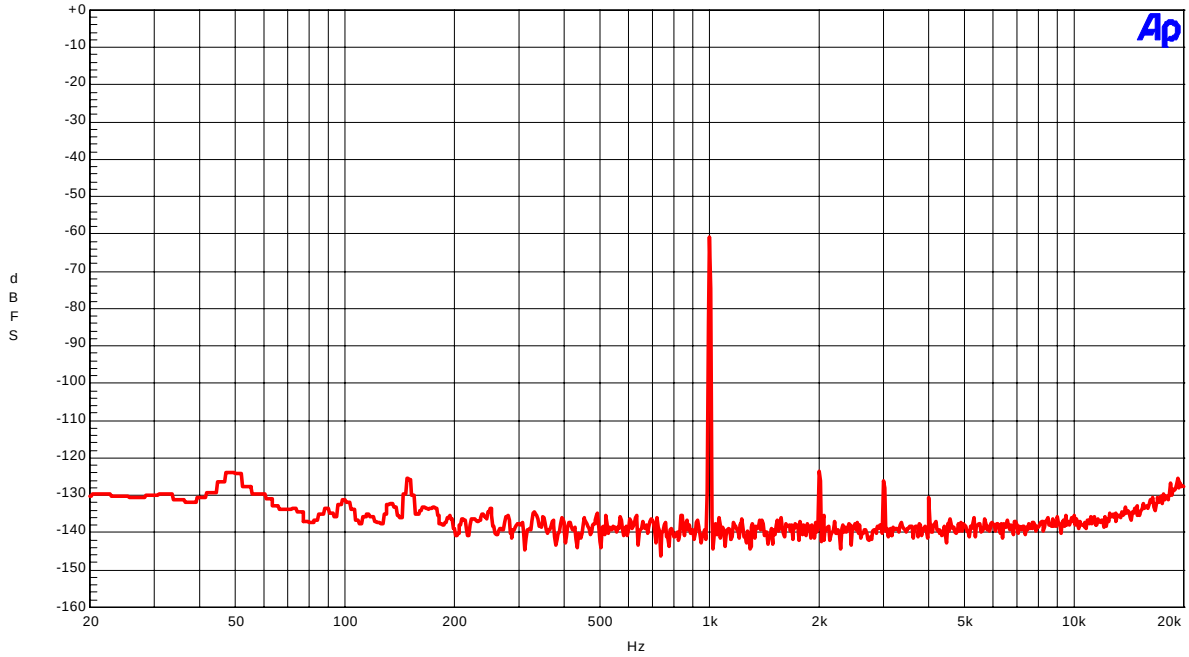
Parameter	Input signal	BW, filter	Results		unit
			Lch	Rch	
S/(N+D)	1kHz, 0dBFS	40kHz	91.2	91.8	dB
Dynamic range	1kHz, -60dBFS	40kHz	104.8	104.9	dB
		80kHz, A-weighted	110.0	110.0	dB
S/N	"0" data	40kHz	104.9	104.8	dB
		80kHz, A-weighted	110.2	109.9	dB

1. ADC

(fs=44.1kHz)

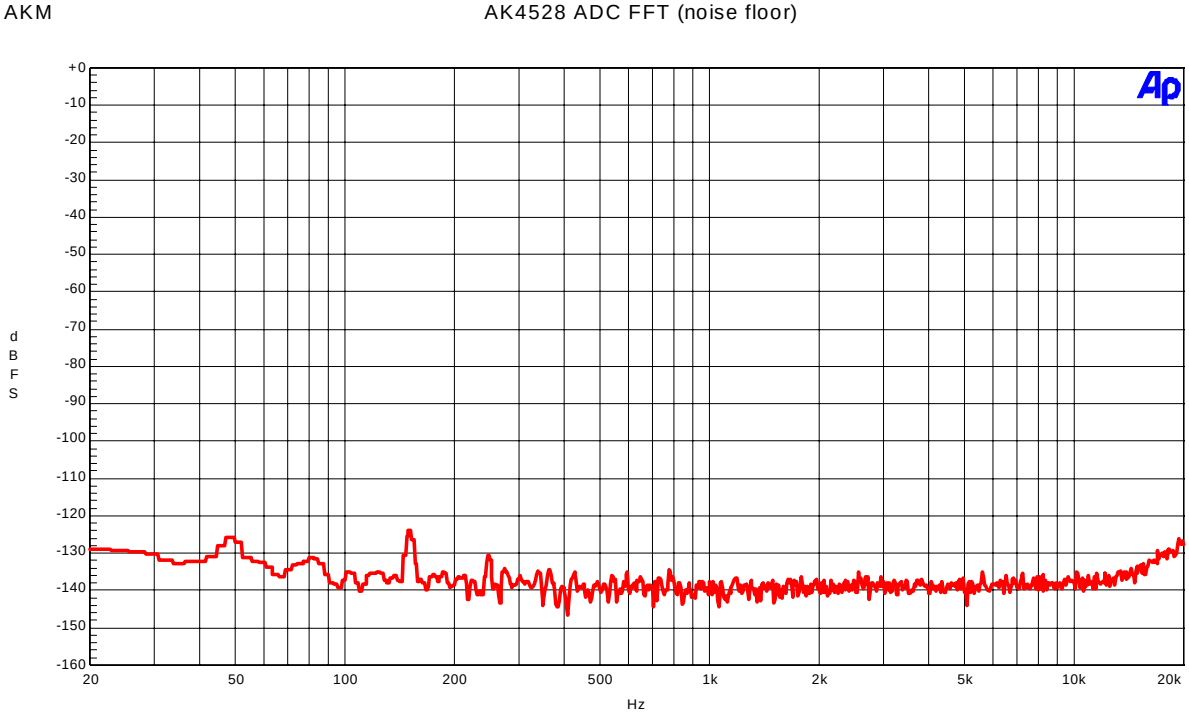


FFT (Input Level = -0.5dBFS, fin=1kHz)



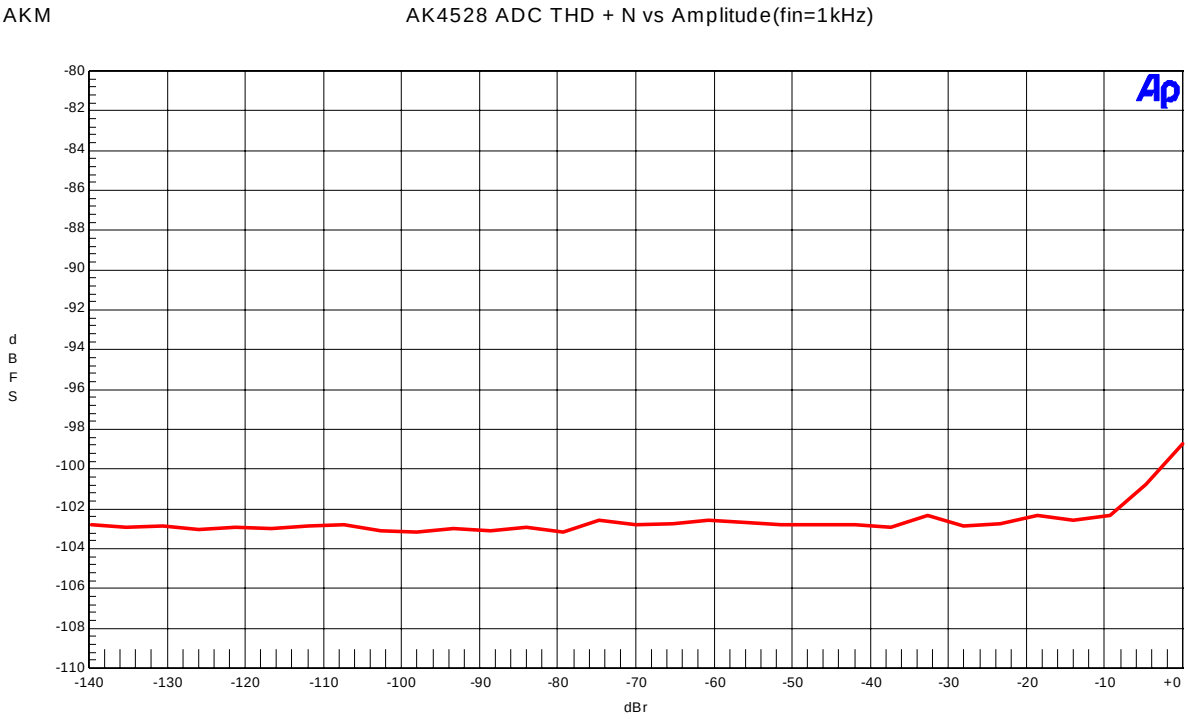
FFT (Input Level = -60dBFS, fin=1kHz)

(fs=44.1kHz)

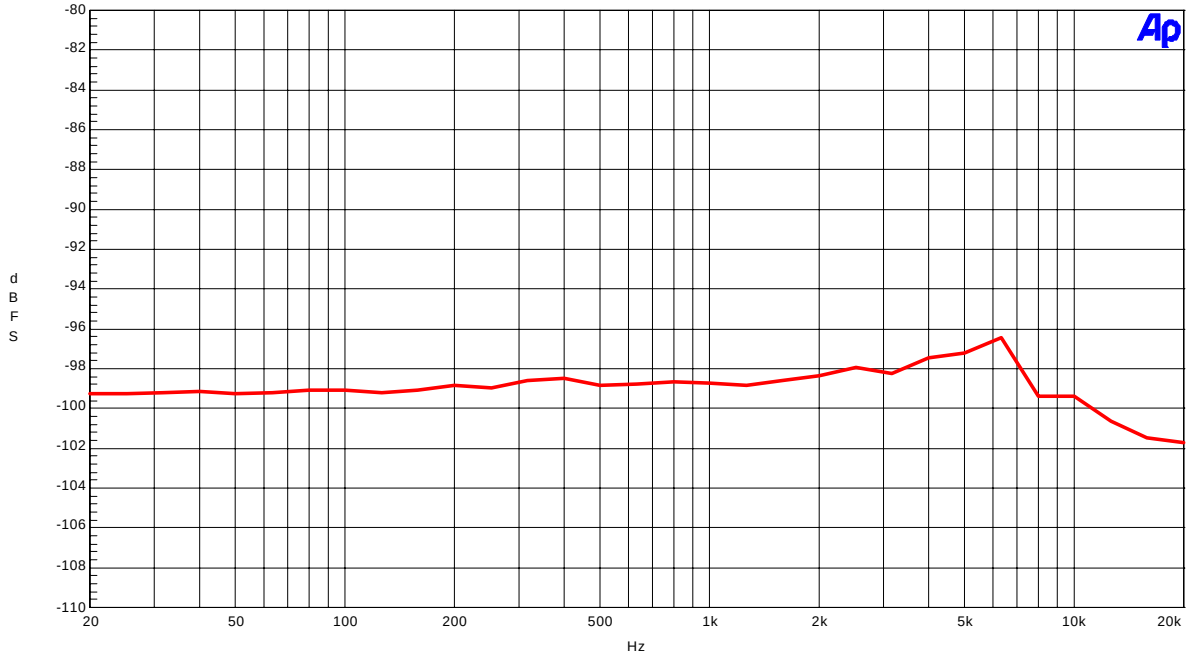


FFT (noise floor)

(fs=44.1kHz)

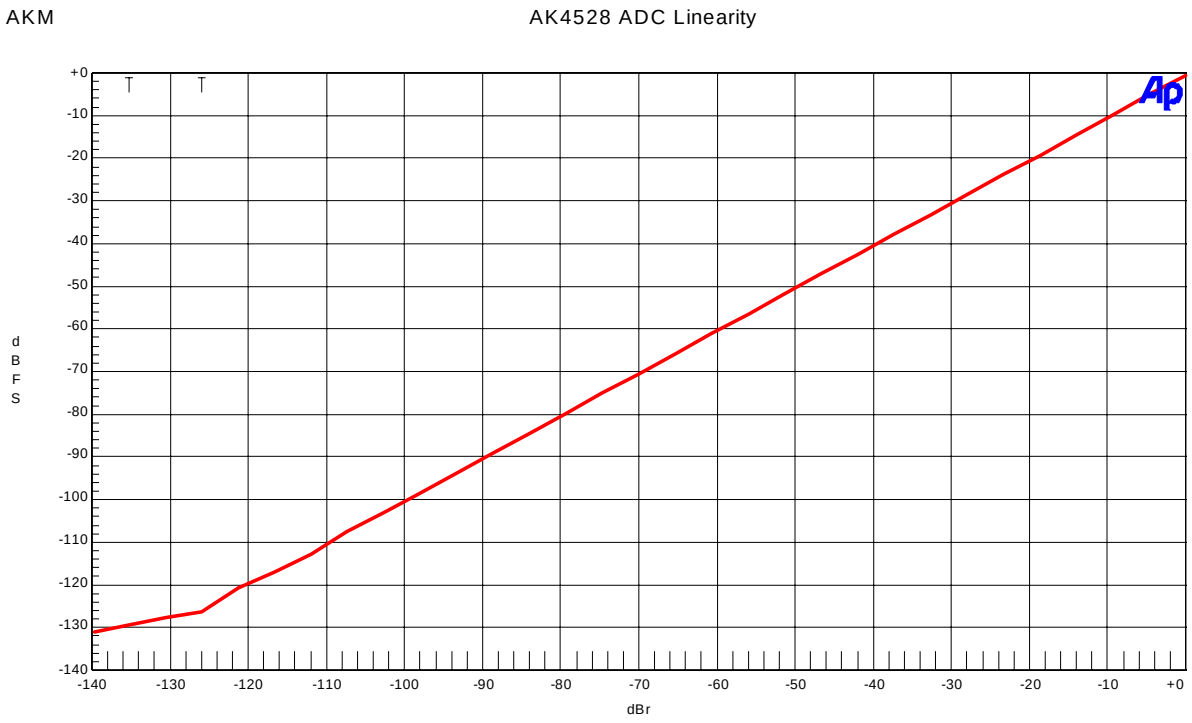


THD + N vs Amplitude (fin=1kHz)

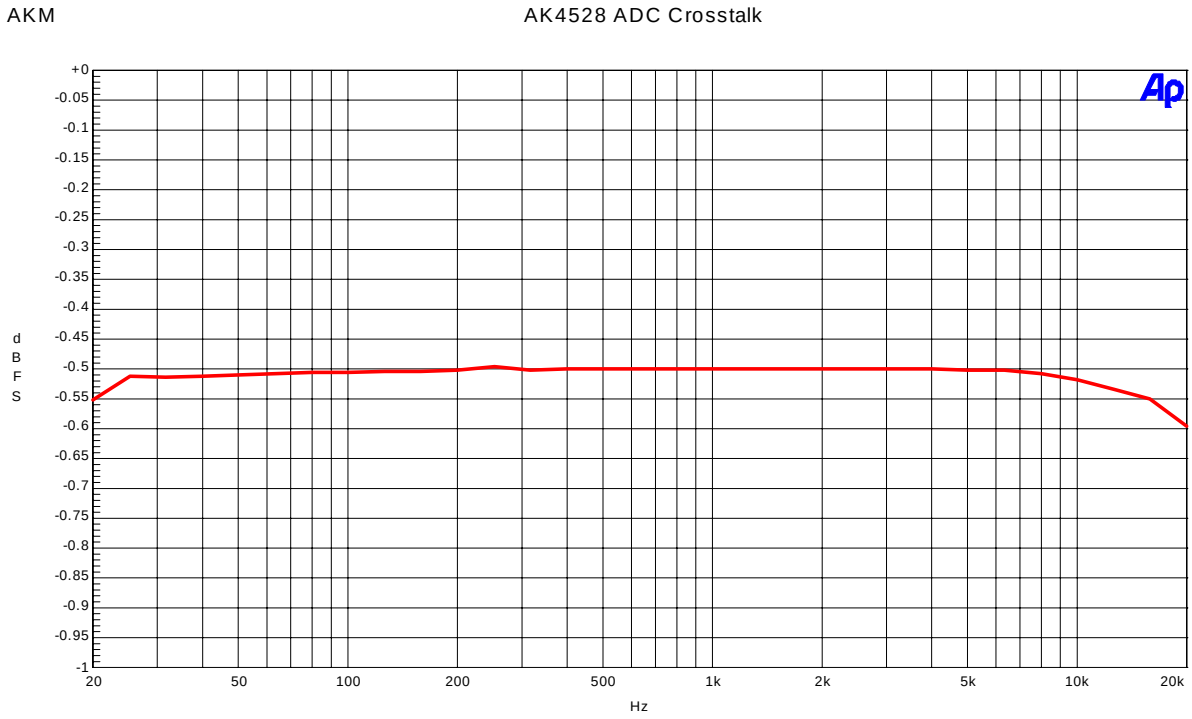


THD + N vs Input Frequency (Input Level = -0.5dBFS)

(fs=44.1kHz)

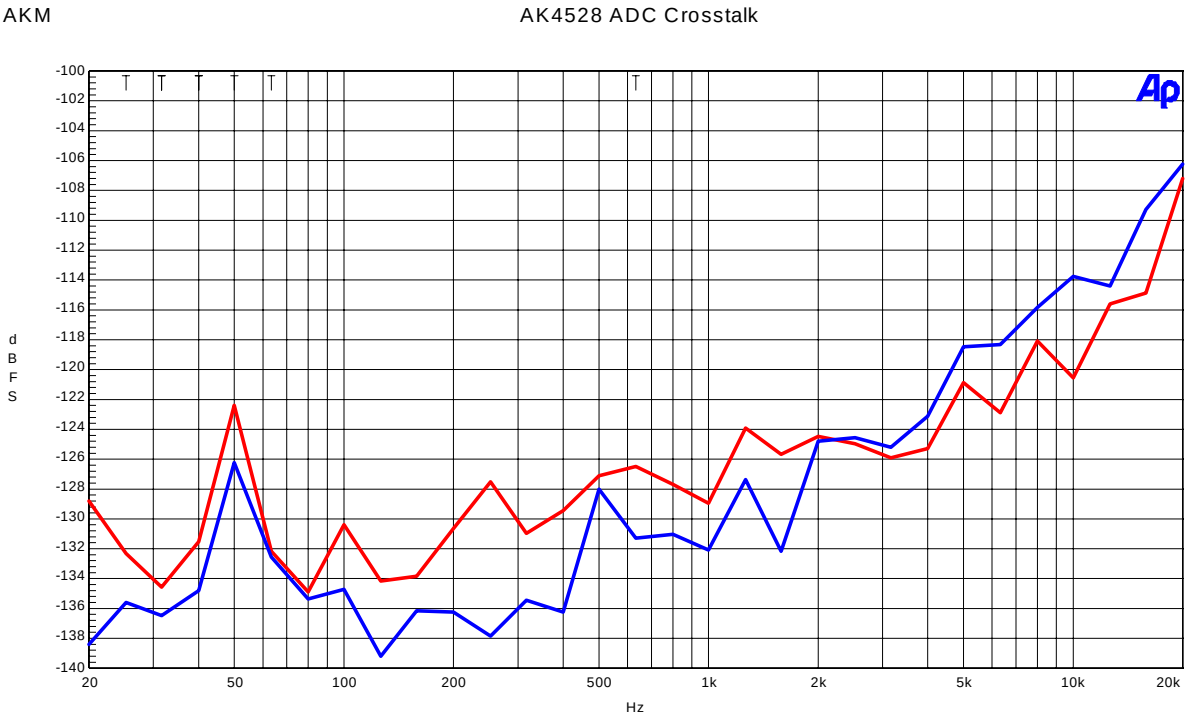


Linearity (fin=1kHz)



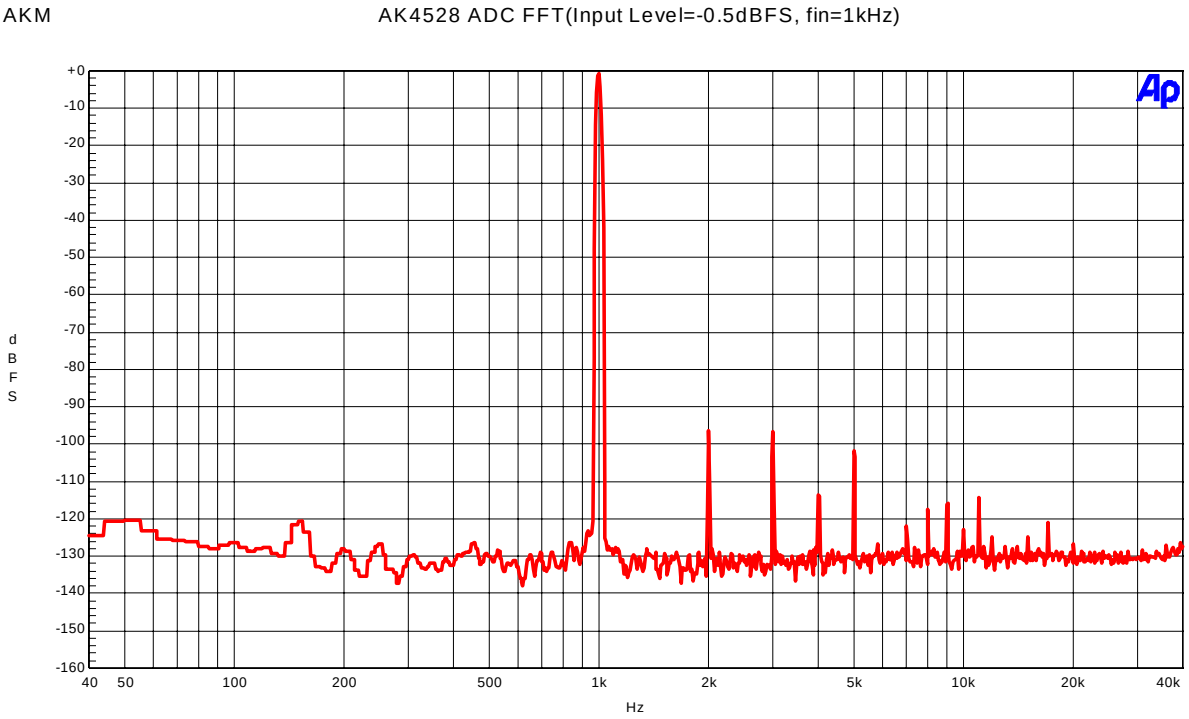
Frequency Response (Input Level=1kHz)

(fs=44.1kHz)

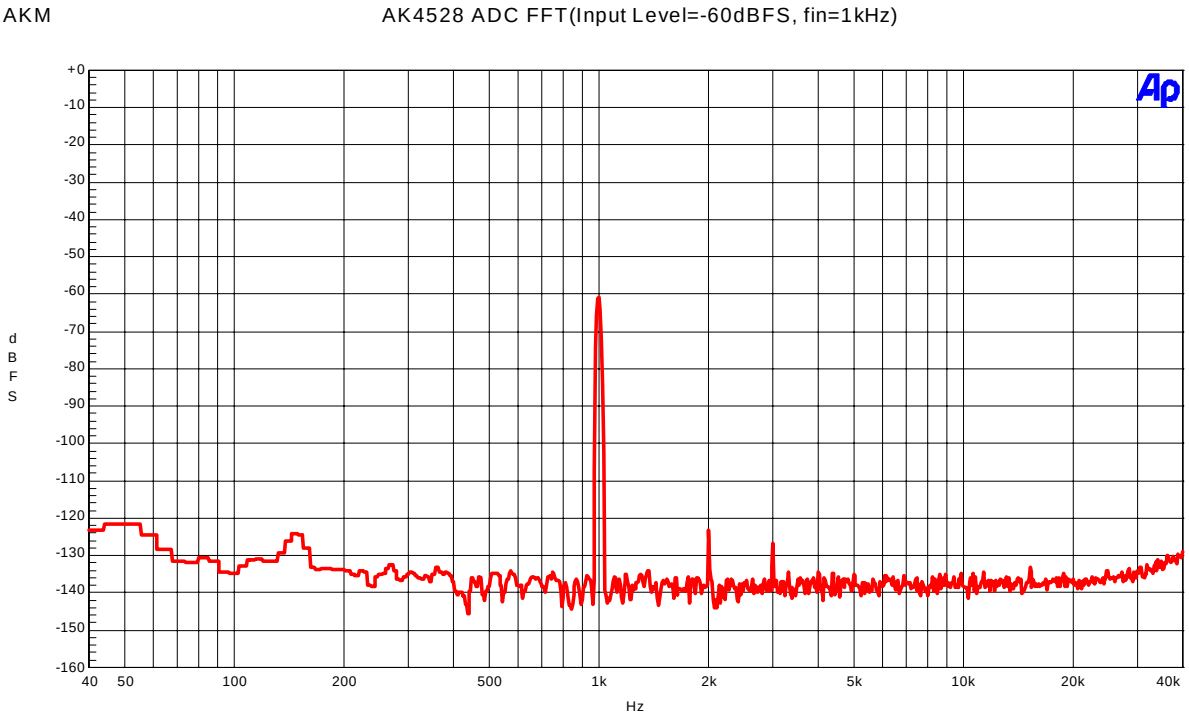


Crosstalk

(fs=96kHz)

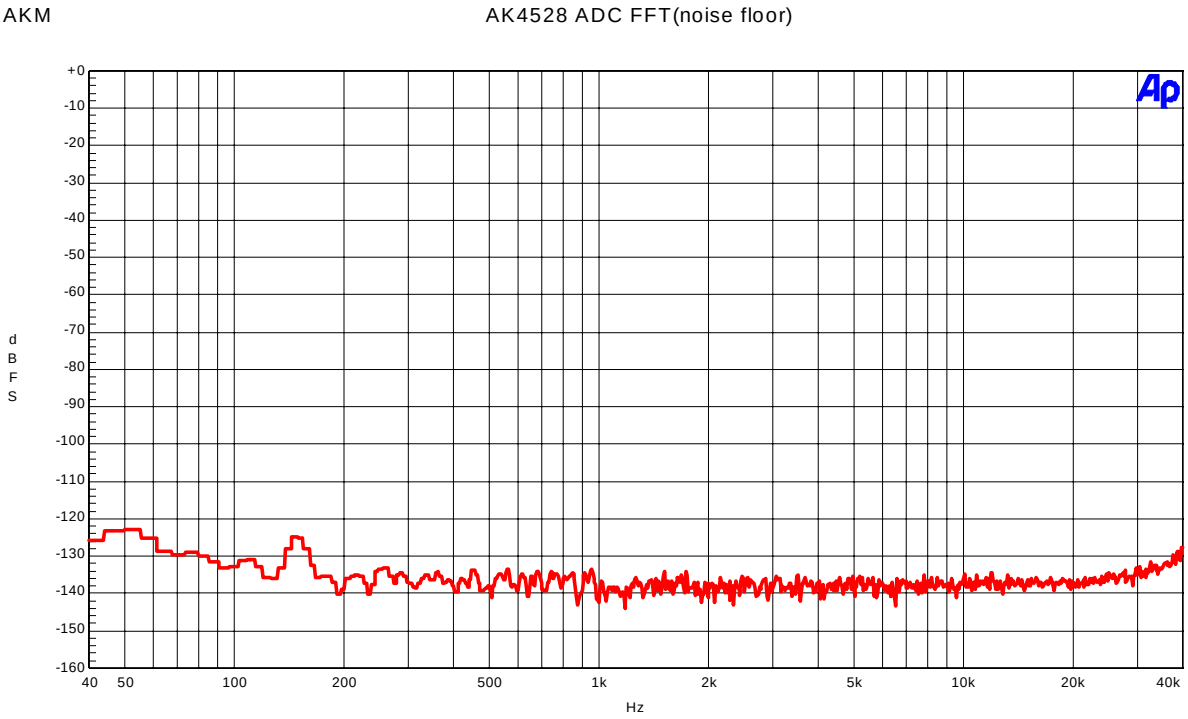


FFT (Input Level = -0.5dBFS, fin=1kHz)



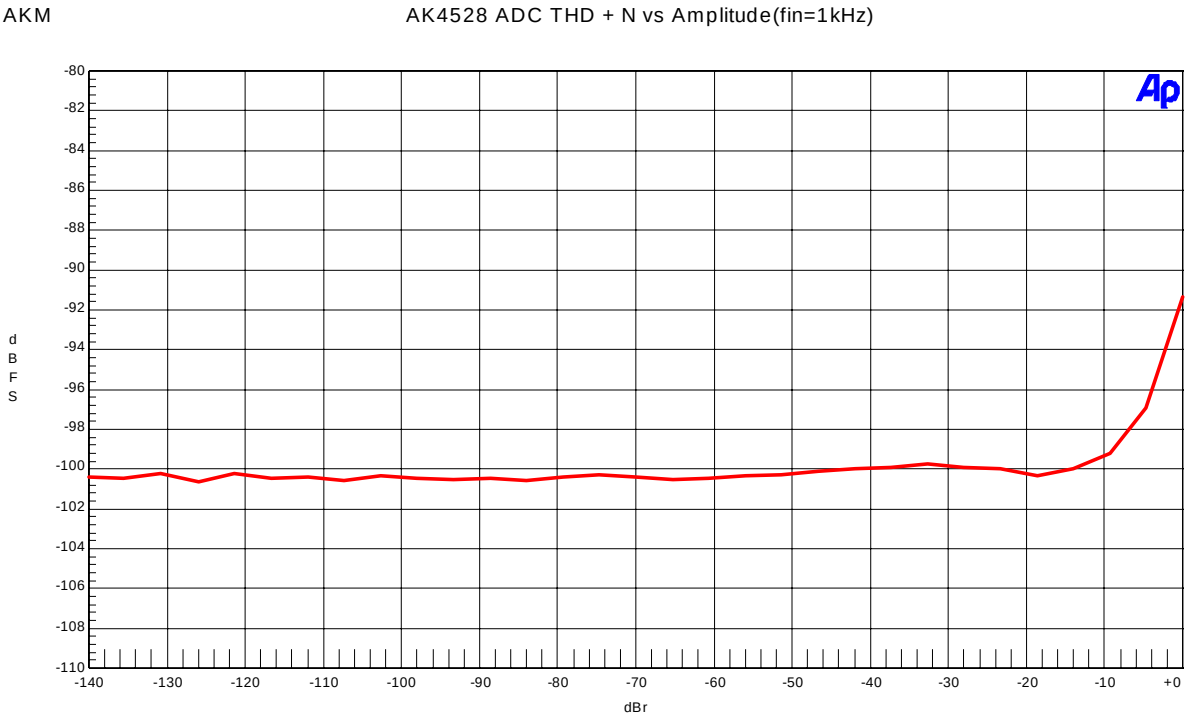
FFT (Input Level = -60dBFS, fin=1kHz)

(fs=96kHz)

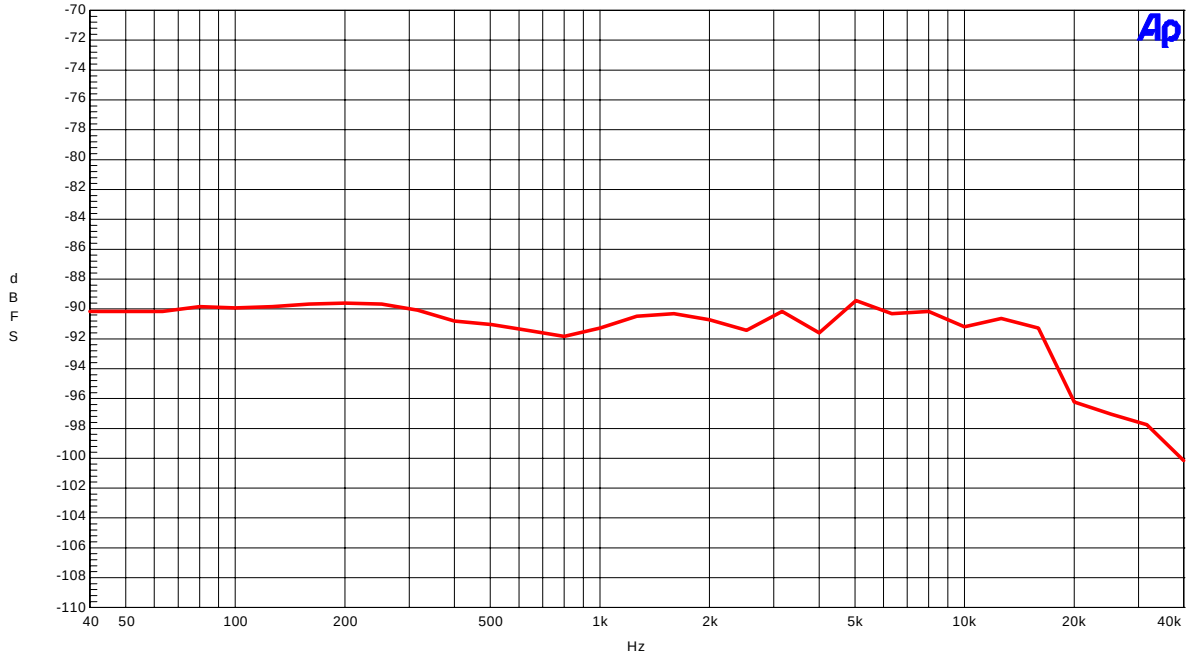


FFT (noise floor)

(fs=96kHz)

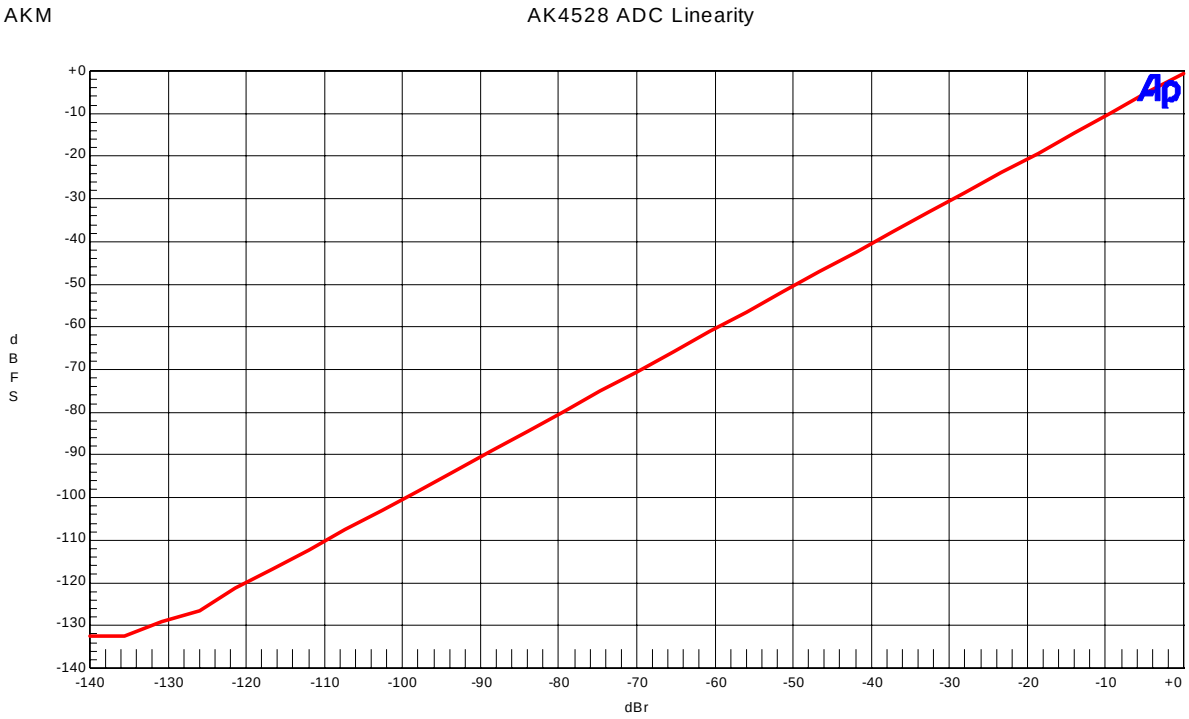


THD + N vs Amplitude (fin=1kHz)

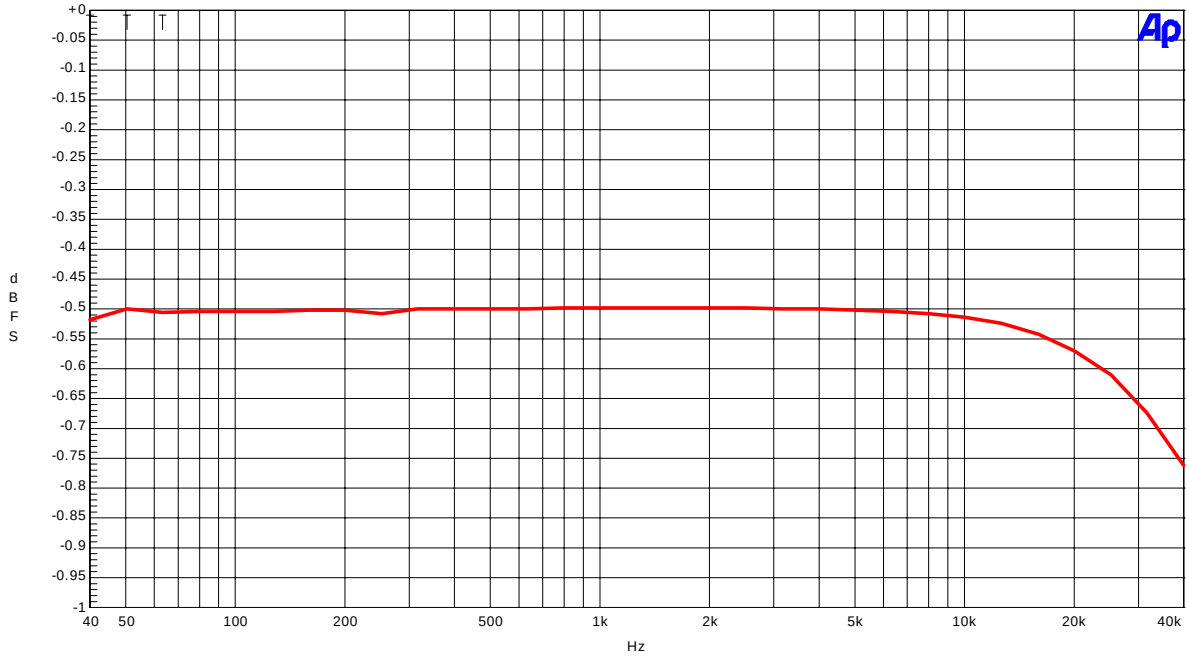


THD + N vs Input Frequency (input Level=-0.5dBFS)

(fs=96kHz)

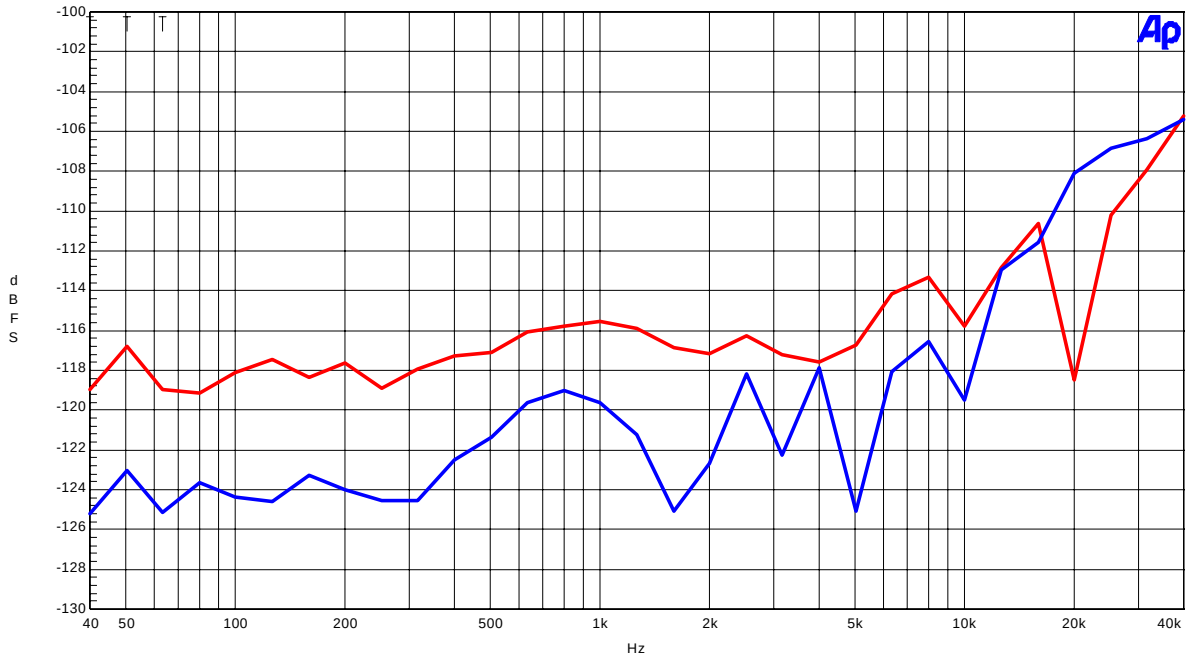


Linearity (fin=1kHz)



Frequency Response (Input Level=-0.5dBFS)

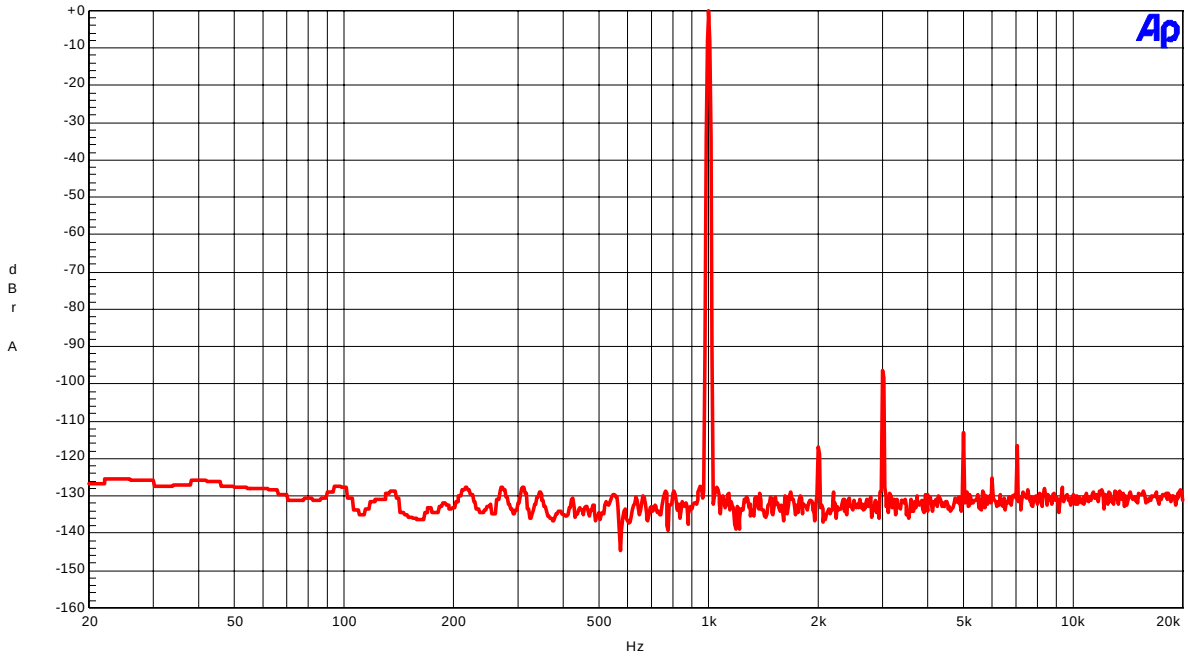
(fs=96kHz)



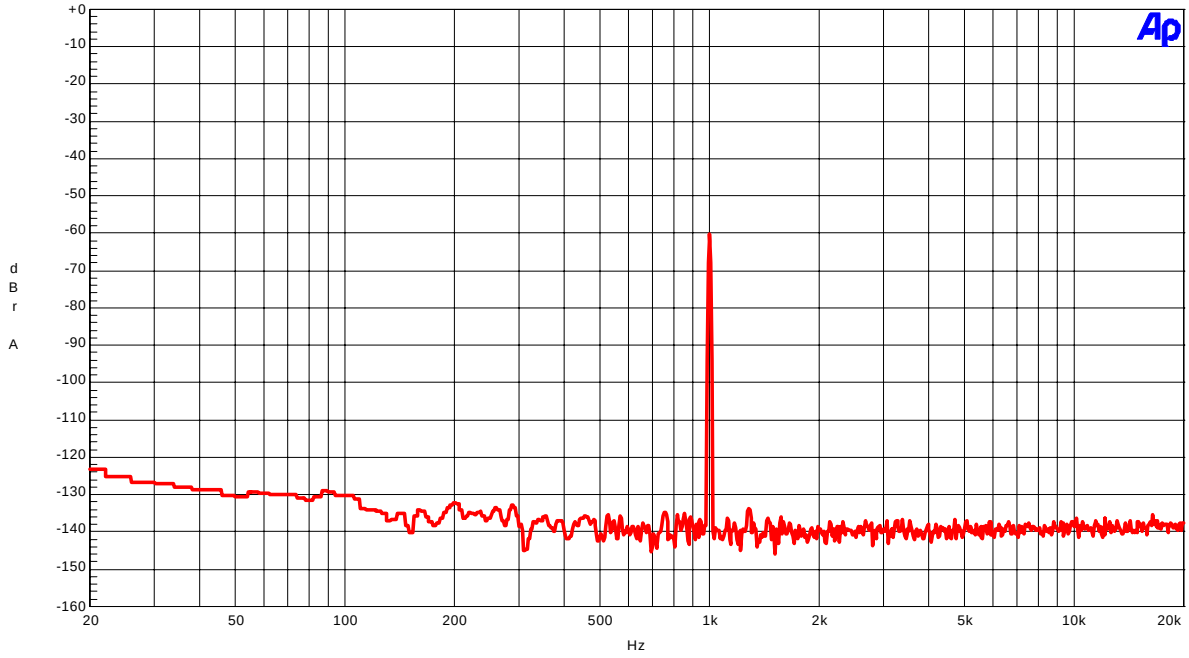
Crosstalk

2. DAC

(fs=44.1kHz)

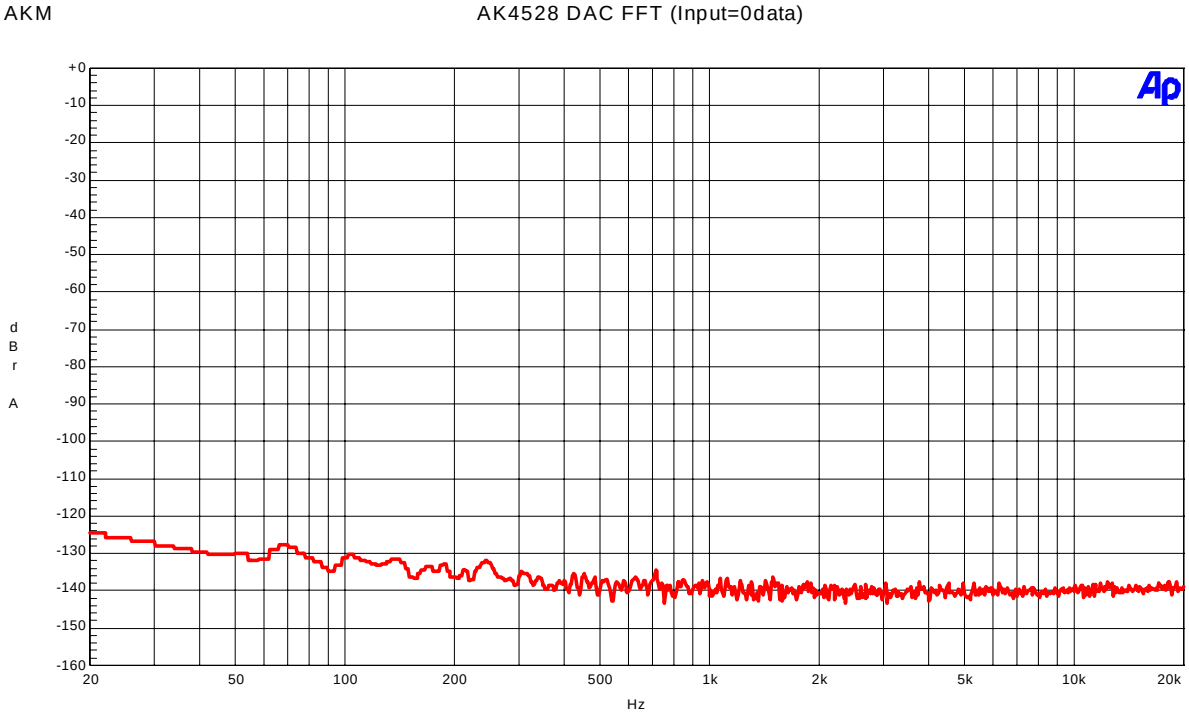


FFT (Input Level=0dBFS, fin=1kHz)

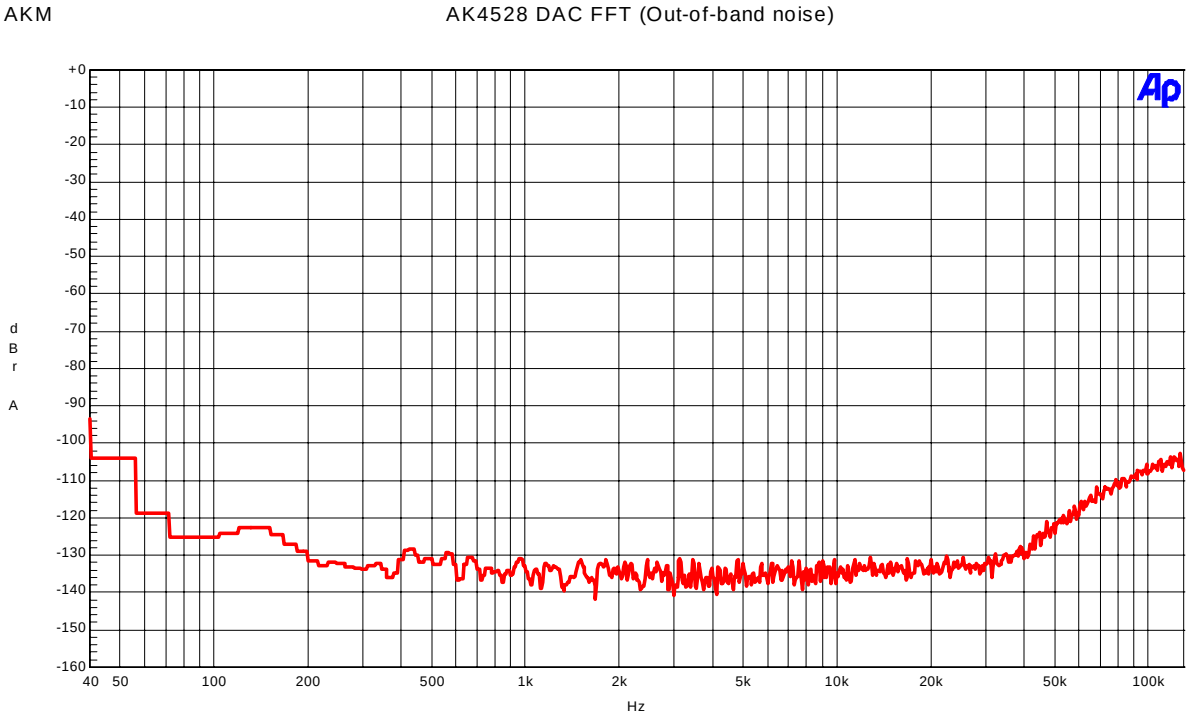


FFT (Input Level=-60dBFS, fin=1kHz)

(fs=44.1kHz)



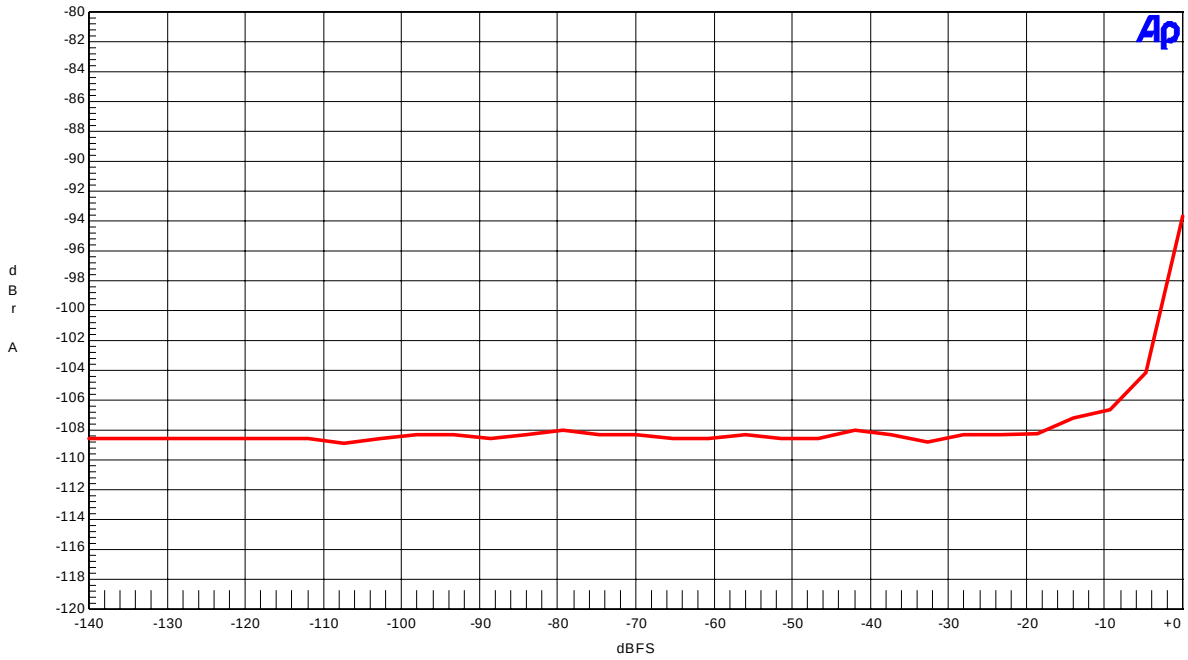
FFT (Input = “0”data)



FFT (out-of-band noise)

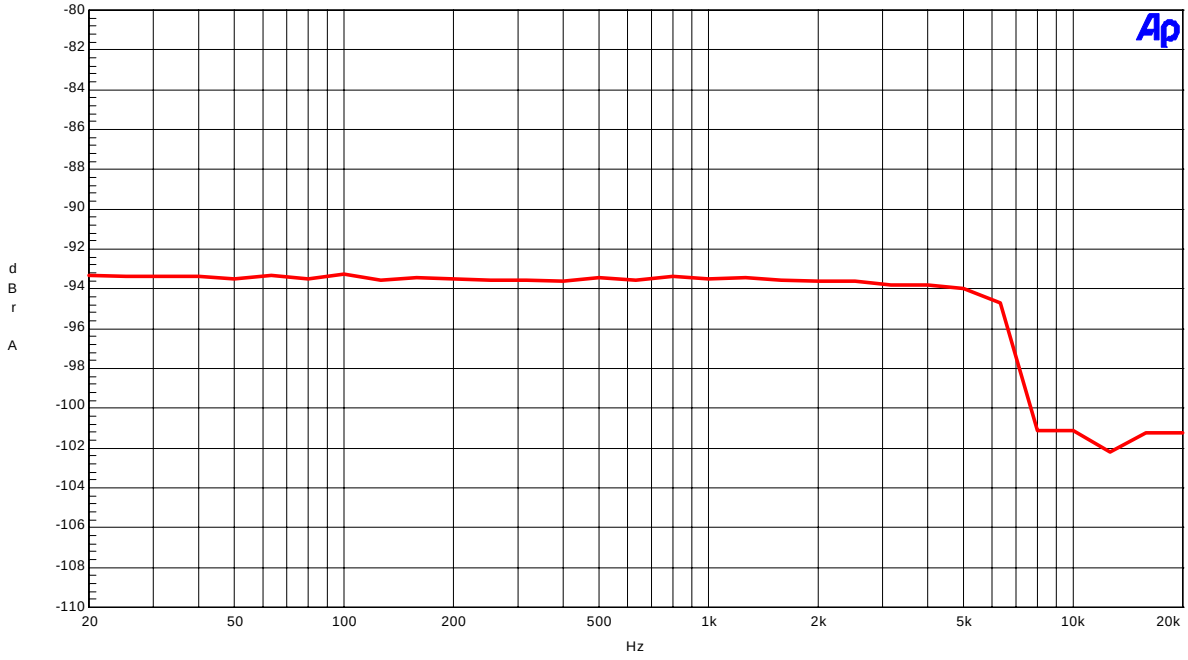
(fs=44.1kHz)

AKM AK4528 DAC THD + N vs Amplitude(fin=1kHz)



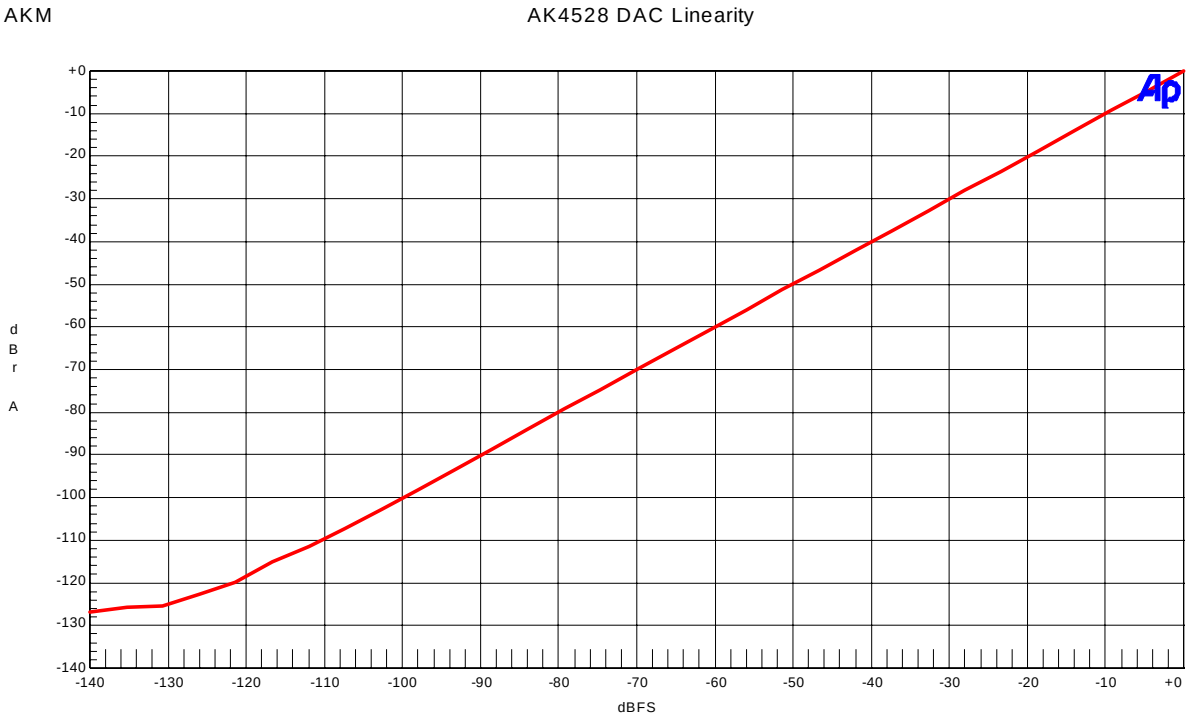
THD + N vs Amplitude (fin=1kHz)

AKM AK4528 DAC THD + N vs Input Frequency (Input Level=0dBFS)

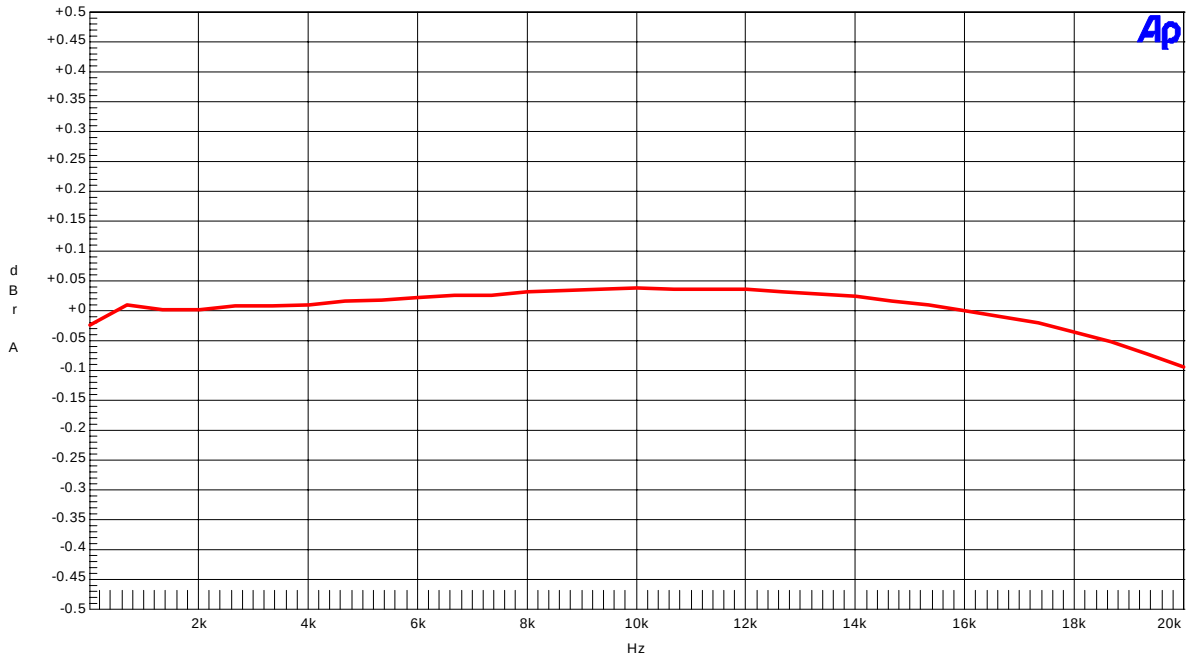


THD + N vs Input Frequency (Input Level=0dBFS)

(fs=44.1kHz)

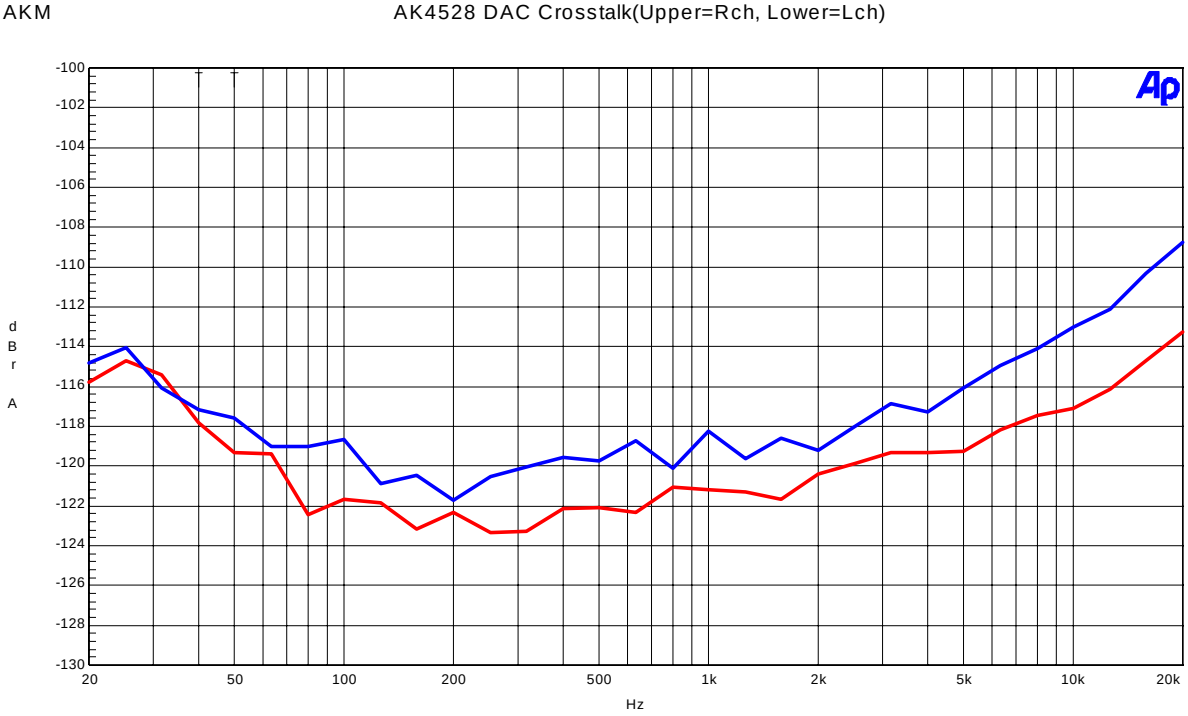


Linearity (fin=1kHz)



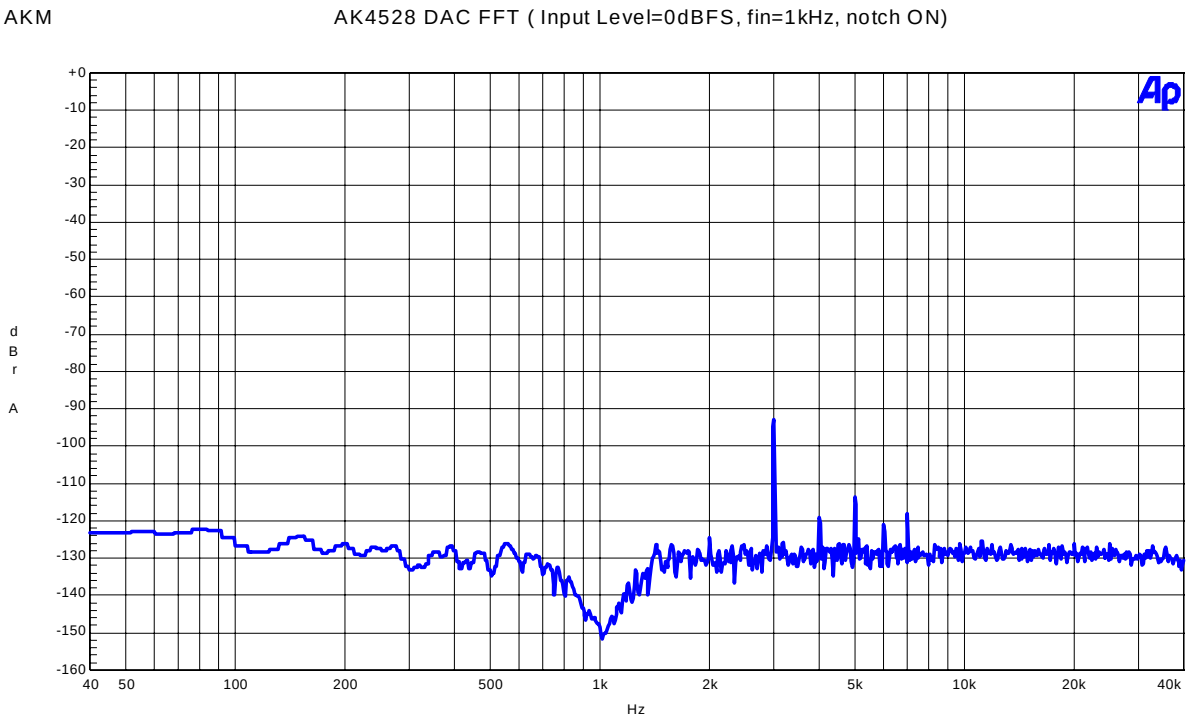
Frequency Response (Input Level = 0dBFS)

(fs=44.1kHz)

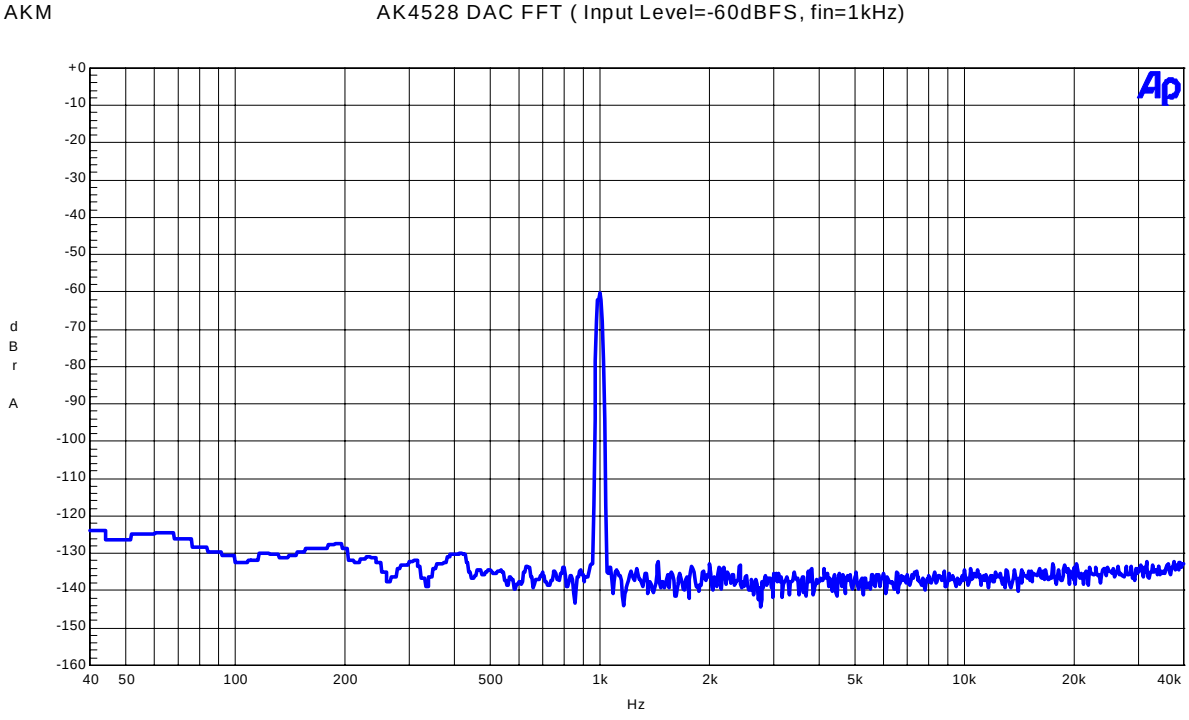


Crosstalk

(fs=96kHz)

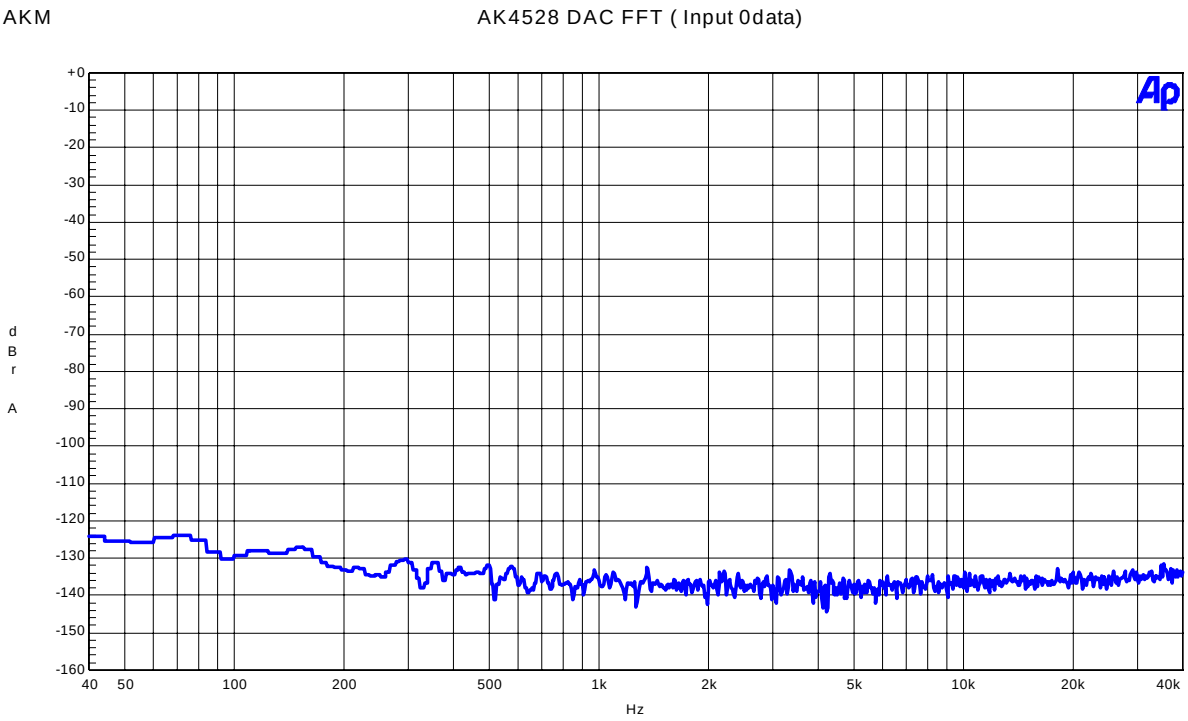


FFT (Input Level=0dBFS, fin=1kHz)



FFT (Input Level=-60dBFS, fin=1kHz)

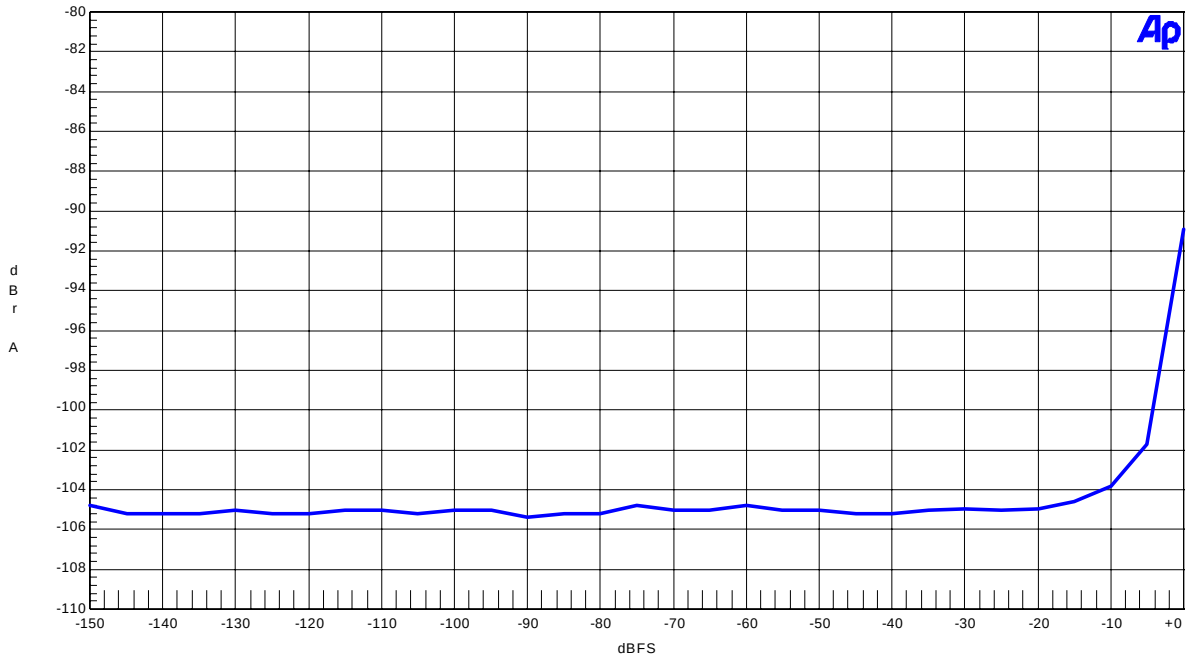
(fs=96kHz)



FFT (Input = “0”data)

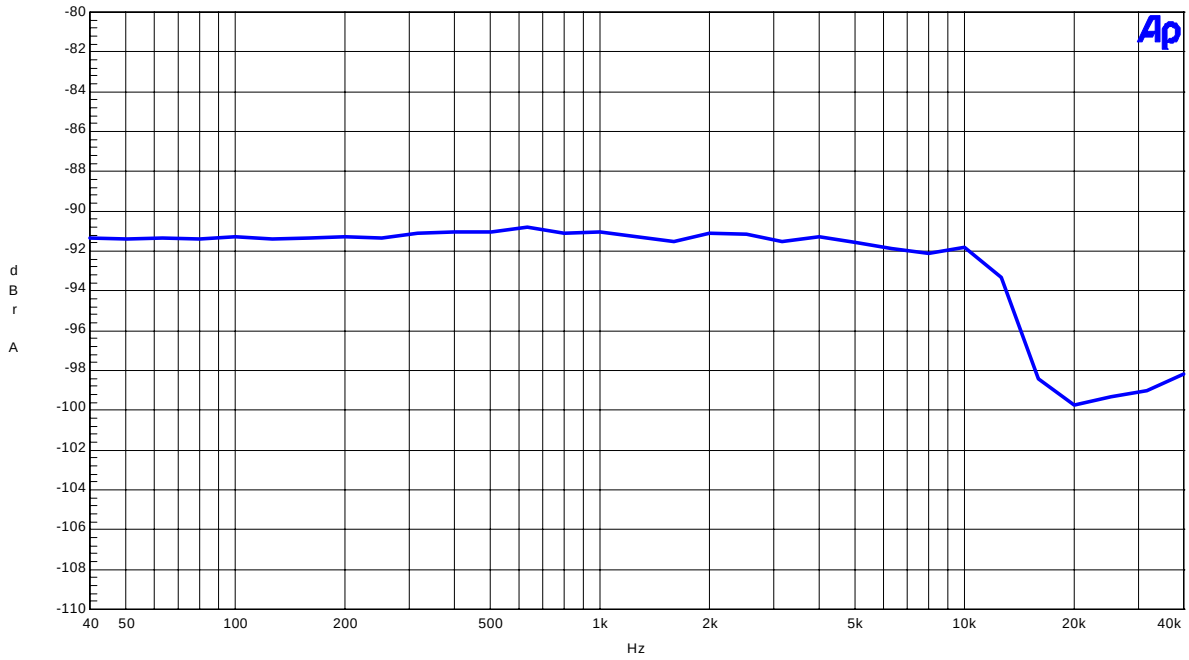
(fs=96kHz)

AKM AK4528 DAC THD + N vs Amplitude(fin=1kHz)



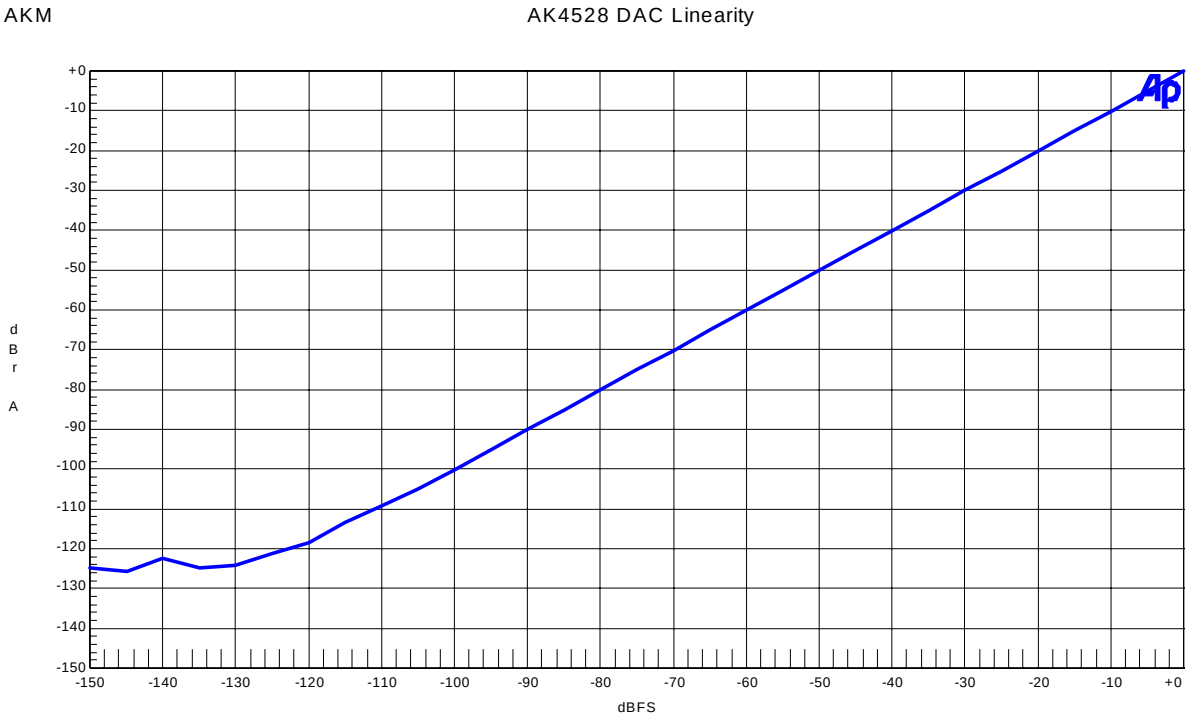
THD + N vs Amplitude (fin=1kHz)

AKM AK4528 DAC THD + N vs Input Frequency (Input Level=0dBFS)

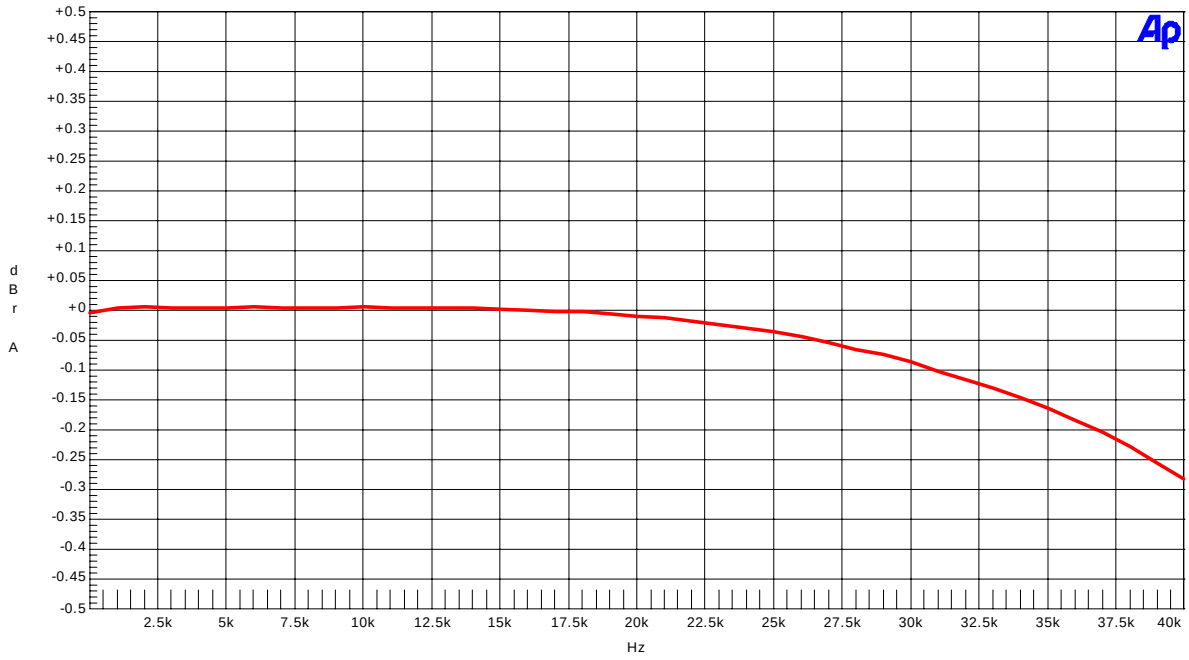


THD + N vs Input Frequency (Input Level=0dBFS)

(fs=96kHz)

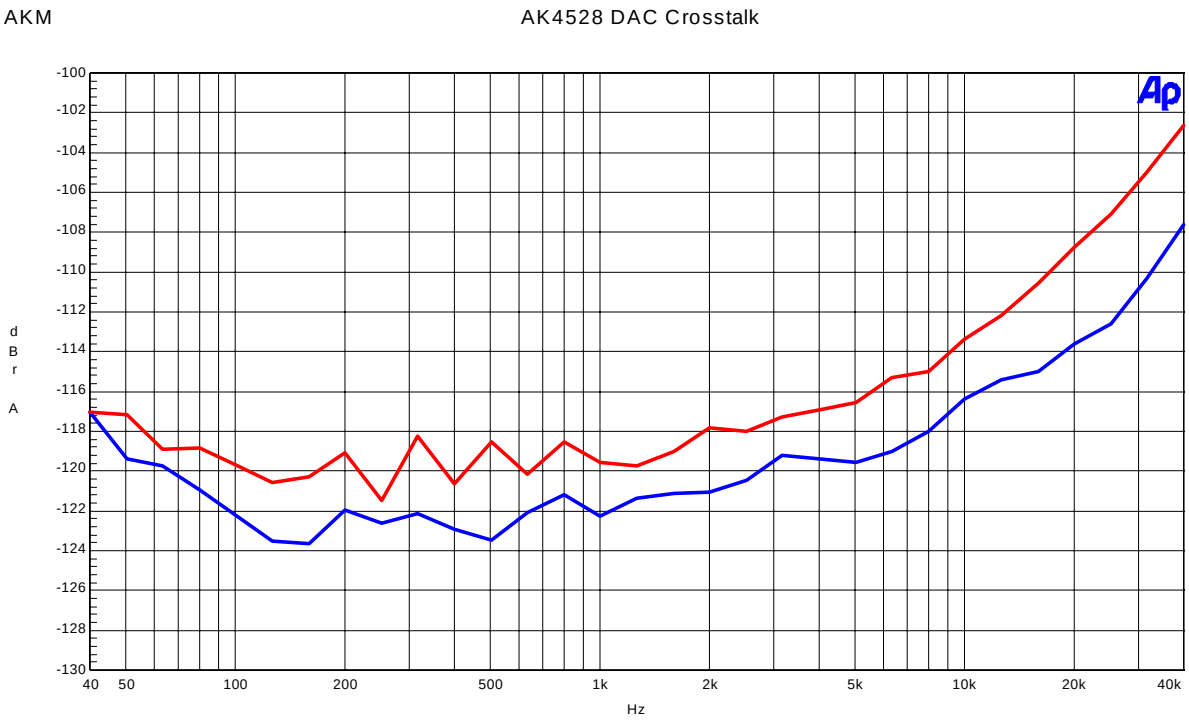


Linearity (fin=1kHz)



Frequency Response (Input Level=0dBFS)

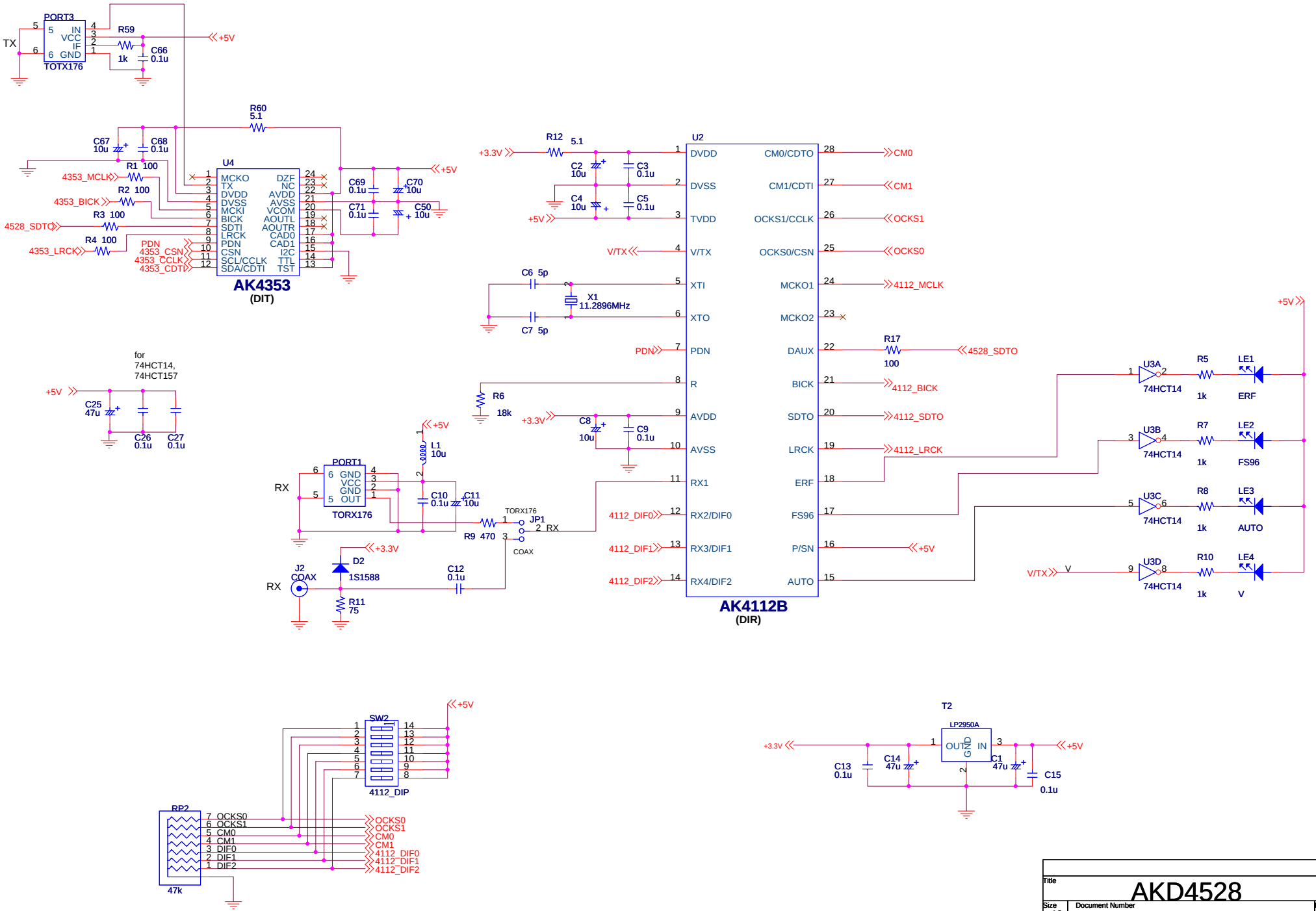
(fs=96kHz)



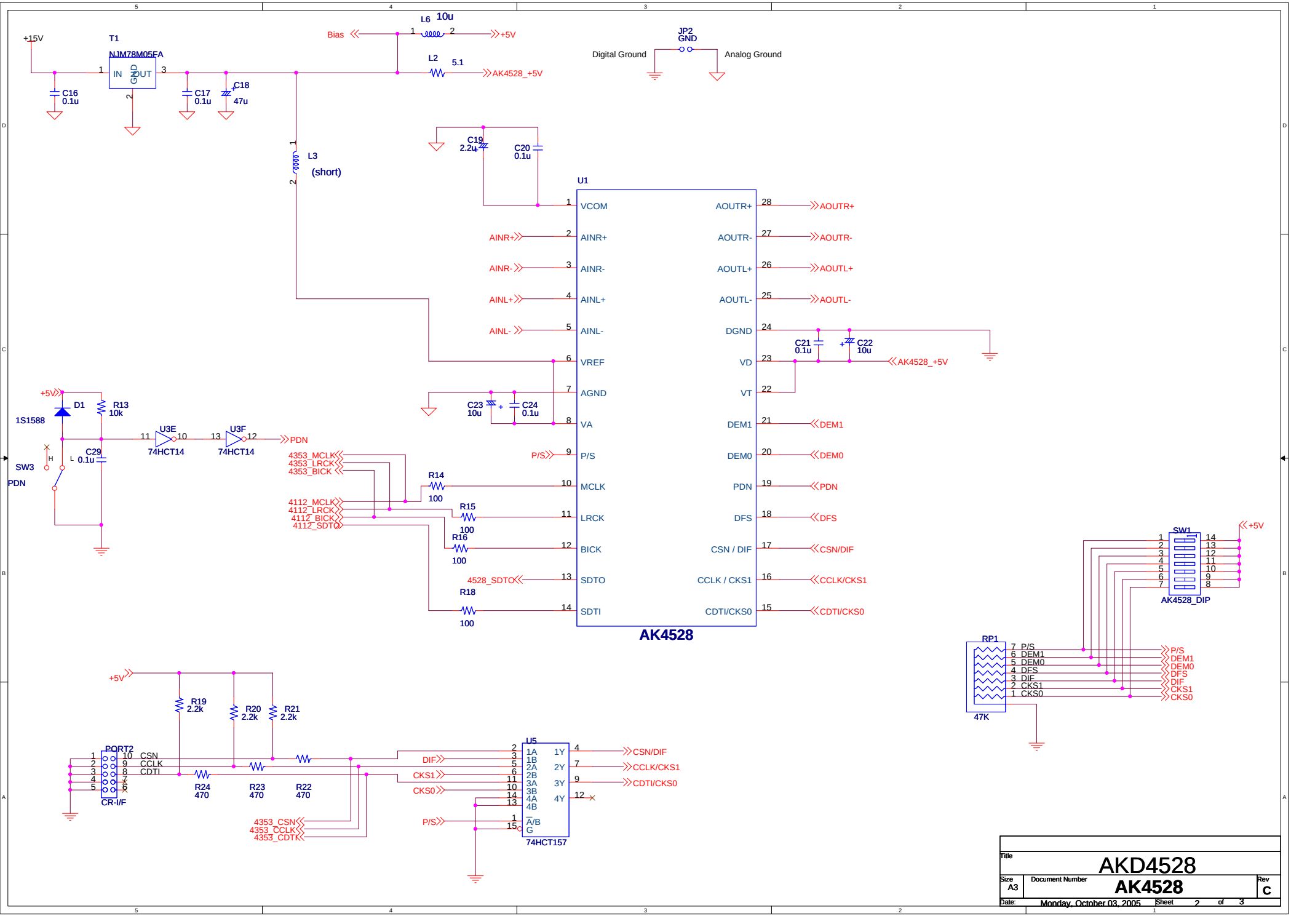
Crosstalk

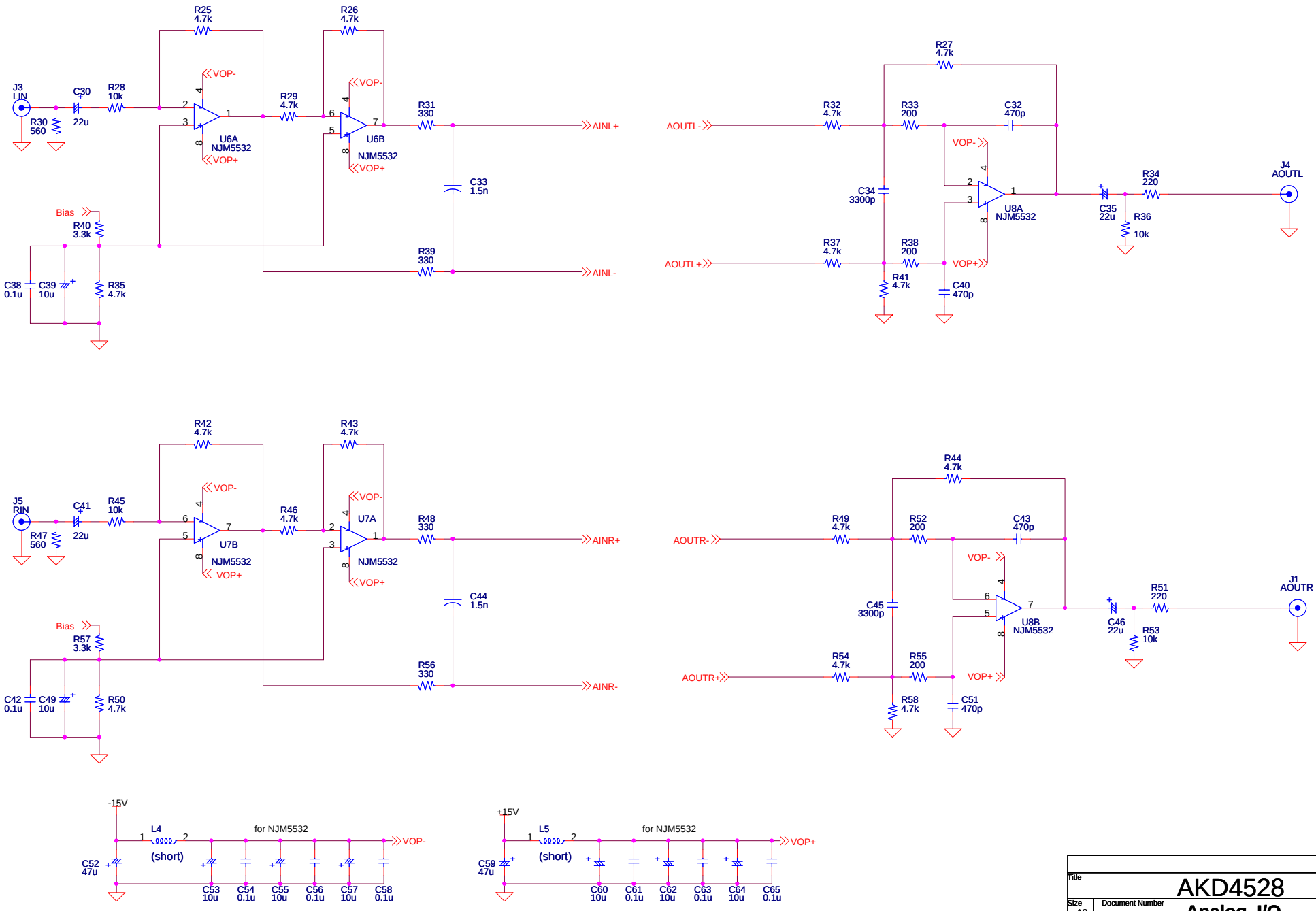
Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
00/06/01	KM063100	0	First Edition	
05/11/01	KM063101	1	Circuit Change	(1) AK4112A→AK4112B (2) C6, C7: 22pF→5pF (3) C36, C37, C47, C48→Delete (4) L2: short→Resistance: 5.1 Ohm
			Manual Change	(1) Change DOS base program to Windows base program. (2) Change the description about control program. (3) Add register / pin settings of AK4528 and AK4353.

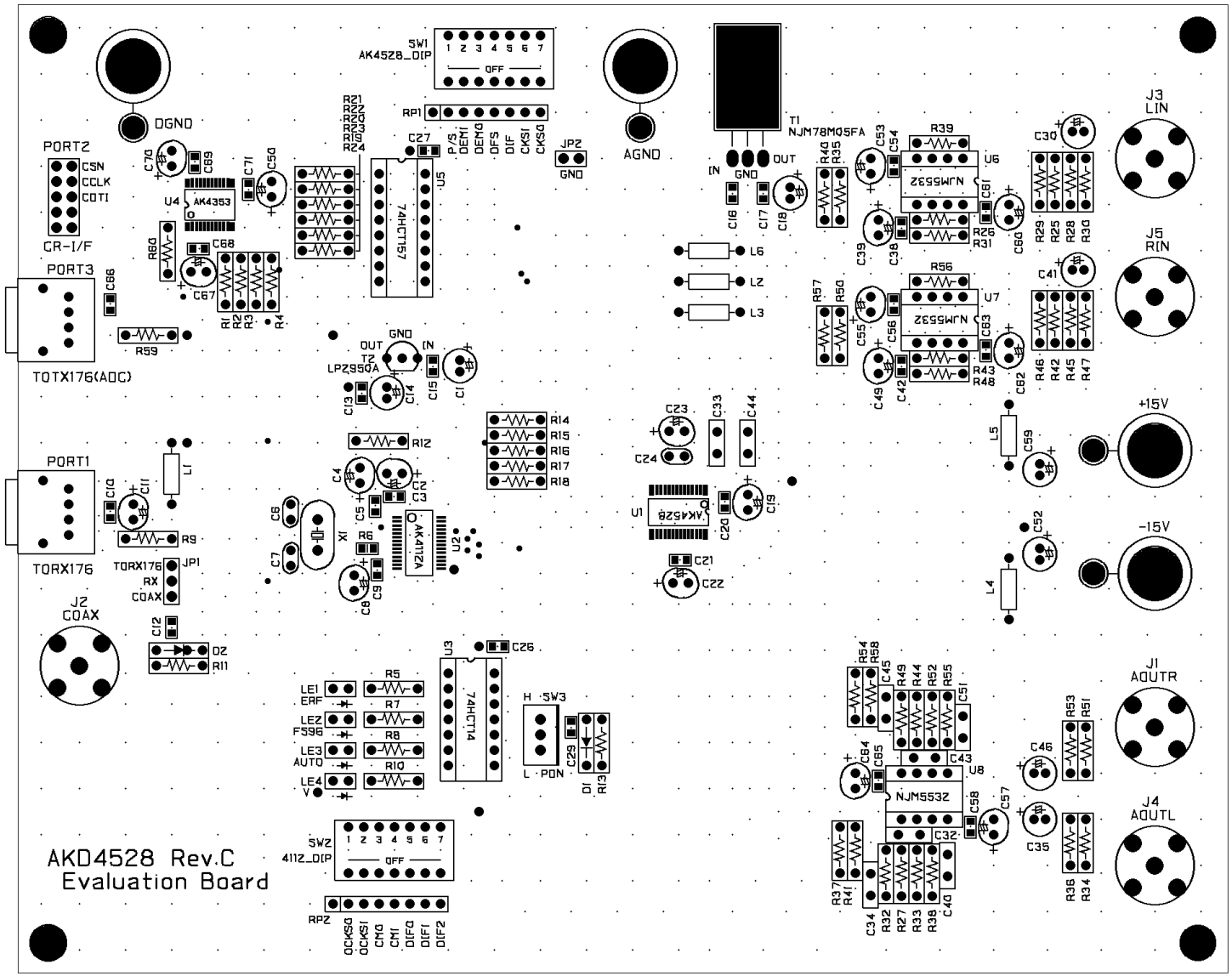


Title	AKD4528		
Size A3	Document Number AK4112B AK4353 DIR DIT		Rev C
Date: Monday, October 03, 2005	Sheet 1 of 3		

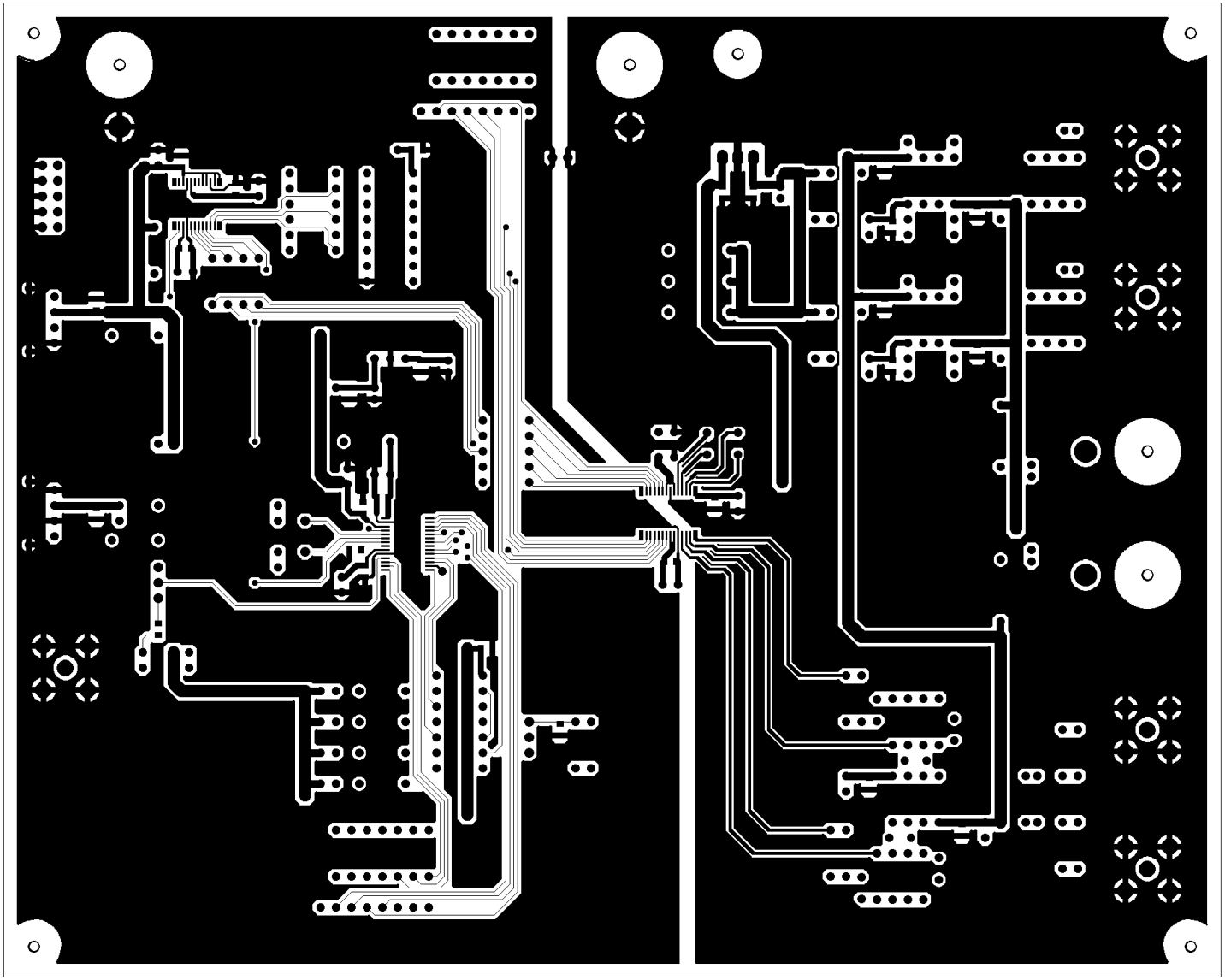

+15V
T1
NJM78M05FA
IN
GND
OUT
C16 0.1u
C17 0.1u
C18 47u
L6 10u
Bias
+5V
L2 5.1
AK4528_+5V
JP2
GND
Digital Ground
Analog Ground
L3 (short)
C19 2.2u
C20 0.1u
U1
VCOM
AINR+
AINR-
AINL+
AINL-
VREF
AGND
VA
P/S
MCLK
LRCK
BICK
SDTO
SDTI
AOUTR+
AOUTR-
AOUTL+
AOUTL-
DGND
VD
VT
DEM1
DEM0
PDN
DFS
CSN / DIF
CCLK / CKS1
CDTI/CKS0
C21 0.1u
C22 10u
C23 10u
C24 0.1u
AK4528
+5V
D1
1S1588
R13 10k
U3E
U3F
74HCT14
PDN
SW3
C29 0.1u
4353_MCLK
4353_LRCK
4353_BICK
4112_MCLK
4112_LRCK
4112_BICK
4112_SDTO
4528_SDTO
R14 100
R15 100
R16 100
R18 100
SW1
AK4528_DIP
RP1
47K
R19 2.2k
R20 2.2k
R21 2.2k
PORT2
CR-I/F
CSN
CCLK
CDTI
R24 470
R23 470
R22 470
4353_CSN
4353_CCLK
4353_CDTK
DIF
CKS1
CKS0
U5
74HCT157
A/B
G
Title
AKD4528
Size
A3
Document Number
AK4528
Rev
C
Date:
Monday, October 03, 2005
Sheet
2
of
3



Title	AKD4528	
Size: A3	Document Number: Analog_I/O	Rev: C
Date: Monday, October 03, 2005	Sheet 3 of 3	



AKD4528 Rev.C L1 SR SILK



AKD4528 Rev.C L1

AKD4529 Rev.C L2