

AKD4386

Evaluation board Rev.A for AK4386

GENERAL DESCRIPTION

The AKD4386 is an evaluation board for the AK4386, the 24bit, 96kHz D/A converter for portable audio and home audio systems. The AKD4386 has the interface with AKM's A/D converter evaluation boards. Therefore, it is easy to evaluate the AK4386. The AKD4386 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ **Ordering guide**

AKD4386 --- Evaluation board for AK4386

FUNCTION

- **Compatible with 2 types of interface**
 - Direct interface with AKM's A/D converter evaluation boards
 - On-board AK4112B as DIR which accepts optical
- **BNC connector for an external clock input**

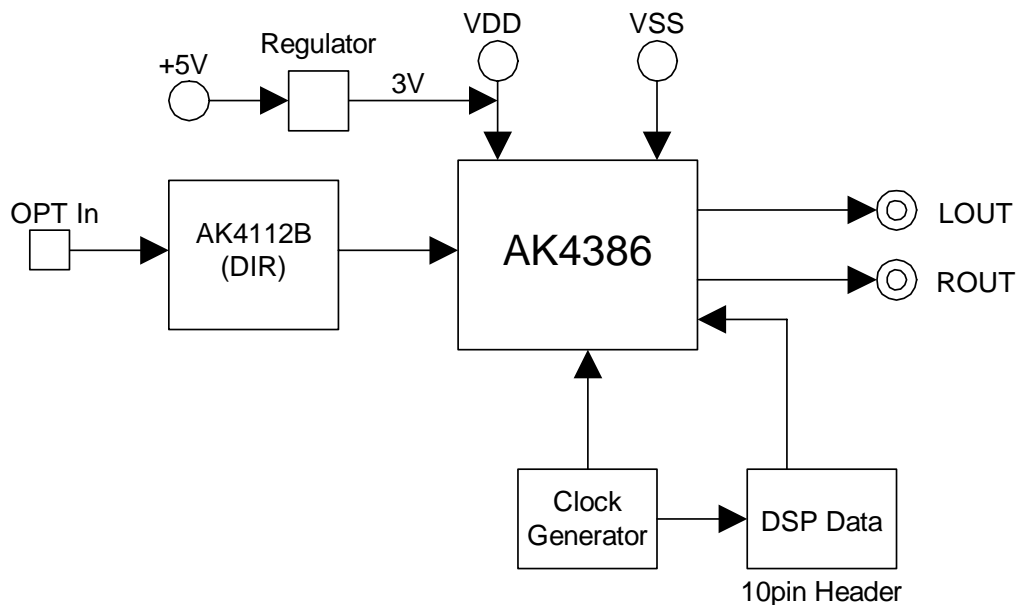


Figure 1. AKD4386 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ **Operation sequence**

1) Set up the power supply lines.

- [VDD] (red) = 2.2 ~ 3.6V (typ. 3.0V, for VDD pin)
- [D3V] (red) = 2.2 ~ 3.6V (typ. 3.0V, for 74LVC541)
- [+5V] (orange) = 5V (for regulator)
- [VCC] (red) = 3.3V (for digital logic)
- [AGND] (black) = 0V
- [DGND] (black) = 0V

Each supply line should be distributed from the power supply unit.

2) Set-up the evaluation modes, jumper pins and DIP switches (See the followings.)

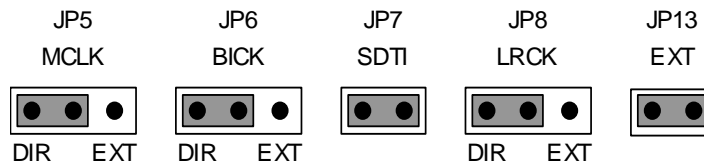
3) Power on.

The AK4386 should be reset once bringing SW2 “L” upon power-up.

■ **Evaluation mode**

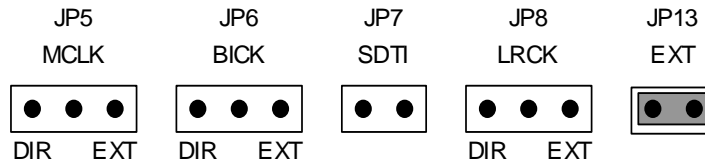
1) DIR (Optical Link) <Default>

The AK4112B (DIR) generates MCLK, BICK, LRCK and SDTI from the received data through PORT2 (TORX141: optical link). Used for the evaluation using CD test disk. Nothing should be connected to PORT1 (DSP).



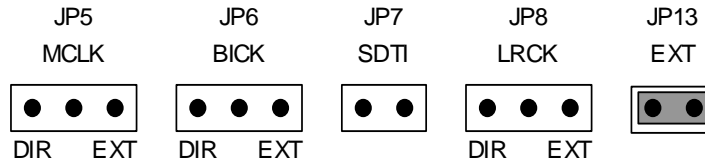
2) Using AKM's evaluation board for ADC

To evaluate the AK4386 with analog input, the AKM's evaluation board for ADC can be used. MCLK, BICK and LRCK and A/D converted data are sent to the AKD4386 through PORT1 (DSP) via 10pin flat cable.



3) Feeding all signals from external

Under the following set-up, all external signals can be fed through POTR1 (DSP).



■ Other Jumper pins set up

[JP1] (VDD2): D3V and VCC

OPEN: Separated

SHORT: Common. (The connector "VCC" can be open.) <Default>

[JP2] (VDD1): VDD and D3V

OPEN: Separated

SHORT: Common. (The connector "D3V" can be open.) <Default>

[JP3] (REG): +5V and VDD

OPEN: Separated

SHORT: Common. (The connector "VDD" can be open.) <Default>

The regulator can be supplied 3.0V to all circuits by shorting JP1, JP2 and JP3 and supplying 5V to +5V connector.

[JP4] (GND): Analog ground and Digital ground

OPEN: Separated

SHORT: Common. (The connector "DGND" can be open.) <Default>

[JP11] (BCFS): Select BICK of the AK4386

x1: BICK=128fs in case of MCLK=256fs/384fs/512fs/768fs.

BICK=64fs in case of MCLK=192fs.

x2: BICK=64fs in case of MCLK=128fs/256fs/384fs/512fs/768fs.

BICK=32fs in case of MCLK=192fs.

BICK=128fs in case of MCLK=1024fs/1536fs.

x4: BICK=32fs in case of MCLK=128fs/256fs/384fs/512fs/768fs.

BICK=64fs in case of MCLK=1024fs/1536fs.

x8: BICK=32fs in case of MCLK=1024fs/1536fs.

[JP9] (DIV), [JP10] (CLK), [JP12] (LRFS)

When using J3 (EXT), these jumper pins should be set according to Table 1.

■ Example for External Clock setting

Refer to the following setting when MCLK, BICK and LRCK are supplied to the AK4386 from J3 (EXT).

Mode	fs	MCLK	JP9 (DIV)	JP10 (CLK)	JP12 (LRFS)
Half	8kHz	512fs = 4.096MHz	x2	x2	x1
		768fs = 6.144MHz	x3	x2	x1
		1024fs = 8.192MHz	x2	x2	x2
		1536fs = 12.288MHz	x3	x2	x2
	24kHz	512fs = 12.288MHz	x2	x2	x1
		768fs = 18.432MHz	x3	x2	x1
		1024fs = 24.576MHz	x2	x2	x2
		1536fs = 36.864MHz	x3	x2	x2
Normal	8kHz	256fs = 2.048MHz	x1	x2	x1
		384fs = 3.072MHz	OPEN	x3	x1
		512fs = 4.096MHz	x2	x2	x1
		768fs = 6.144MHz	x3	x2	x1
	32kHz	256fs = 8.192MHz	x1	x2	x1
		384fs = 12.288MHz	OPEN	x3	x1
		512fs = 16.384MHz	x2	x2	x1
		768fs = 24.576MHz	x3	x2	x1
	44.1kHz	256fs = 11.2896MHz	x1	x2	x1
		384fs = 16.9344MHz	OPEN	x3	x1
		512fs = 22.5792MHz	x2	x2	x1
		768fs = 33.8688MHz	x3	x2	x1
	48kHz	256fs = 12.288MHz	x1	x2	x1
		384fs = 18.432MHz	OPEN	x3	x1
		512fs = 24.576MHz	x2	x2	x1
		768fs = 36.864MHz	x3	x2	x1
Double	48kHz	128fs = 6.144MHz	OPEN	x1	x1
		192fs = 9.216MHz	OPEN	x3	x3
		256fs = 12.288MHz	x1	x2	x1
		384fs = 18.432MHz	OPEN	x3	x1
	96kHz	128fs = 12.288MHz	OPEN	x1	x1
		192fs = 18.432MHz	OPEN	x3	x3
		256fs = 24.576MHz	x1	x2	x1
		384fs = 36.864MHz	OPEN	x3	x1

Default

Table 1. Clock Setting

■ DIP Switch set up

[SW1] : Setting the sampling frequency and de-emphasis filter for the AK4386

No.	Name	OFF ("L")	ON ("H")	Default
1	DFS0	See Table 3		OFF ("L")
2	DFS1			OFF ("L")
3	DEM	De-emphasis OFF	De-emphasis ON	OFF ("L")

Table 2. Mode Setting 1 of SW1

DFS1	DFS0	Mode	fs	Default
L	L	Normal	8kHz ~ 48kHz	
L	H	Double	48kHz ~ 96kHz	
H	L	Half	8kHz ~ 24kHz	
H	H	Auto	8kHz ~ 96kHz	

Table 3. Sampling Speed for AK4386

[SW5] : Setting the audio interface format for the AK4386 and AK4112B

No.	Name	OFF ("L")	ON ("H")	Default
1	DIF0	See Table 5		OFF ("L")
2	DIF1			ON ("H")
3	DIF			OFF ("L")

Table 4. Mode Setting 2 of SW5

DIF1	DIF0	DIF	SDTI Format	Default
L	L	L	16bit, LSB justified	
L	H	H	24bit, LSB justified	
H	L	L	24bit, MSB justified	
H	H	L	16/24bit, I ² S Compatible	

Table 5. Audio Interface Format

Note. The AK4112B does not support 16bit, I²S Compatible.

■ The function of the toggle SW

[SW2] (PDN): Resets the AK4386. Keep “H” during normal operation.

[SW3] (PM): Select power down mode for the AK4386. (See Table 6)

Mode	MCLK	PDN pin	PM pin	DAC Output	State
0	Input	L	L	VCOM Voltage	Power Save
1		L	H	Hi-Z	Full Power Down
2		H	L	VCOM Voltage	Power Save
3		H	H	Normal Output	Normal
4	Stop	L	L	VCOM Voltage	Power Save
5		L	H	Hi-Z	Full Power Down
6		H	L	VCOM Voltage	Power Save
7		H	H	VCOM Voltage	Power Save

Table 6. Power down mode

[SW4] (DIR): Resets the AK4112B. Keep “H” during normal operation.

■ Analog Output Circuit

The analog output of the AK4386’s DAC outputs from J1 and J2.

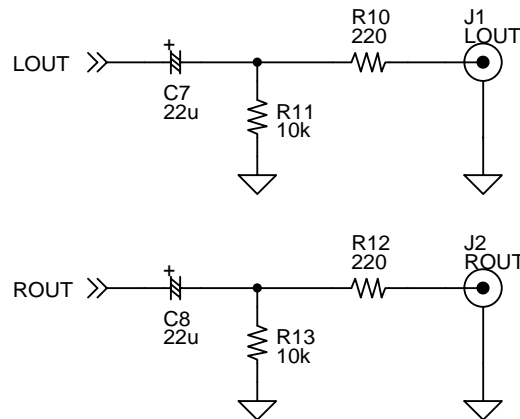


Figure 2. LOUT/ROUT Output circuit

* AKM assumes no responsibility for the trouble when using the above circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 44.1kHz, 96kHz
- Bit : 24bit
- Power Supply : VDD = 3.0V
- Interface : DIR
- Temperature : Room

[Measurement Results]

Parameter	Results	Unit
DAC Analog Output Characteristics	Lch / Rch	
S/(N+D)		
(fs=44.1kHz, 0dBFS)	86.3 / 86.1	dB
(fs=96kHz, 0dBFS)	84.7 / 84.4	dB
D-Range		
(fs=44.1kHz, -60dBFS, A-weighted)	100.8 / 100.8	dB
(fs=96kHz, -60dBFS)	96.1 / 96.1	dB
S/N		
(fs=44.1kHz, A-weighted)	100.8 / 100.8	dB
(fs=96kHz)	96.1 / 96.1	dB
Interchannel Isolation	117.3 / 116.4	dB

[DAC Plot : fs=44.1kHz]

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AK4386 THD+N vs. Input Level
VDD=3.0V, fs=44.1kHz, fin=1kHz

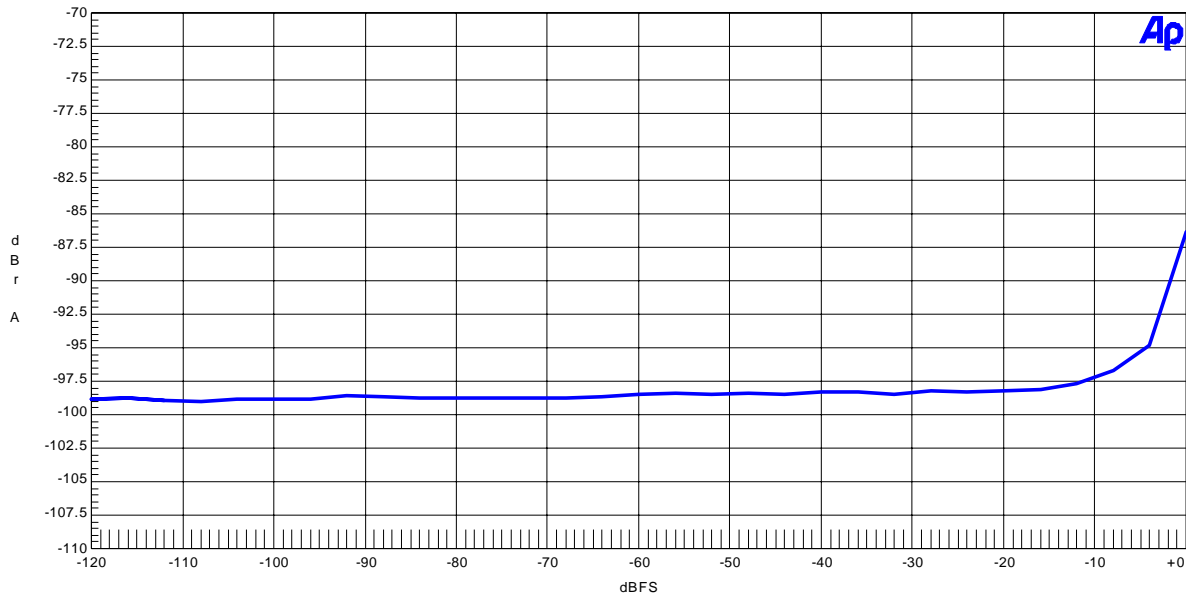


Figure 1. THD+N vs. Input Level

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AK4386 THD+N vs. Input Frequency
VDD=3.0V, fs=44.1kHz, Input=0dBFS

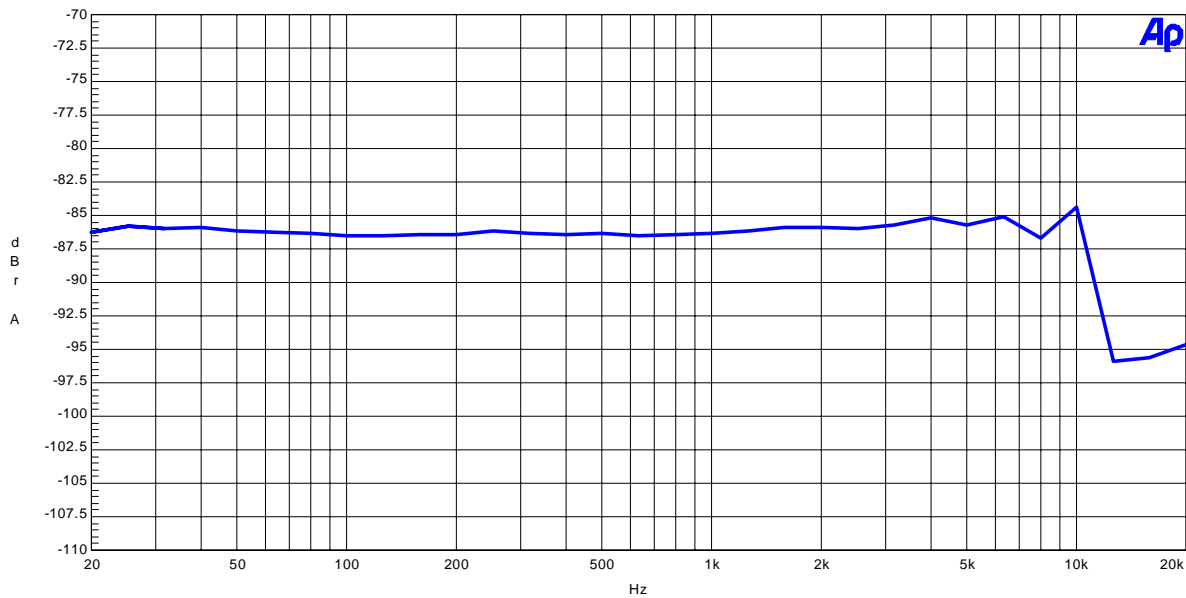


Figure 2. THD+N vs. Input Frequency

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AK4386 Linearity
VDD=3.0V, fs=44.1kHz, fin=1kHz

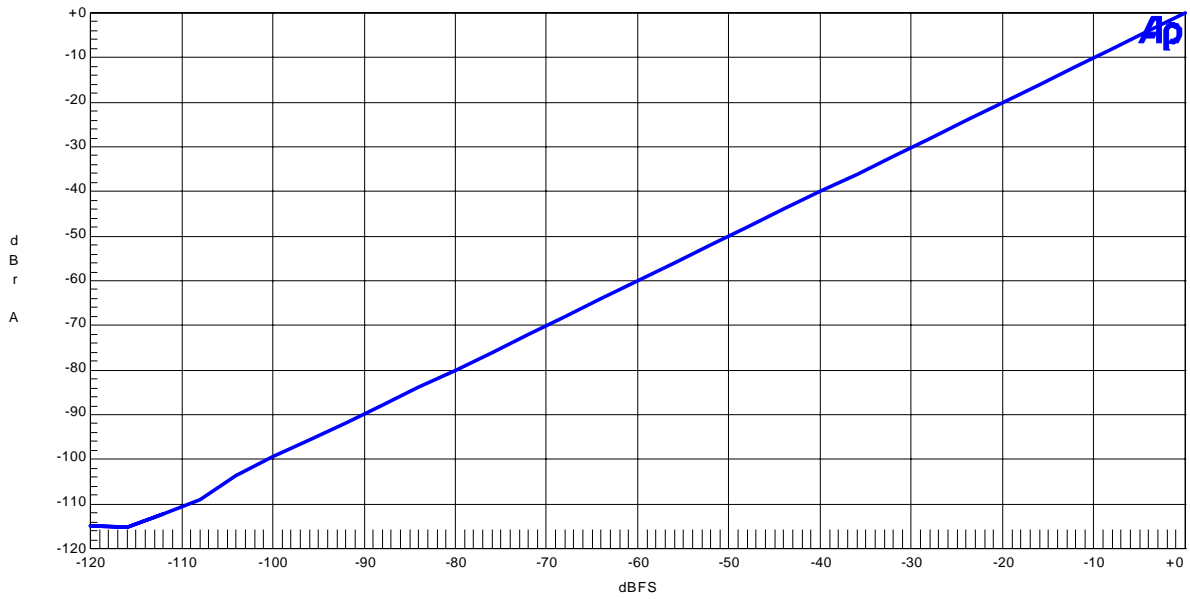


Figure 3. Linearity

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AK4386 Frequency Response
VDD=3.0V, fs=44.1kHz, Input=0dBFS

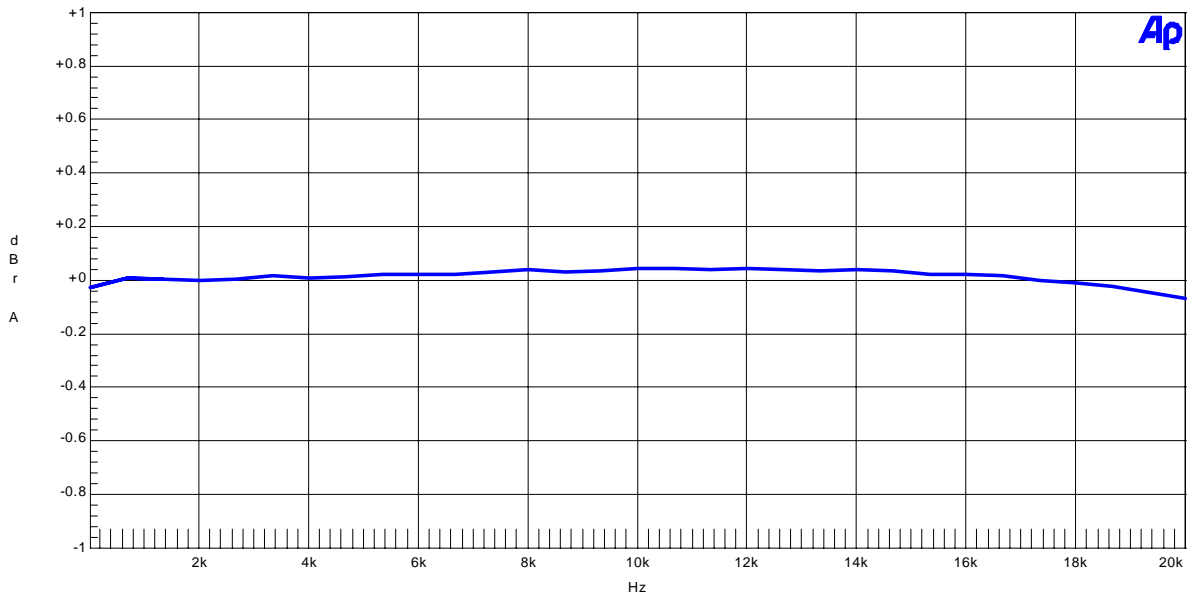


Figure 4. Frequency Response

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AK4386 Crosstalk (Blue:Rch->Lch, Red:Lch->Rch)
VDD=3.0V, fs=44.1kHz, Input=0dBFS

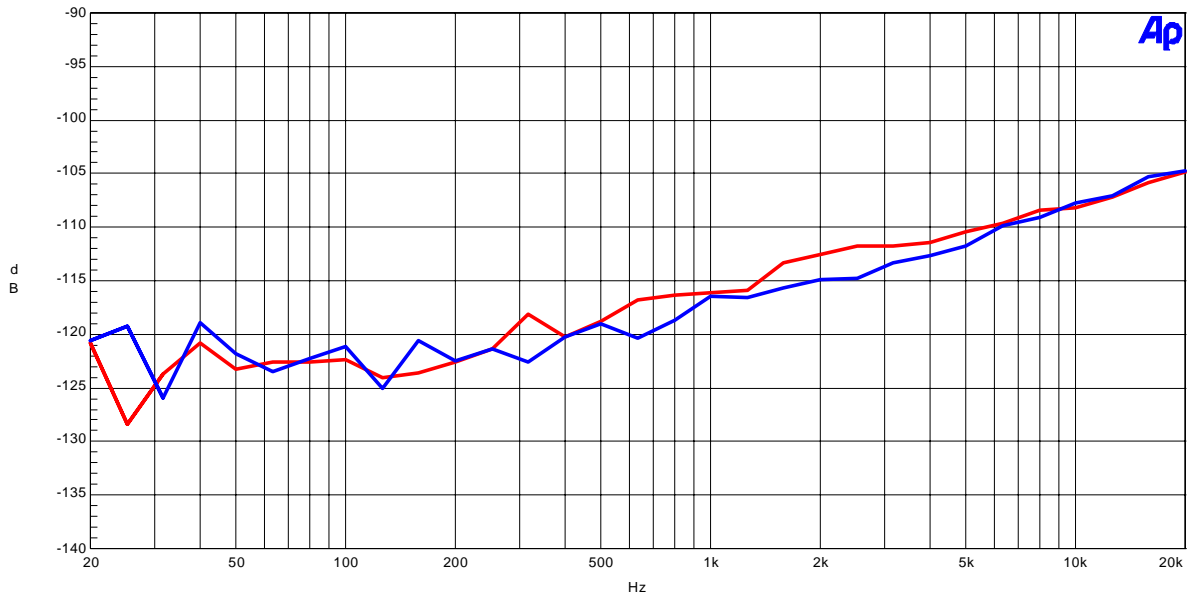


Figure 5. Crosstalk

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AK4386 FFT Plot
VDD=3.0V, fs=44.1kHz, Input=0dBFS, fin=1kHz

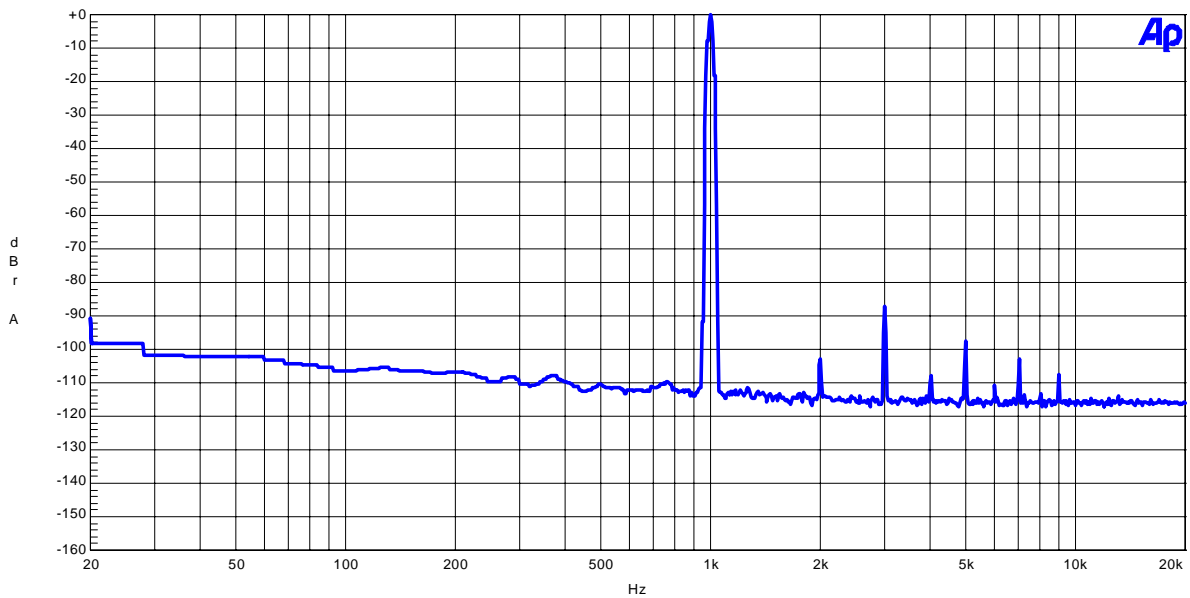


Figure 6. FFT Plot (Input = 0dBFS)

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AK4386 FFT Plot
VDD=3.0V, fs=44.1kHz, Input=-60dBFS, fin=1kHz

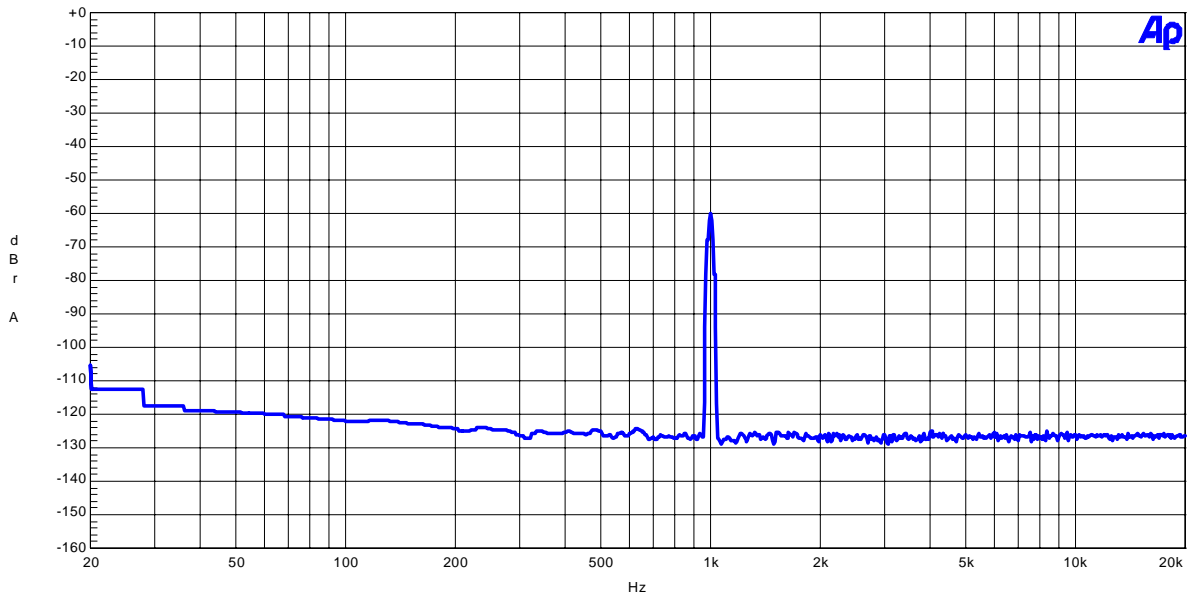


Figure 7. FFT Plot (Input = -60dBFS)

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AK4386 FFT Plot
VDD=3.0V, fs=44.1kHz, fin=None

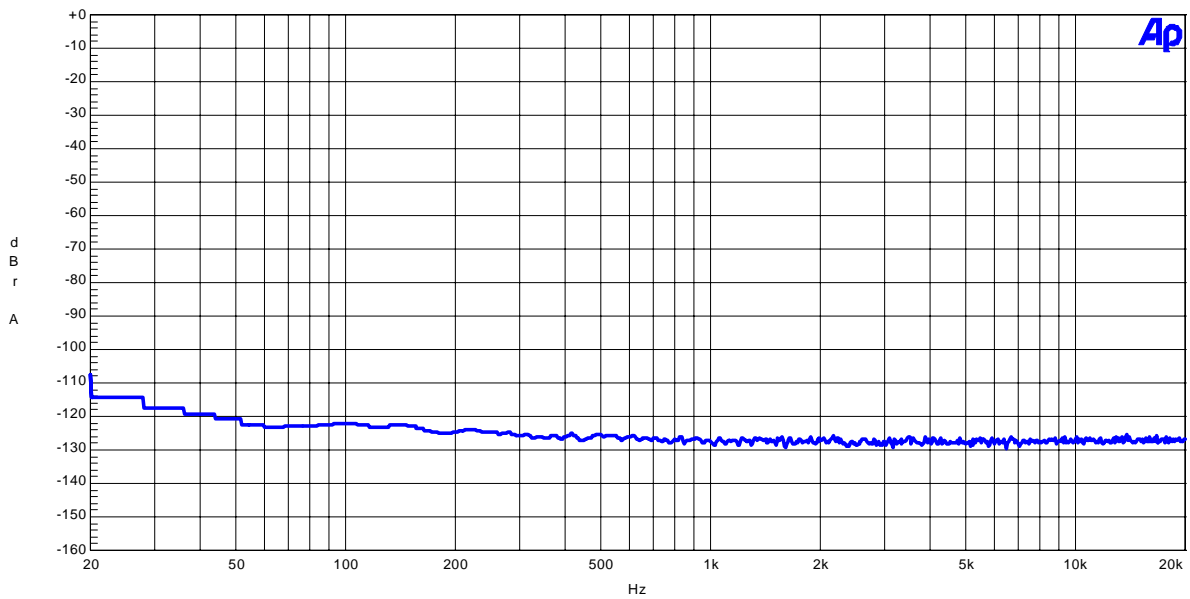


Figure 8. FFT Plot (Input = None)

[DAC Plot : fs=96kHz]

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AK4386 THD+N vs. Input Level
VDD=3.0V, fs=96kHz, fin=1kHz

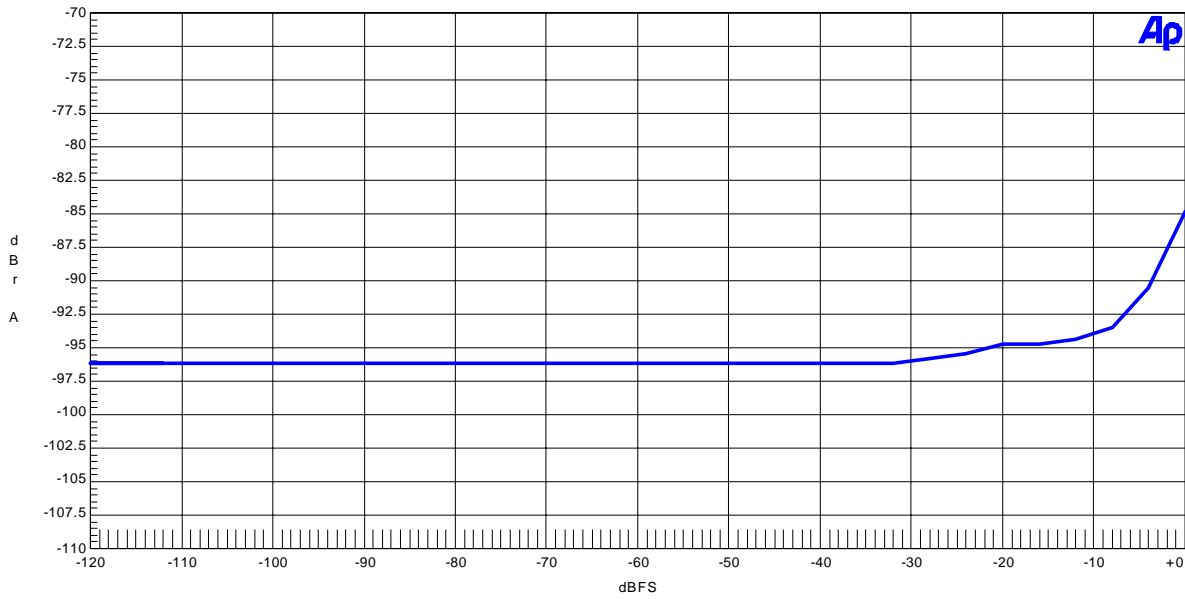


Figure 9. THD+N vs. Input Level

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AK4386 THD+N vs. Input Frequency
VDD=3.0V, fs=96kHz, Input=0dBFS

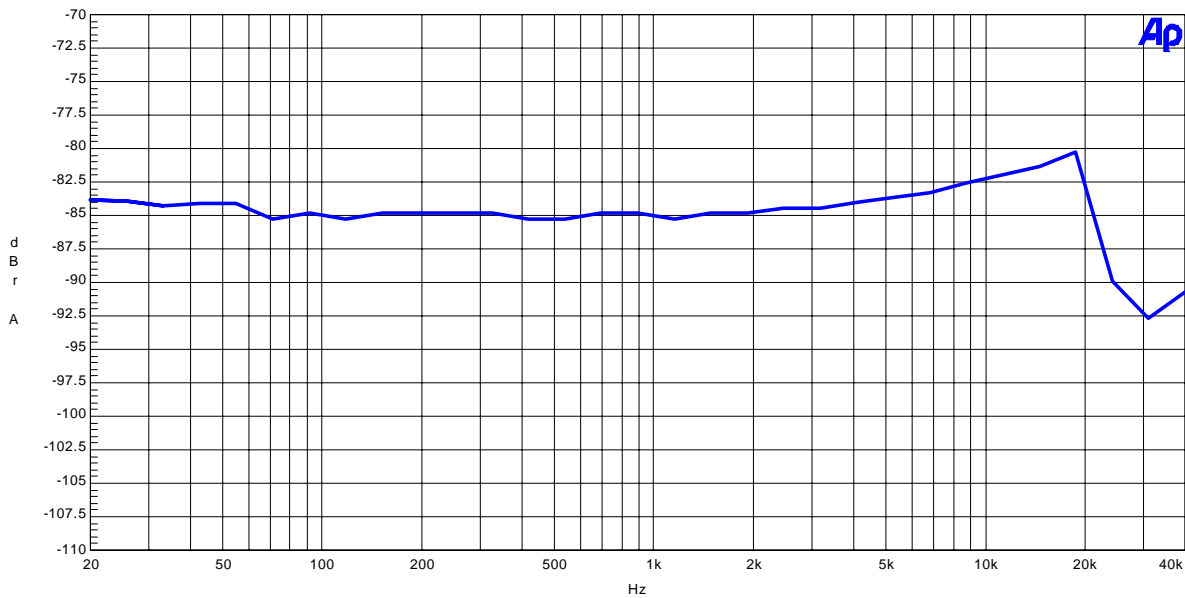


Figure 10. THD+N vs. Input Frequency

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AK4386 Linearity
VDD=3.0V, fs=96kHz, fin=1kHz

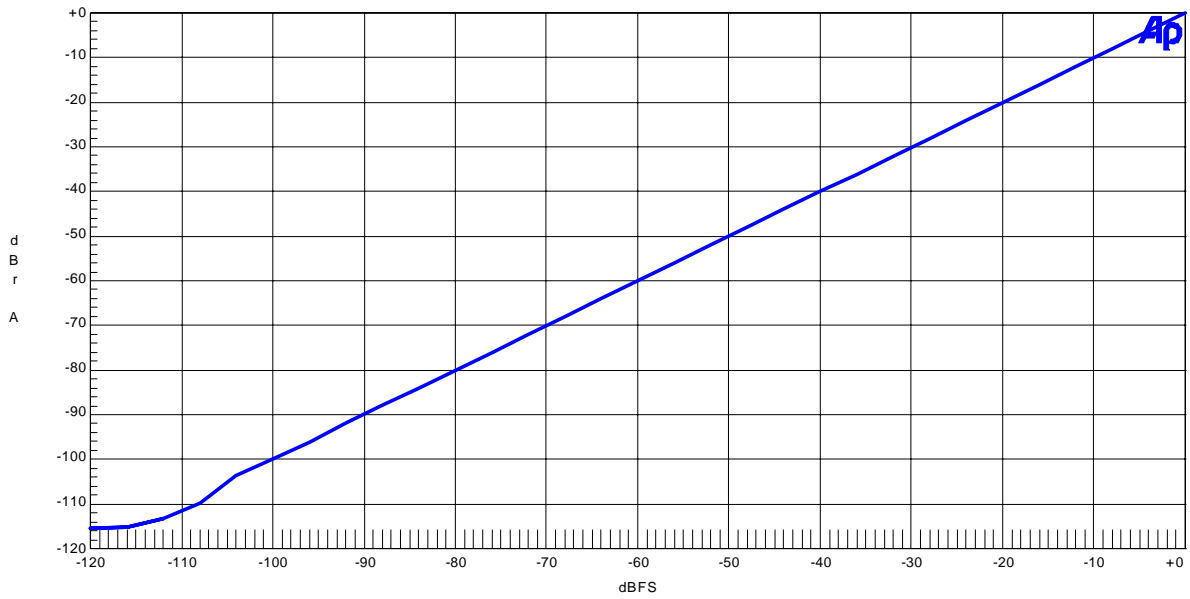


Figure 11. Linearity

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AK4386 Frequency Response
VDD=3.0V, fs=96kHz, Input=0dBFS

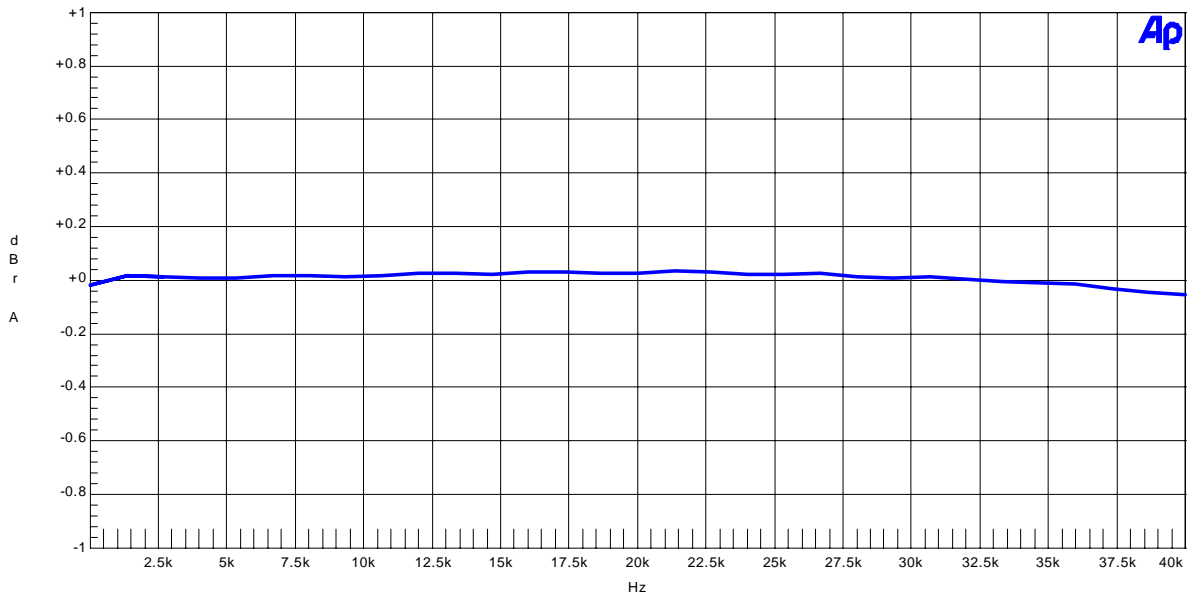


Figure 12. Frequency Response

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AK4386 Crosstalk (Blue:Rch->Lch, Red:Lch->Rch)
VDD=3.0V, fs=96kHz, Input=0dBFS

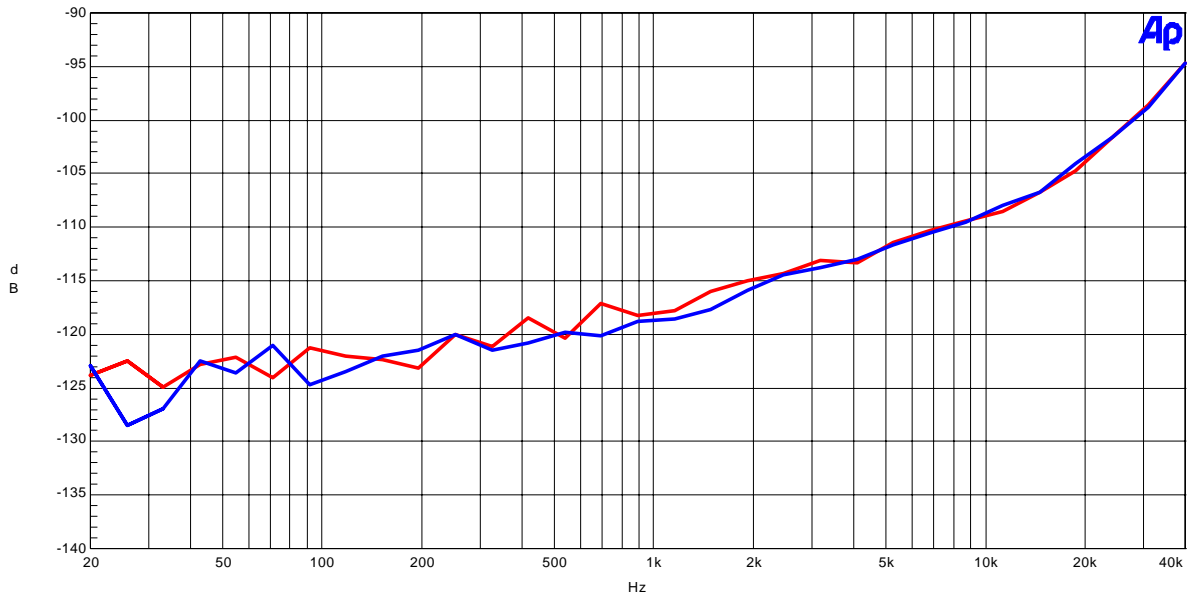


Figure 13. Crosstalk

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AK4386 FFT Plot
VDD=3.0V, fs=96kHz, Input=0dBFS, fin=1kHz

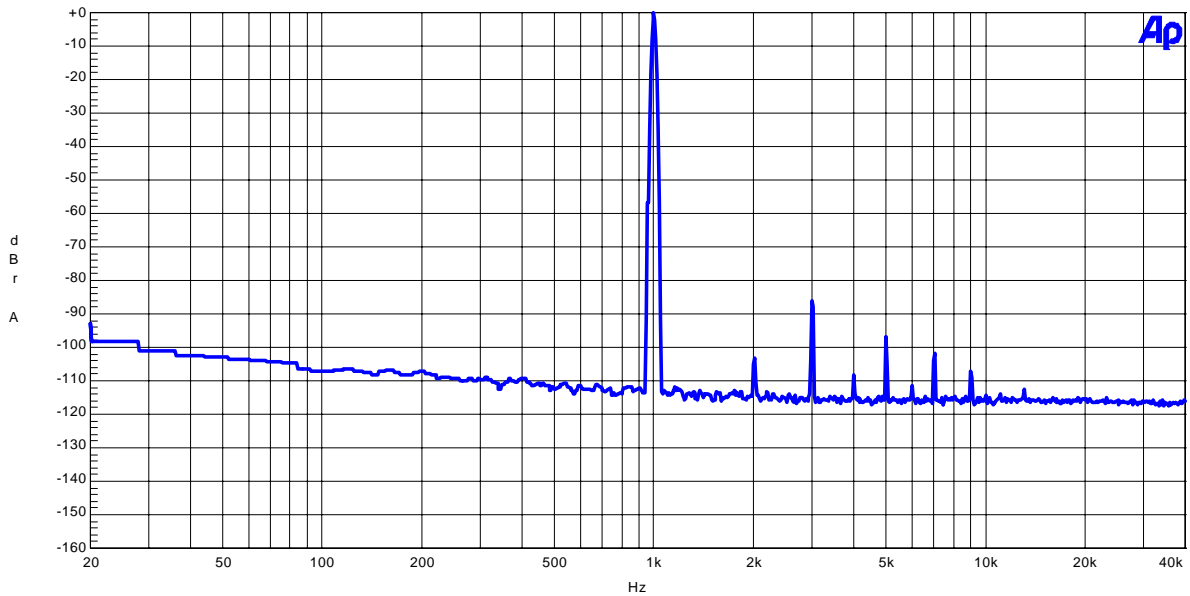


Figure 14. FFT Plot (Input = 0dBFS)

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AK4386 FFT Plot
VDD=3.0V, fs=96kHz, Input=-60dBFS, fin=1kHz

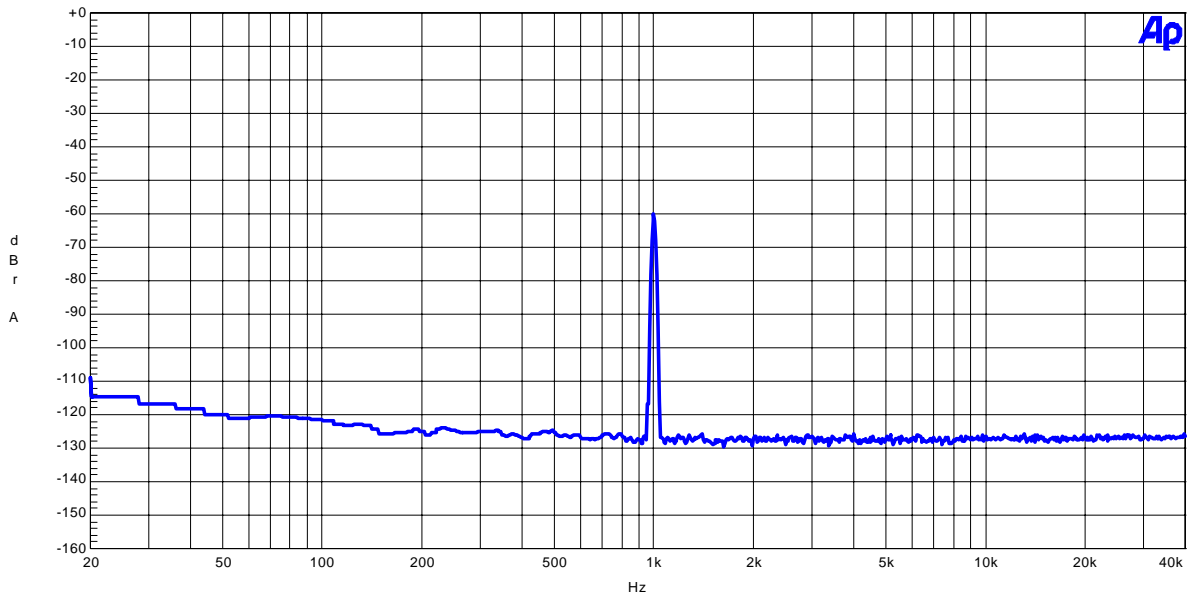


Figure 15. FFT Plot (Input = -60dBFS)

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AK4386 FFT Plot
VDD=3.0V, fs=96kHz, fin=None

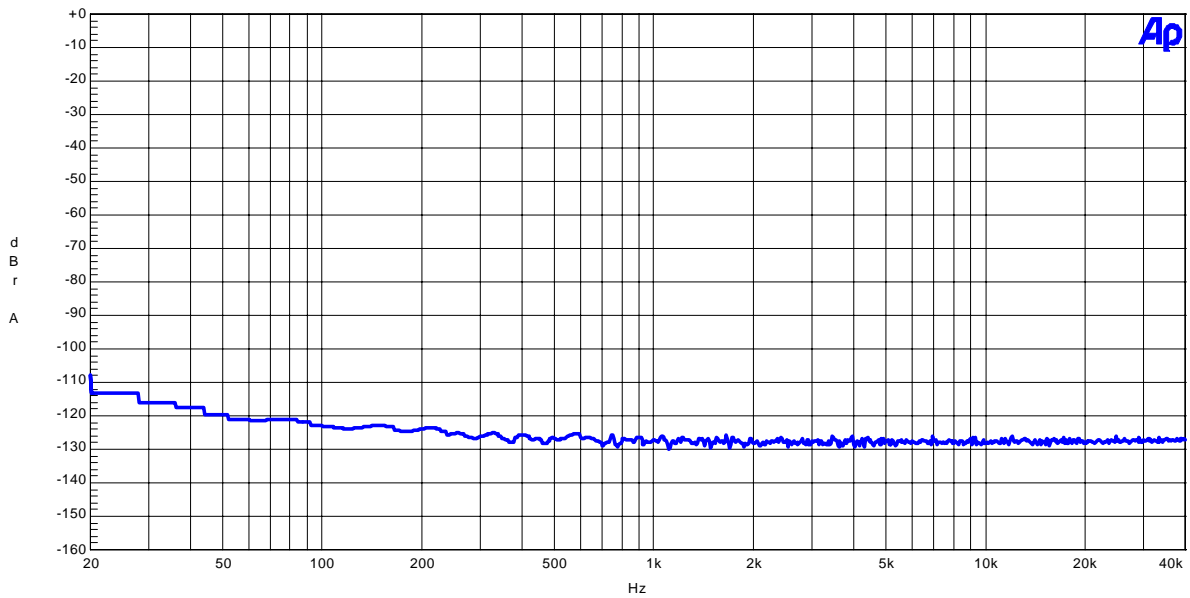
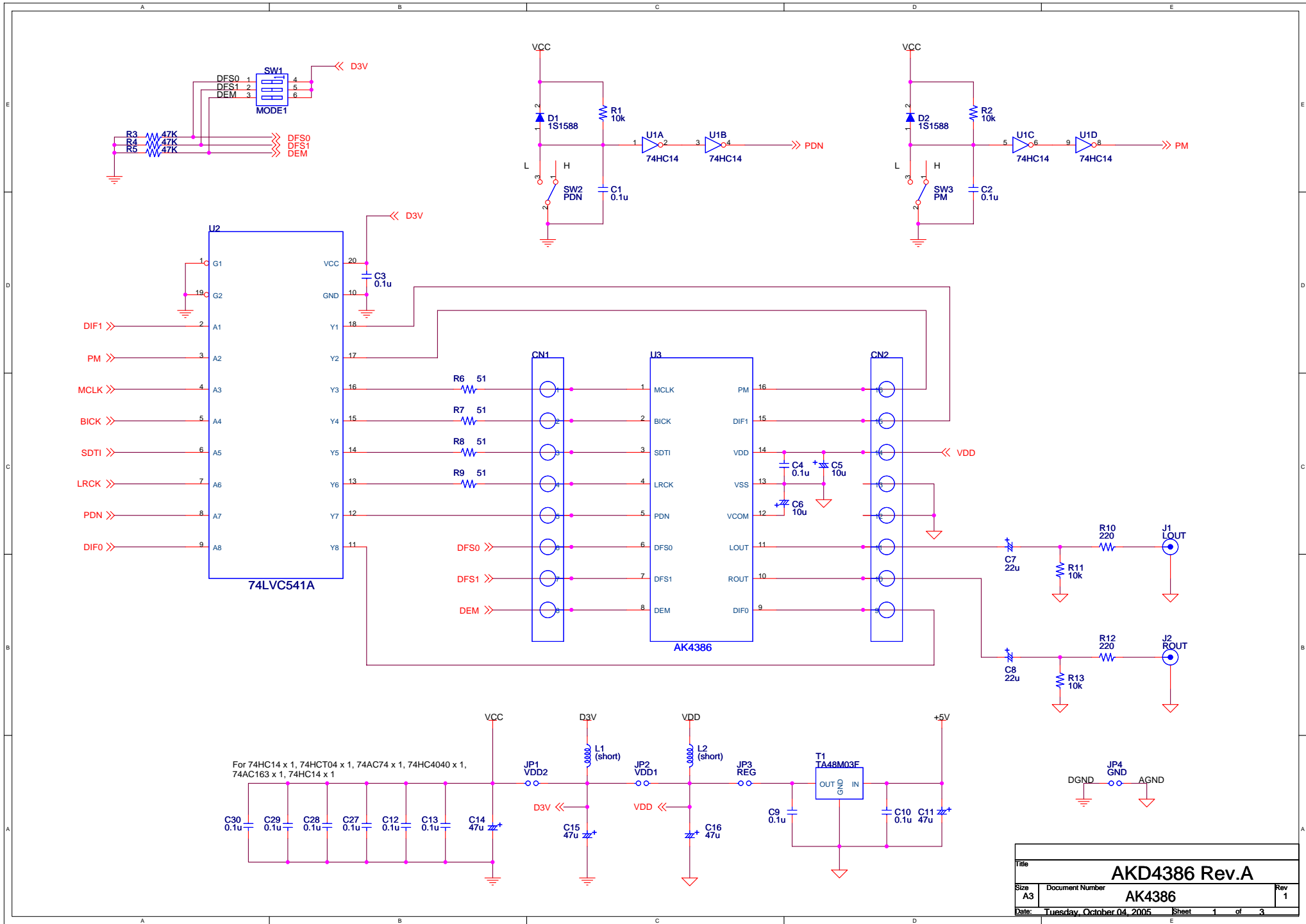


Figure 16. FFT Plot (Input = None)

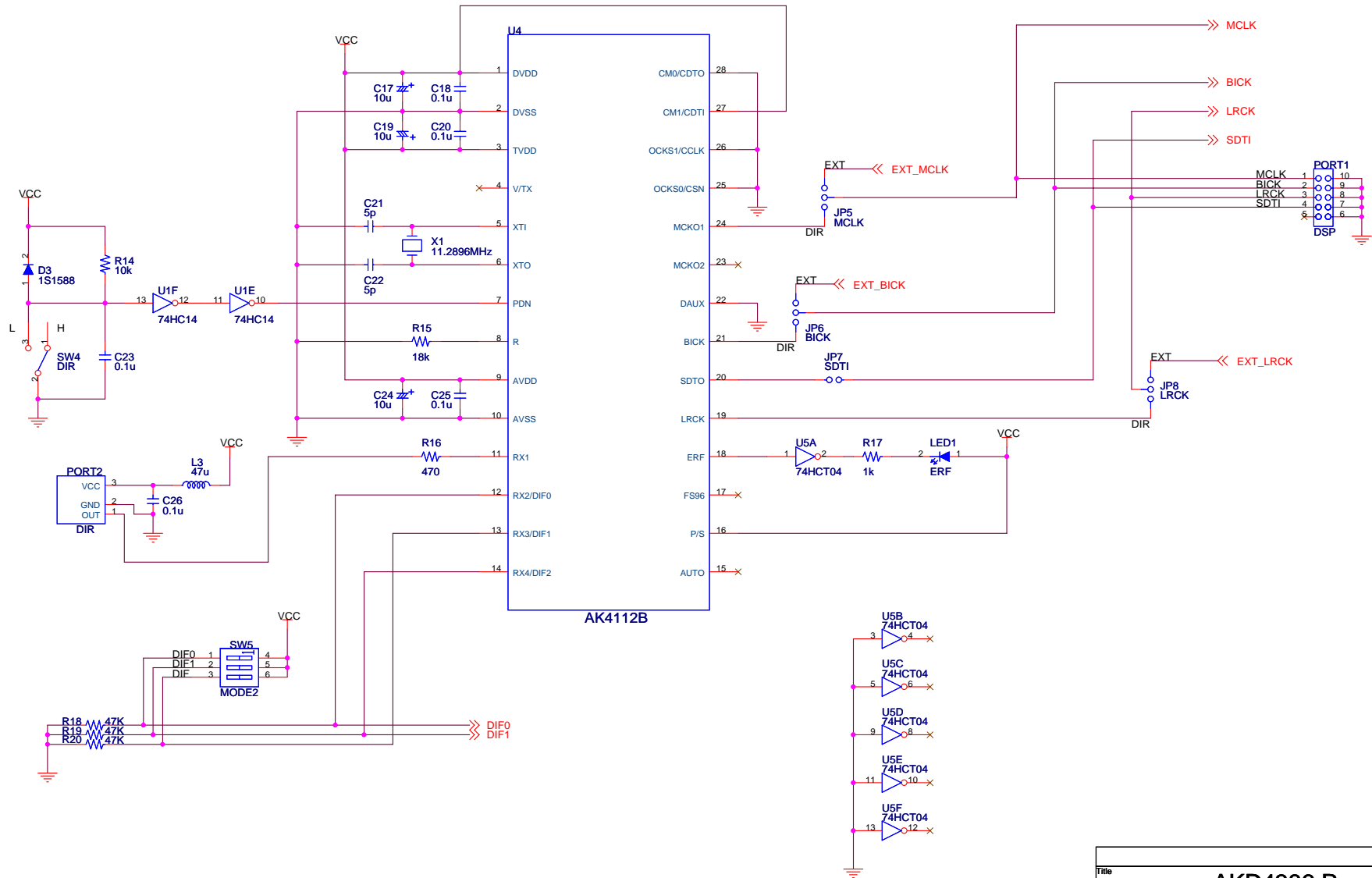
Revision History				
Date	Manual Revision	Board Revision	Reason	Contents
03/07/02	KM072000	0	First Edition	
05/10/04	KM072001	1	Update	Change of circuit

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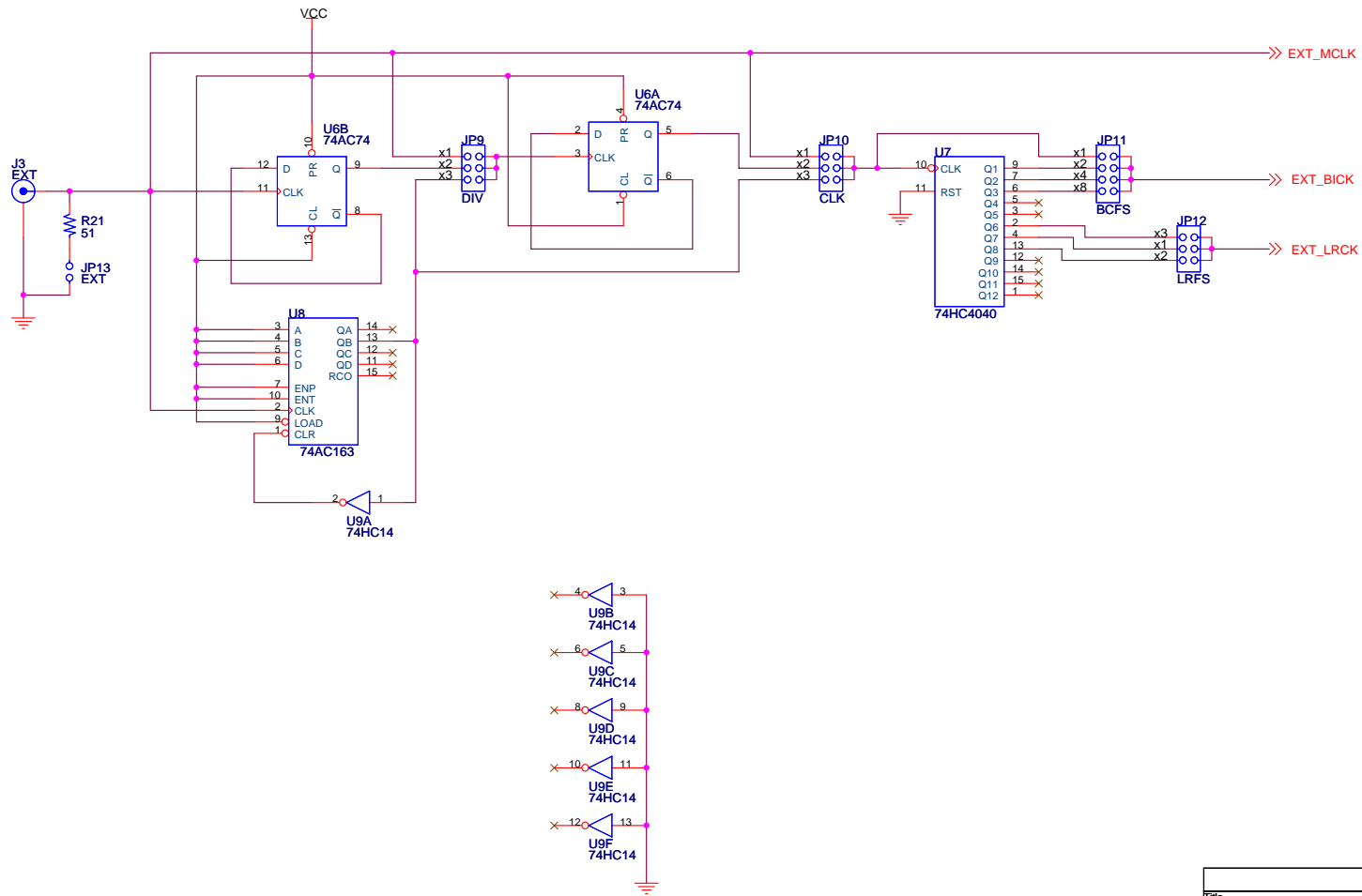
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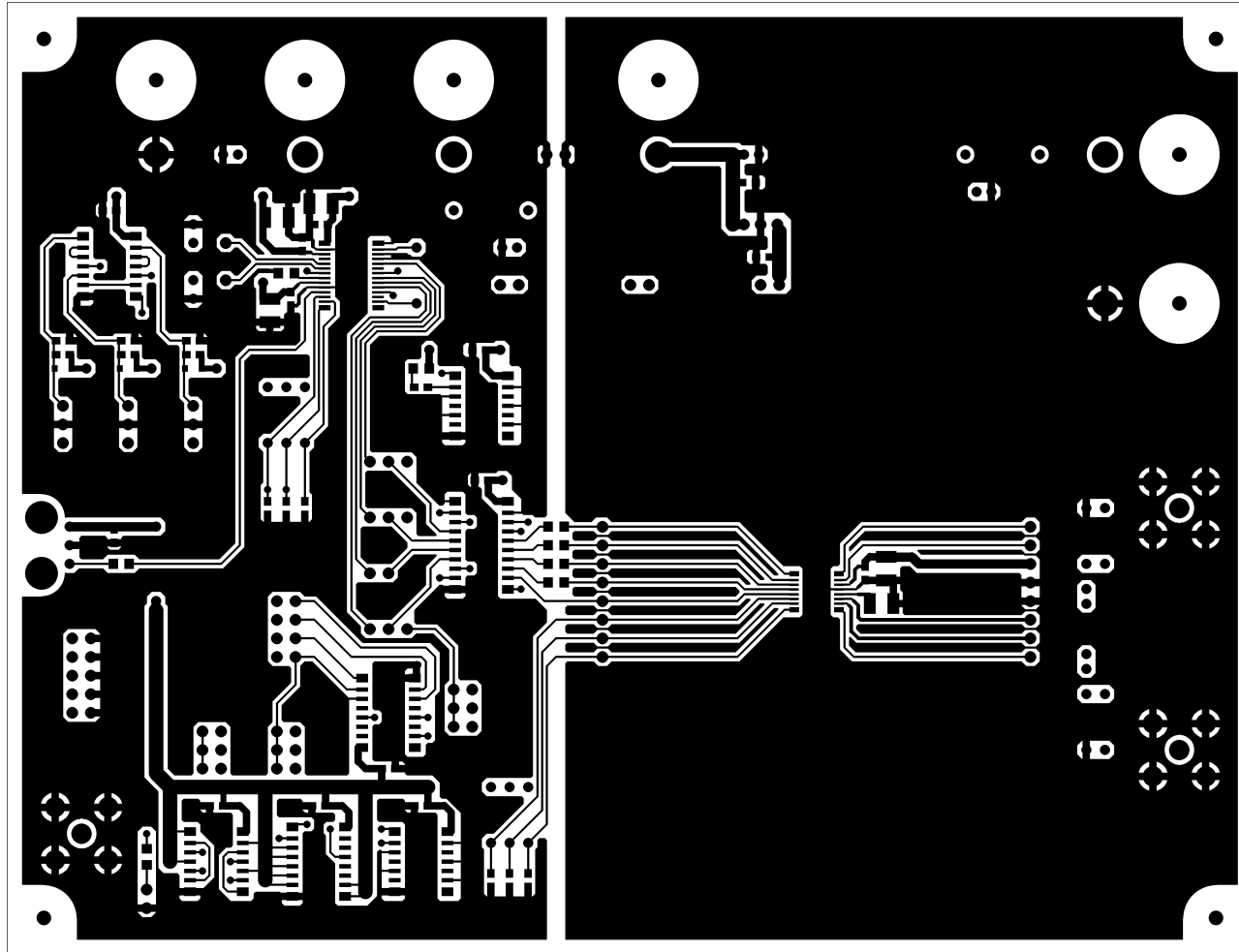
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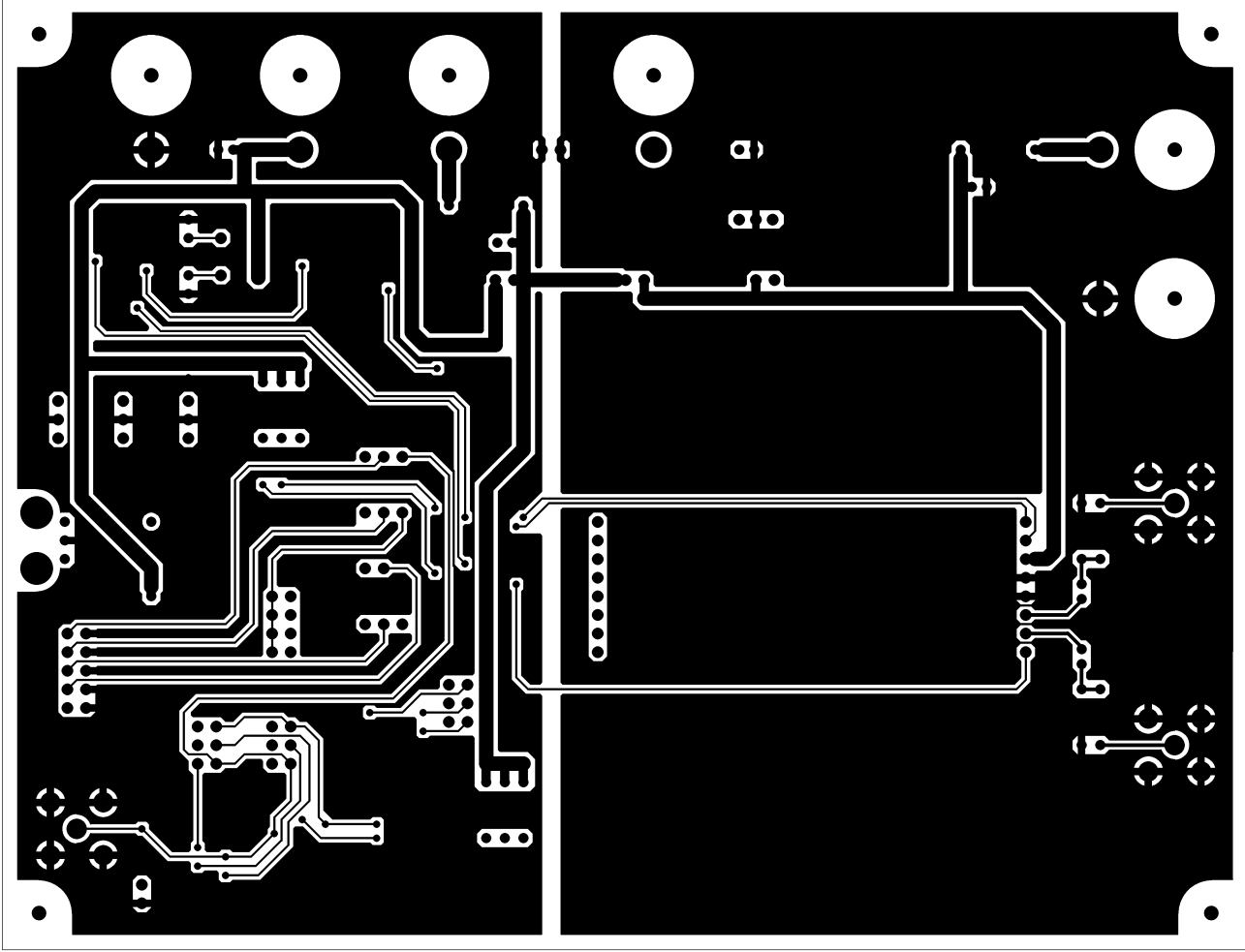
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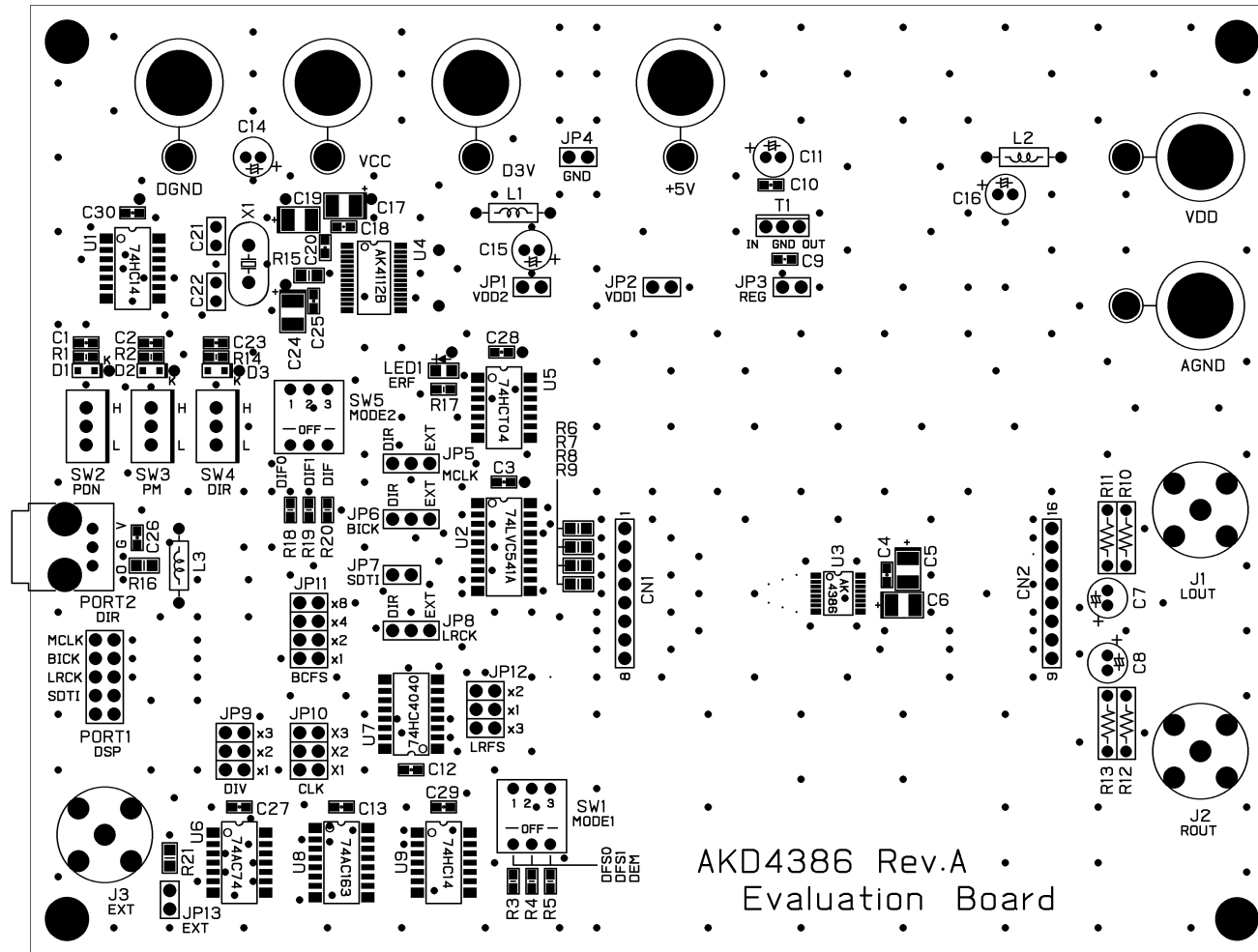
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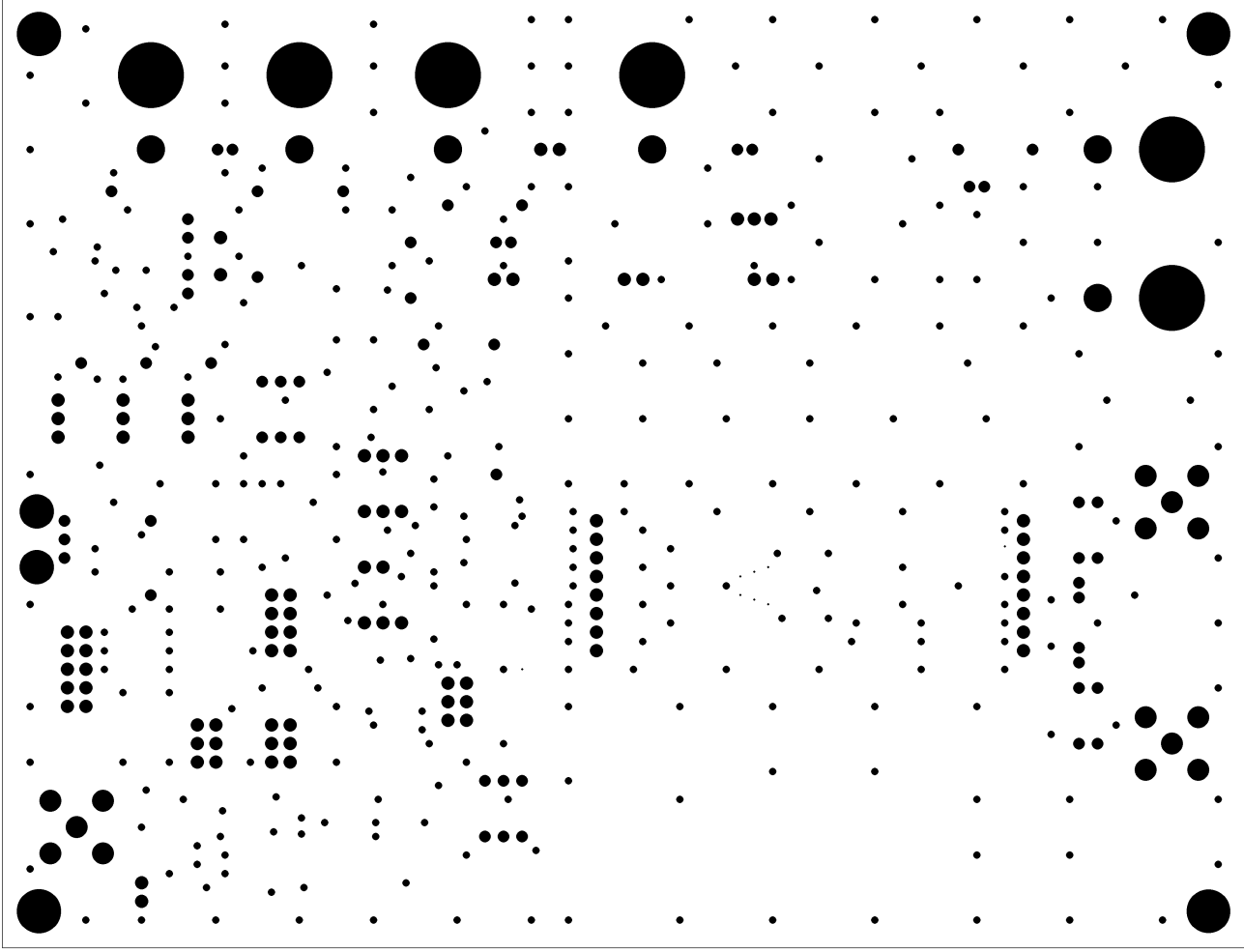
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