AK4665A

20-Bit Stereo CODEC with MIC/HP-AMP

GENERAL DESCRIPTION

The AK4665A is a 20bit CODEC with built-in Input PGA and Headphone Amplifier. The AK4665A includes a microphone/line input selector and an ALC circuit for input, and a stereo line output buffer, analog volume controls and capless stereo headphone amplifier for output. The AK4665A also features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features “pop-free” power-on/off, a mute control and delivers 31mW of power into 16Ω load. The AK4665A is housed in a 32pin QFN package, making it suitable for portable applications.

FEATURE

- **2ch 20bit ADC**
  - **Mono MIC-Amp: +30dB/+6dB/0dB/–6dB**
  - **Single-ended Input**
  - **Input Selector**
  - **Digital ALC: +41.25dB ~ –54dB, 0.375dB Step, Mute**
  - **Digital HPF for DC-offset cancellation**
  - **I/F format: 20bit MSB justified, I^2S**
  - **S/N: 93dB**
- **2ch 20bit DAC**
  - **Digital ATT: 0dB ~ –127dB, Mute, 0.5dB step (soft transition)**
  - **Soft Mute**
  - **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
  - **Bass Boost**
  - **I/F Format: I^2S, 20bit MSB justified, 20bit/16bit LSB justified**
- **Sampling Rate: 8kHz ~ 48kHz**
- **System clock: 256fs/512fs**
- **Analog Mixing Circuit**
- **Stereo Lineout**
  - **ALC: +19.5dB ~ –12dB, 0.5dB step**
  - **Analog Volume: 0dB ~ –30dB, Mute, 2dB step**
- **Capless Stereo Headphone Amplifier**
  - **Output Power: 31mW x 2ch @16Ω**
  - **Line output mode: 1Vrms @10kΩ**
  - **Charge pump circuit for negative power supply**
  - **S/N: 88dB**
- **µP Interface: 3-wire**
- **Power Management**
- **Power Supply:**
  - **AVDD, DVDD, HVDD: 2.6V ~ 3.6V**
  - **TVDD (Digital I/O): 1.6V ~ 3.6V**
- **Power Supply Current: 20mA**
- **Ta: –30 ~ 85°C**
- **Small Package: 32pin QFN (5mm x 5mm, 0.5mm pitch)**

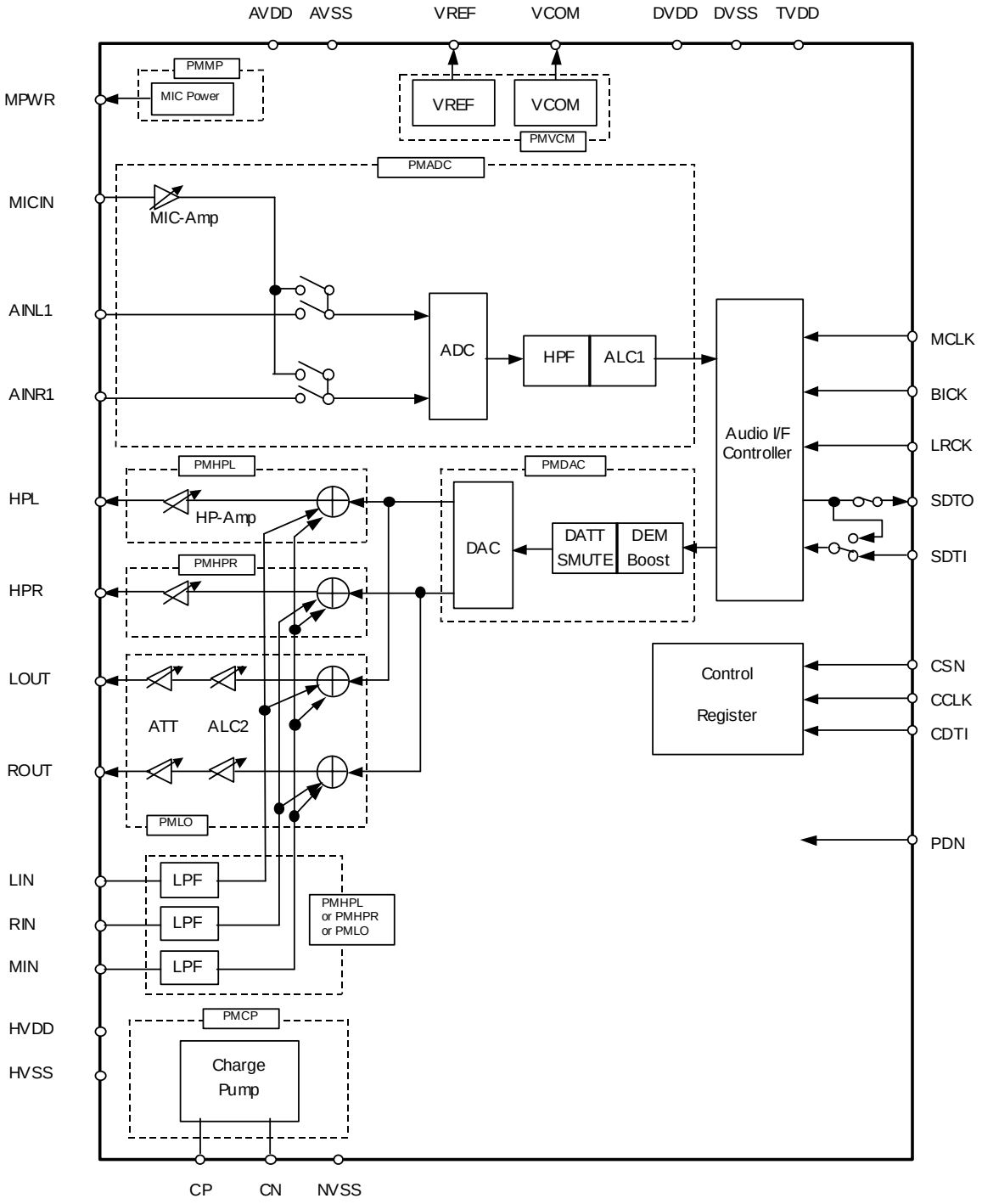
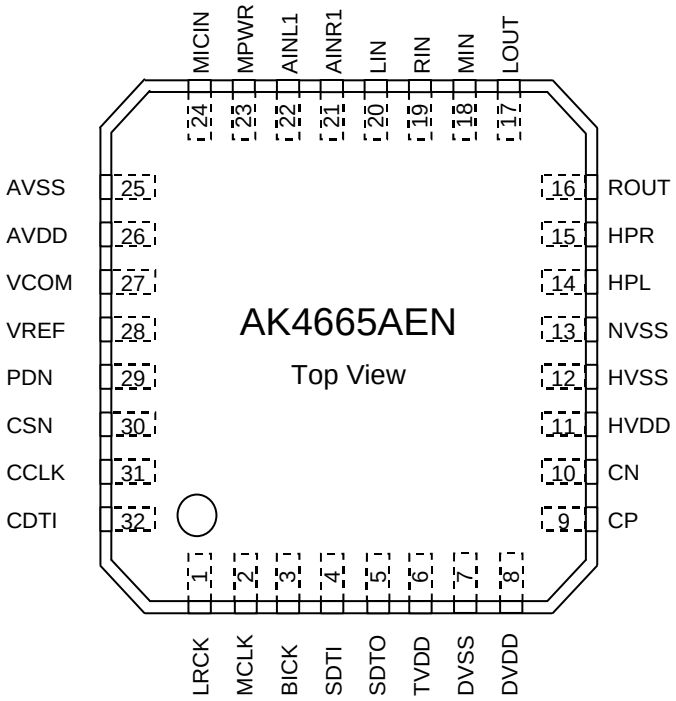


Figure 1. Block Diagram

■ Ordering Guide

AK4665AEN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AKD4665A	Evaluation board for AK4665A	

■ Pin Layout



■ Comparison Table between AK4569 and AK4665A

Function	AK4569	AK4665A
HP-Amp Power Supply	Single Power Supply	Dual Power Supply (Single Power Supply as external case)
HP-Amp Output	8.7mW@16Ω	31mW@16Ω
MIC-Amp	No	Yes
MIC-Power	No	Yes
ALC for Recording	Analog MIC: +32 ~ –19dB, 0.5dB step LINE: +20 ~ –31dB, 0.5dB step	Digital +41.25 ~ –54dB, 0.375dB step
ALC for Playback	No	Yes
Loopback	No	Yes
SDTO Disable	No	Yes
Lineout	Mono	Stereo
MCLK	CMOS or AC coupling input	CMOS input
Power Supply	2.5 ~ 3.6V	AVDD, DVDD, HVDD: 2.6 ~ 3.6V TVDD: 1.6 ~ 3.6V
Package	28QFN (5.2mm x 5.2mm, 0.5mm pitch)	32QFN (5mm x 5mm, 0.5mm pitch)

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LRCK	I	L/R Clock Pin This clock determines which audio channel is currently being output on SDTO pin and input on SDTI pin.
2	MCLK	I	Master Clock Input Pin
3	BICK	I	Serial Bit Clock Pin This clock is used to latch audio data.
4	SDTI	I	Audio Data Input Pin
5	SDTO	O	Audio Data Output Pin SDTO pin goes to DVSS when PDN pin is "L" or PMADC bit is "0".
6	TVDD	-	Digital I/O Power Supply Pin
7	DVSS	-	Digital Ground Pin
8	DVDD	-	Digital Power Supply Pin
9	CP	O	Positive Charge Pump Capacitor Terminal Pin
10	CN	I	Negative Charge Pump Capacitor Terminal Pin
11	HVDD	-	Power Supply Pin for Headphone Amplifier and Charge Pump Circuit
12	HVSS	-	Ground Pin for Headphone Amplifier and Charge Pump Circuit
13	NVSS	O	Negative Voltage Output Pin for Headphone Amplifier and Charge Pump Circuit
14	HPL	O	Lch Headphone Amplifier Output Pin HPL pin goes to AVSS when PMHPL bit is "0".
15	HPR	O	Rch Headphone Amplifier Output Pin HPR pin goes to AVSS when PMHPR bit is "0".
16	ROUT	O	Rch Analog Output Pin
17	LOUT	O	Lch Analog Output Pin
18	MIN	I	Mono Analog Input Pin
19	RIN	I	Rch Analog Input Pin
20	LIN	I	Lch Analog Input Pin
21	AINR1	I	Rch Analog Input 1 Pin for ADC (LINE Input)
22	AINL1	I	Lch Analog Input 1 Pin for ADC (LINE Input)
23	MPWR	O	MIC Power Supply Pin
24	MICIN	I	MIC Input Pin
25	AVSS	-	Analog Ground Pin
26	AVDD	-	Analog Power Supply Pin
27	VCOM	O	Common Voltage Output Pin, 1.2V (typ, respect to AVSS) Normally connected to AVSS pin with a 0.1μF ceramic capacitor in parallel with a 2.2μF electrolytic capacitor. VCOM pin goes to AVSS when PMVCM bit = "0".
28	VREF	O	Reference Voltage Output Pin, 2.1V (typ, respect to AVSS) Reference Voltage Output Pin, 2.1V (typ, respect to AVSS) Normally connected to AVSS pin with a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic capacitor. VREF pin goes to AVSS when PMVCM bit = "0".
29	PDN	I	Power-down Pin When "L", the AK4665A is in power-down mode and is held in reset. The AK4665A should always be reset upon power-up.
30	CSN	I	Control Data Chip Select Pin
31	CCLK	I	Control Clock Input Pin
32	CDTI	I	Control Data Input Pin

Note 1. Do not allow digital input pins except analog input pins (MICIN, AINL1, AINR1, LIN, RIN and MIN pins) to float.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	HPR, HPL, LOUT, ROUT, MICIN, AINR1, AINL1, MPWR	These pins should be open.
Digital	SDTO	This pin should be open.
	SDTI	This pin should be connected to DVSS.

ABSOLUTE MAXIMUM RATING

(AVSS, DVSS, HVSS=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	–0.3	4.0	V
	Digital	DVDD	–0.3	4.0	V
	Digital I/O	TVDD	–0.3	4.0	V
	HP-AMP	HVDD	–0.3	4.0	V
	|AVSS – HVSS| (Note 3)	ΔGND1	-	0.3	V
	|AVSS – DVSS| (Note 3)	ΔGND2	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	–0.3	(AVDD+0.3) or 4.0	V
Digital Input Voltage (Note 5)		VIND	–0.3	(TVDD+0.3) or 4.0	V
Ambient Temperature		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 2. All voltages with respect to ground
Note 3. AVSS, DVSS and HVSS must be connected to the same analog ground plane.
Note 4. MIN, RIN, LIN, MICIN, AINR1, AINL1 pins
Max is smaller value between (AVDD+0.3)V and 4.0V.
Note 5. PDN, CSN, CCLK, CDTI, LRCK, MCLK, BICK, SDTI pins
Max is smaller value between (TVDD+0.3)V and 4.0V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS, HVSS=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	2.6	3.0	3.6	V
	Digital	DVDD	2.6	3.0	3.6	V
	HP-AMP	HVDD	2.6	3.0	3.6	V
	Digital I/O	TVDD	1.6	3.0	DVDD	V
	Difference	AVDD–DVDD	–0.3	0	+0.3	V

Note 2. All voltages with respect to ground
Note 6. If each power supply is gradually switched on or off, some supply current may occur at the other power supply that is still switched on during the supply voltage transition time.

Note: AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=HVDD=TVDD=3.0V, AVSS=DVSS=HVSS=0V; fs=44.1kHz; ALC1=DEM =BOOST=ALC2=OFF; ATTL=ATTR=ATTS=0dB; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	Typ	max	Units
ADC Resolution		-	-	20	bit
MIC Amplifier: MICIN pin					
Input Resistance	MGAIN1-0 bits = "00" or "01"	40	60	80	kΩ
	MGAIN1-0 bits = "10" or "11"	20	30	40	kΩ
Input Voltage	MGAIN1-0 bits = "00"	-	1.5	-	Vpp
	MGAIN1-0 bits = "01"	-	3.0	-	Vpp
	MGAIN1-0 bits = "10"	-	0.75	-	Vpp
	MGAIN1-0 bits = "11"	-	0.047	-	Vpp
Gain	MGAIN1-0 bits = "00"	-	0	-	dB
	MGAIN1-0 bits = "01"	-	–6	-	dB
	MGAIN1-0 bits = "10"	-	+6	-	dB
	MGAIN1-0 bits = "11"	-	+30	-	dB
MIC Power Supply: MPWR pin					
Output Voltage		1.8	2.0	2.2	V
Load Resistance		2	-	-	kΩ
Load Capacitance		-	-	30	pF
ADC Analog Input Characteristics: AINL1/AINR1 pins → ADC → IVOL, IVOL=0dB, ALC1=OFF					
S/(N+D) (–1dBFS)		78	90	-	dB
D-Range (–60dBFS, A-weighted)		84	94	-	dB
S/N (A-weighted)		84	94	-	dB
Interchannel Isolation		80	100	-	dB
Interchannel Gain Mismatch		-	0.2	0.5	dB
Gain Drift		-	200	-	ppm/°C
Input Voltage		1.35	1.5	1.65	Vpp
Input Resistance		40	60	80	kΩ
Power Supply Rejection (Note 7)		-	50	-	dB
DAC Resolution				20	bit
Headphone-Amp: (HPL/HPR pins) (Note 8) R_L =16Ω, HPG bit = "0"					
S/(N+D)	0dBFS Output, HPG bit = "0", Po=17mW@16Ω	40	60	-	dB
	–3dBFS Output, HPG bit = "1", Po=31mW@16Ω	-	20	-	dB
	0dBFS Output, HPG bit = "1", R_L=10kΩ	-	80	-	dB
D-Range (–60dBFS Output, A-weighted)		80	88	-	dB
S/N (A-weighted)		80	88	-	dB
Interchannel Isolation		60	80	-	dB
Interchannel Gain Mismatch		-	0.2	1.0	dB
Gain Drift		-	200	-	ppm/°C
Output Voltage	0dBFS Output, HPG bit = "0", R_L=16Ω	1.35	1.5	1.65	Vpp
	–3dBFS Output, HPG bit = "1", R_L=16Ω	-	2.0	-	Vpp
	0dBFS Output, HPG bit = "1", R_L=10kΩ	-	2.83	-	Vpp
Load Resistance		16	-	-	Ω
Load Capacitance		-	-	300	pF
Power Supply Rejection (Note 7)		-	50	-	dB

Note 7. PSR is applied to AVDD, DVDD and HVDD with 1kHz, 50mVpp.

Note 8. DACHL=DACHR bits = "1", MINHL=MINHR=LINHL=RINHR bits = "0", ATTL7-0=ATTR7-0 bits=0dB.

Parameter	min	Typ	max	Units
Stereo Line Output: (LOUT/ROUT pins) (Note 9)				
S/(N+D) (0dBFS Output)	72	84	-	dB
S/N (A-weighted)	80	88	-	dB
Interchannel Isolation	70	90	-	dB
Interchannel Gain Mismatch	-	0.2	0.5	dB
Gain Drift	-	200	-	ppm/°C
Output Voltage	1.35	1.5	1.65	Vpp
Load Resistance (Note 10)	10	-	-	kΩ
Load Capacitance	-	-	30	pF
Power Supply Rejection (Note 7)	-	50	-	dB
Output Volume (OPGA): (LOUT/ROUT pins)				
Step Size	1	2	3	dB
Gain Control Range	–30		0	dB
Analog Input: (LIN/RIN/MIN pins)				
Input Resistance	100	200	300	kΩ
Gain				
LIN→HPL, RIN→HPR, HPG bit = "0", LING bit = "0"	–1	0	+1	dB
LIN→HPL, RIN→HPR, HPG bit = "0", LING bit = "1"	-	–12	-	dB
LIN→HPL, RIN→HPR, HPG bit = "1", LING bit = "0"	-	+5.5	-	dB
LIN→HPL, RIN→HPR, HPG bit = "1", LING bit = "1"	-	–6.5	-	dB
MIN→HPL/HPR, HPG bit = "0"	–1	0	+1	dB
MIN→HPL/HPR, HPG bit = "1"	-	+5.5	-	dB
LIN/MIN→LOUT, RIN/MIN→ROUT, ATTS=0dB	–1	0	+1	dB
Power Supplies				
Power Supply Current: AVDD+DVDD+TVDD+HVDD				
Normal Operation (PDN pin = "H") (Note 11)	-	20	30	mA
Power-Down Mode (PDN pin = "L") (Note 12)	-	1	100	μA

Note 9. DACL=DACR bits = "1", LINL=RINR=MINL=MINR bits = "0", ATTL7-0=ATTR7-0=ATTS3-0 bits=0dB.

Note 10. AC Load

Note 11. All blocks are powered-up (MVCM=PMADC=PMDAC=PMHPL=PMHPR=PMLO=PMCP=PMMP bits = "1"), and HP-AMP output is off. Output current of MPWR pin is 0mA.
AVDD=12mA(typ), DVDD+TVDD=2mA(typ), HVDD=6mA(typ).
14mA(typ) at playback only (PMVCM=PMDAC=PMHPL=PMHPR=PMLO=PMCP bits = "1", PMADC bit = "0"), AVDD=6.5mA(typ), DVDD+TVDD=1.5mA(typ), HVDD=6mA(typ).

Note 12. All digital input pins including clock pins (MCLK, BICK and LRCK) are held at DVDD or DVSS. PDN pin is held at DVSS.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD=2.6 ~ 3.6V; TVDD=1.6~ 3.6V; fs=44.1kHz; DEM=OFF; BOOST=OFF)

Parameter			Symbol	min	typ	max	Units
ADC Digital Filter (LPF):							
Passband (Note 13)	±0.16dB		PB	0	-	17.3	kHz
	–0.66dB			-	19.4	-	kHz
	–1.1dB			-	19.9	-	kHz
	–6.9dB			-	22.1	-	kHz
Stopband (Note 13)			SB	26.1	-	-	kHz
Passband Ripple			PR	-	-	±0.1	dB
Stopband Attenuation			SA	73	-	-	dB
Group Delay (Note 14)			GD	-	17	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
ADC Digital Filter (HPF):							
Frequency Response (Note 13)	–3dB		FR	-	3.4	-	Hz
	–0.5dB			-	10	-	Hz
	–0.1dB			-	22	-	Hz
DAC Digital Filter: (Note 15)							
Passband (Note 13)	±0.1dB		PB	0	-	19.6	kHz
	–0.7dB			-	20.0	-	kHz
	–6.0dB			-	22.05	-	kHz
Stopband (Note 13)			SB	25.2	-	-	kHz
Passband Ripple			PR	-	-	±0.01	dB
Stopband Attenuation			SA	59	-	-	dB
Group Delay (Note 14)			GD	-	17.5	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter: (Note 15)							
Frequency Response: 0 ~ 20.0kHz			FR	-	±1.0	-	dB
Analog Filter: (Note 16)							
Frequency Response: 0 ~ 20.0kHz			FR	-	±1.0	-	dB
BOOST Filter: (Note 17)							
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 13. The passband and stopband frequencies scale with fs.
For example (DAC), PB=0.44*fs(@±0.1dB), SB=0.57*fs(@–59dB).

Note 14. This is the calculated delay time caused by digital filtering. This time is measured from the input of analog signal to setting the 20 bit data of both channels on input register to the output register of ADC. For DAC, this time is from setting the 20 bit data of both channels on input register to the output of analog signal.

Note 15. BOOST OFF (BST1-0 bits = "00")

Note 16. LIN→HPL, RIN→HPR, MIN→HPL/HPR.

Note 17. These frequency responses scale with fs. If high-level signal is input, the AK4665A clips at low frequency.

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD = 2.6 ~ 3.6V; TVDD=1.6~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤TVDD≤3.6V	VIH	70%TVDD	-	-	V
	1.6V≤TVDD<2.2V	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	2.2V≤TVDD≤3.6V	VIL	-	-	30%TVDD	V
	1.6V≤TVDD<2.2V	VIL	-	-	20%TVDD	V
High-Level Output Voltage	(Iout= –100μA)	VOH	TVDD–0.4	-	-	V
Low-Level Output Voltage	(Iout= 100μA)	VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD = 2.6 ~ 3.6V; TVDD=1.6~ 3.6V; CL = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fCLK	2.048	-	24.576	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
LRCK Timing					
Frequency	fs	8	44.1	48	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing (Note 18)					
BICK Period	tBCK	325.5	-	-	ns
BICK Pulse Width Low	tBCKL	130	-	-	ns
Pulse Width High	tBCKH	130	-	-	ns
LRCK Edge to BICK "↑" (Note 19)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	50	-	-	ns
LRCK to SDTO(MSB)	tLRS	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 20)	tPD	150	-	-	ns
PMADC "↑" to SDTO valid (Note 21)	tPDV	-	2081	-	1/fs

Note 18. Refer to "Serial Data Interface".

Note 19. BICK rising edge must not occur at the same time as LRCK edge.

Note 20. The AK4665A can be reset by bringing PDN= "L" to "H" only upon power up.

Note 21. This is the count of LRCK "↑" from PMADC bit="1".

■ Timing Diagram

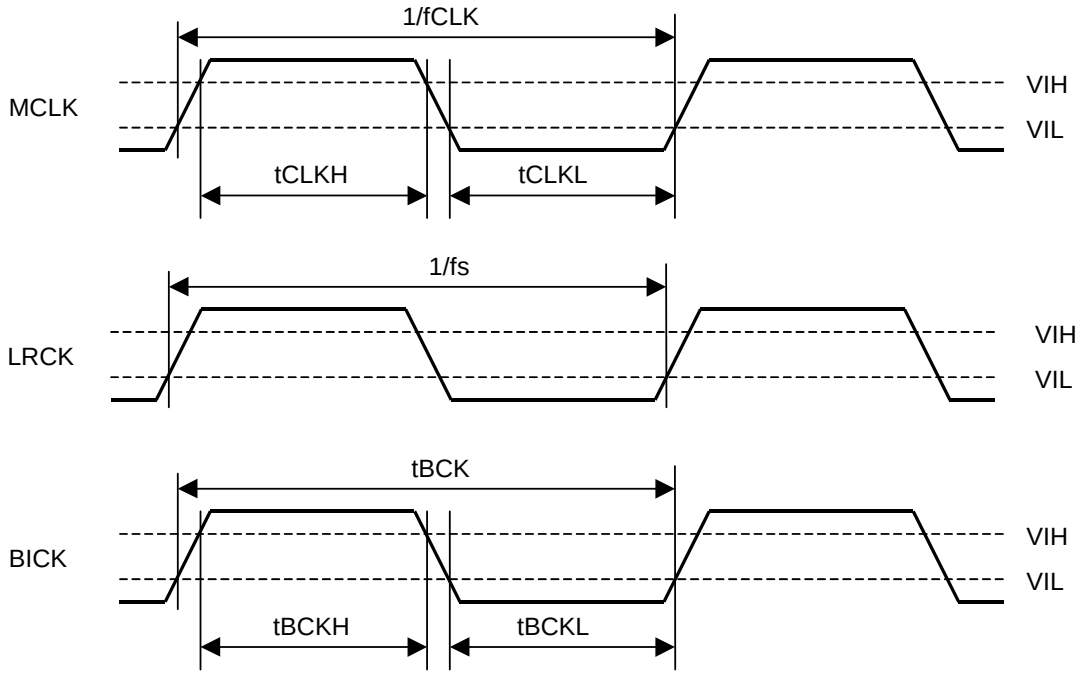


Figure 2. Clock Timing

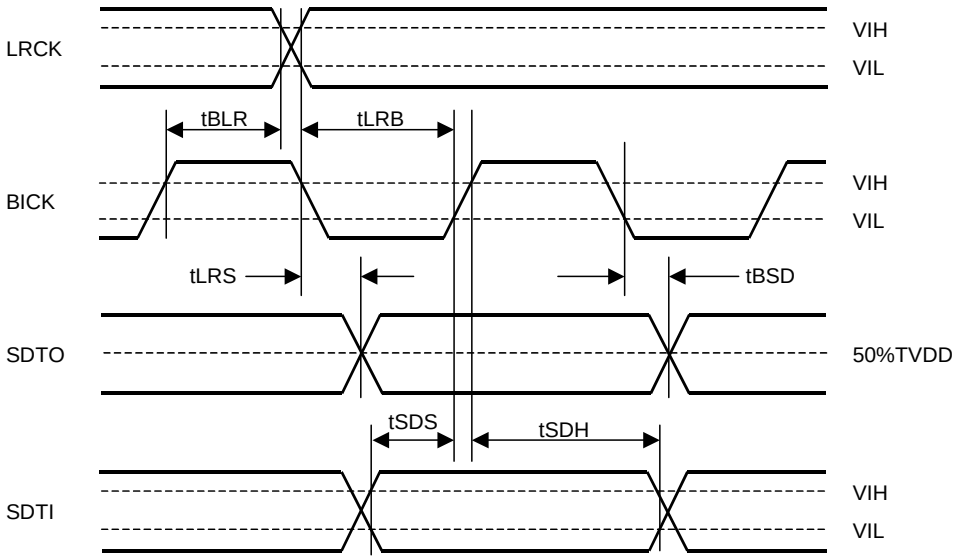


Figure 3. Serial Interface Timing

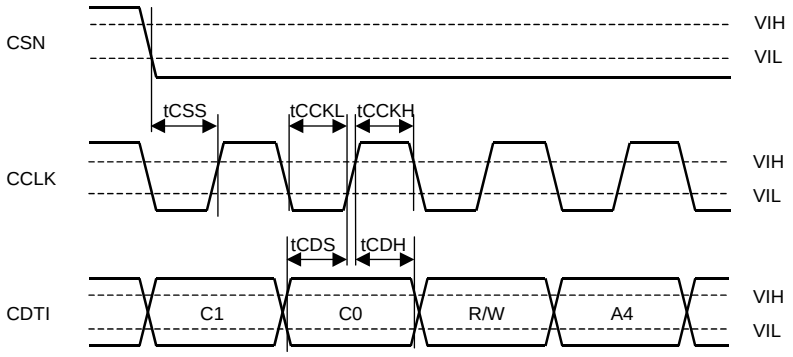


Figure 4. WRITE Command Input Timing

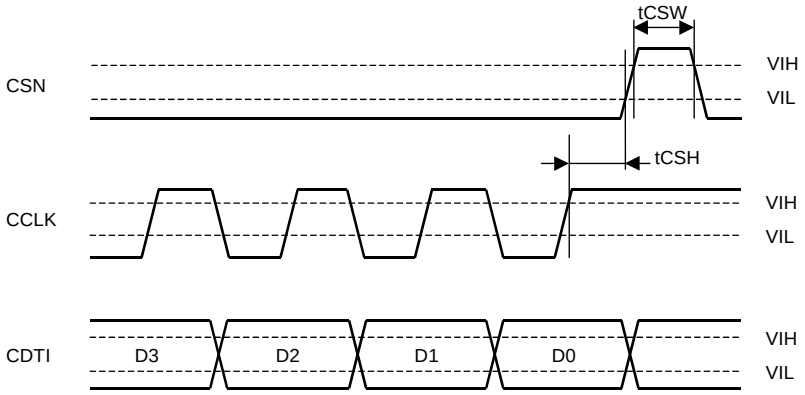


Figure 5. WRITE Data Input Timing

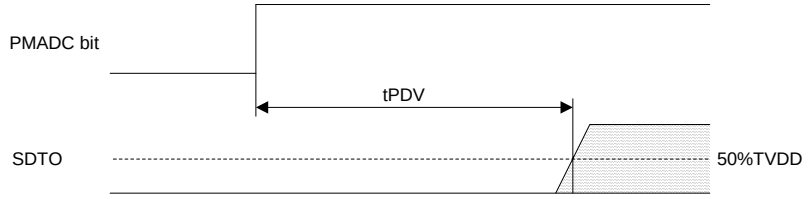


Figure 6. Power Down & Reset Timing 1

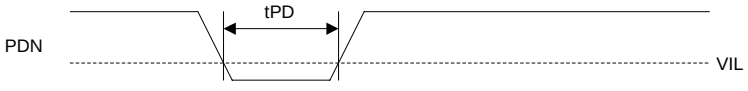


Figure 7. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4665A are MCLK (256fs/512fs), LRCK (fs) and BICK. The master clock (MCLK) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. The sampling frequency is selected by FS3-0 bits (refer to Table 1). The frequency of MCLK is detected automatically, and the internal master clock becomes the appropriate frequency. Table 2 shows system clock example.

FS3	FS2	FS1	FS0	fs	
0	0	0	0	44.1kHz	Default
0	0	0	1	32kHz	
0	0	1	0	48kHz	
1	0	0	0	22.05kHz	
1	0	0	1	16kHz	
1	0	1	0	24kHz	
1	1	0	0	11.025kHz	
1	1	0	1	8kHz	
1	1	1	0	12kHz	
Others				N/A	

Table 1. Sampling Frequency

LRCK	MCLK (MHz)		BICK (MHz)
fs	256fs	512fs	64fs
8kHz	2.048	4.096	0.512
11.025kHz	2.8224	5.6448	0.7056
12kHz	3.072	6.144	0.768
16kHz	4.096	8.192	1.024
22.05kHz	5.6448	11.2896	1.4112
24kHz	6.144	12.288	1.536
32kHz	8.192	16.384	2.048
44.1kHz	11.2896	22.5792	2.8224
48kHz	12.288	24.576	3.072

Table 2. Systems Clock Example

External clocks (MCLK, BICK and LRCK) are needed to operate ADC, DAC, ALC2 or HP-Amp. External clocks are also needed for each path setting of HP-Amp (DACHL, LINHL, MINHL, DACHR, RINHR, MINHR and HPMTN bits) and Lineout (DACL, LINL, MINL, DACR, RINR and MINR bits) when MOFF8 bit = “0” or MOFF9 bit = “0”. All external clocks (MCLK, BICK and LRCK) should always be present whenever ADC, DAC, ALC2 or HP-Amp is in normal operation mode (PMADC bit = “1”, PMDAC bit = “1”, PMLO=ALC2 bits = “1” or PMCP=PMHPL=PMHPR bits = “1”). If these clocks are not provided, the AK4665A may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4665A should be placed in power-down mode (PDN pin = “L” or PMADC=PMDAC=ALC2=PMCP=PMHPL=PMHPR bits = “0”).

For low sampling rates, outband noise causes S/N to degrade. S/N is improved by setting DFS bit to "1". Table 3 shows S/N of DAC output for both HP-Amp and Stereo-Lineout. When DFS bit is "1", MCLK needs 512fs.

DFS	fs	MCLK	S/N (fs=8kHz, BW=20kHz, A-weighted)		
			HP-amp	Lineout	
0	8kHz~48kHz	256fs/512fs	84dB	84dB	Default
1	8kHz~24kHz	512fs	90dB	88dB	

Table 3. Relationship among fs, MCLK frequency and S/N of HP-amp and Lineout

■ Serial Data Interface

The AK4665A interfaces with external systems via the BICK, LRCK, SDTO and SDTI pins. Four data formats are available and are selected by setting DIF1-0 bits (Table 4). Mode 0 of SDTI is compatible with existing 16bit DAC and digital filters. Mode 1 of SDTI is a 20bit version of Mode 0. Mode 2 of SDTI is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In SDTI Modes 2 and 3, the following formats are also valid: 16-bit data followed by four zeros and 18-bit data followed by two zeros. In all modes, the serial data is MSB first and 2's complement format.

Mode	DIF1	DIF0	SDTO	SDTI	BICK	LRCK	
0	0	0	20bit, MSB justified	16bit, LSB justified	≥ 32fs	H/L	
1	0	1	20bit, MSB justified	20bit, LSB justified	≥ 40fs	H/L	
2	1	0	20bit, MSB justified	20bit, MSB justified	≥ 40fs	H/L	Default
3	1	1	IIS (I^2S)	IIS (I^2S)	≥ 40fs	L/H	

Table 4. Audio Data Format

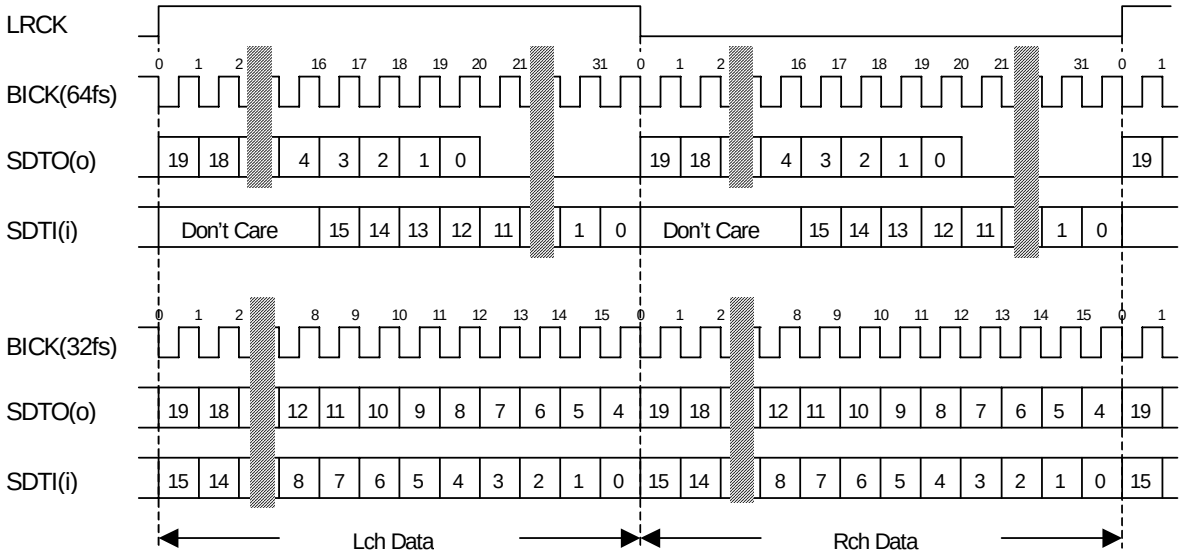


Figure 8. Mode 0 Timing

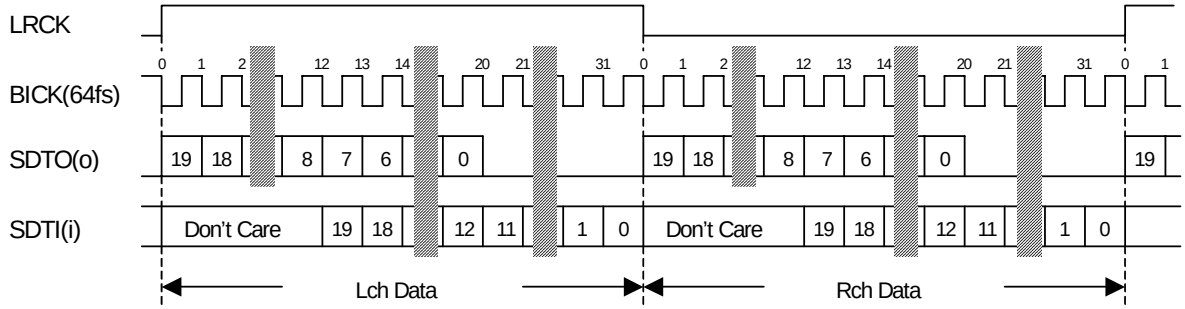


Figure 9. Mode 1 Timing

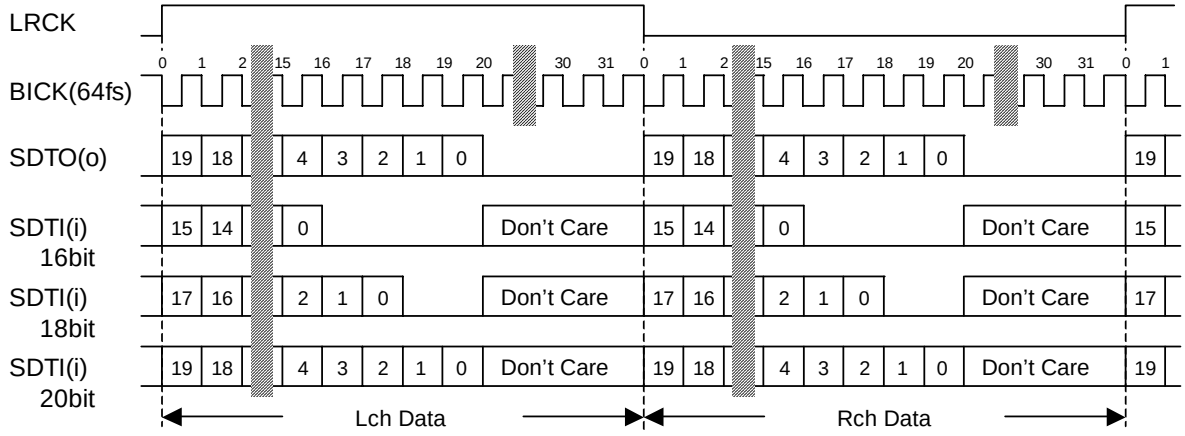


Figure 10. Mode 2 Timing

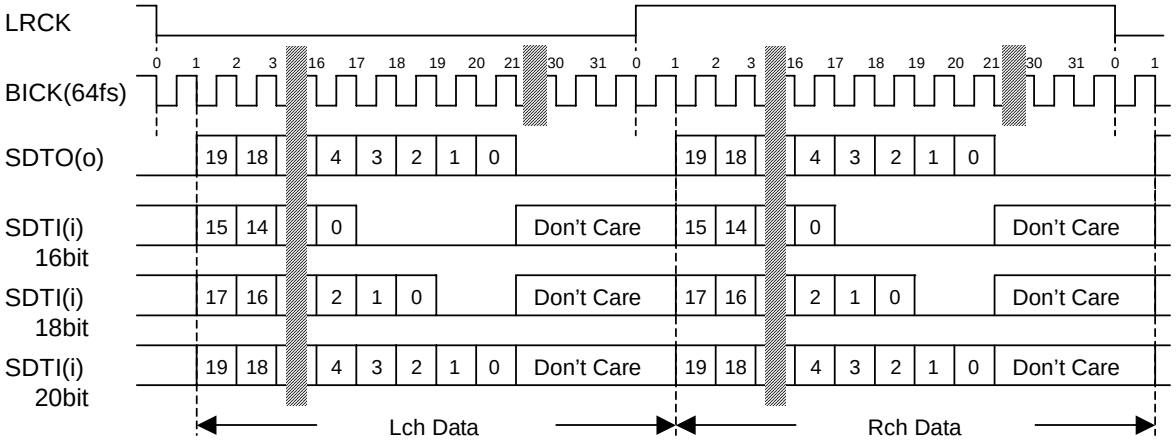


Figure 11. Mode 3 Timing

■ Digital High Pass Filter

The AK4665A has a Digital High Pass Filter (HPF) to cancel DC-offsets in ADC. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz. This filter scales with the sampling frequency (fs).

■ Mono-MIC Gain Amplifier (MICIN pin)

The AK4665A has a gain amplifier for mono-mic input. The gain of Mic-Amp is selected by MGAIN1-0 bits (see Table 5). The input impedance is 60kΩ(typ) at MGAIN1-0 bits = "00", "01" and 30kΩ(typ) at MGAIN1-0 bits = "10", "11".

MGAIN1 bit	MGAIN0 bit	Input Gain	Input Resistance	
0	0	0dB	60kΩ (typ)	Default
0	1	–6dB	60kΩ (typ)	
1	0	+6dB	30kΩ (typ)	
1	1	+30dB	30kΩ (typ)	

Table 5. MIC Input Gain

■ MIC Power (MPWR pin)

When PMMP bit is "1", MPWR pin supplies power for the microphone. This output voltage is 2.0V(typ), and the load resistance is minimum 2kΩ. Capacitor must not be connected directly to MPWR pin (see Figure 12).

PMMP bit	MPWR pin	
0	Hi-Z	Default
1	Output	

Table 6. MIC Power

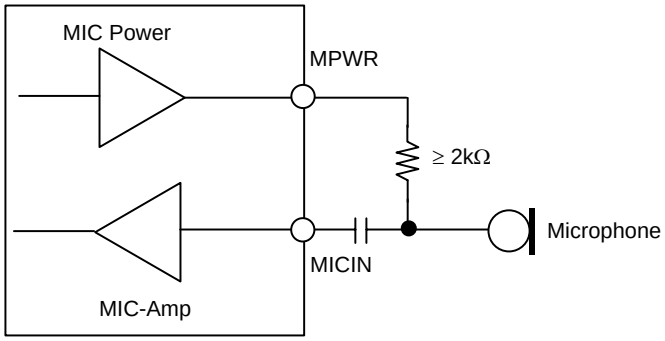


Figure 12. MIC Block Circuit

■ Input Selector

The AK4665A has 2-input selector for ADC. ADC input is selected by INL1, INR1 and INL2 bits.

INL1 bit	INR1 bit	INL2 bit	Lch	Rch	
1	1	0	AINL1	AINR1	Default
0	0	1	MICIN	MICIN	

Table 7. Input Selector

The input impedance of stereo line input (AINL1 and AINR1 pins) are 60kΩ(typ).

■ Mono-Record Mode

When ADM bit is “1”, ADC Lch data is output on both Lch and Rch of SDTO.

ADM bit	Lch	Rch	
0	L	R	Default
1	L	L	

Table 8. Mono-Record Mode

■ ALC1 Operation (MIC-ALC)

The ALC1 (Automatic Level Control) is done by ALC1 block when ALC1 bit is "1".

1. ALC1 Limiter Operation

During the ALC1 limiter operation, when either Lch or Rch exceeds the ALC1 limiter detection level (LMTH1-0 bits: Table 9), the IVOL value (same value for Lch and Rch) is attenuated automatically by the ALC1 limiter ATT step (LMAT1-0 bits: Table 10).

When ZELMN bit is "0" (zero crossing detection is enabled), the IVOL value is changed by the ALC1 limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both the ALC1 limiter and recovery operation (Table 11).

When ZELMN bit is "1" (zero crossing detection is disabled), the IVOL value is immediately (period: 1/fs) changed by the ALC1 limiter operation. Attenuation step is fixed to 1 step regardless as the setting of LMAT1-0 bits.

After completing the attenuation operation, unless ALC1 bit is changed to "0", the operation repeats when the input signal level exceeds ALC1 limiter detection level.

LMTH1	LMTH0	ALC1 Limier Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	0	ALC1 Output ≥ –4.1dBFS	–4.1dBFS > ALC1 Output ≥ –6.0dBFS	Default
0	1	ALC1 Output ≥ –6.0dBFS	–6.0dBFS > ALC1 Output ≥ –8.5dBFS	
1	0	ALC1 Output ≥ –8.5dBFS	–8.5dBFS > ALC1 Output ≥ –12dBFS	
1	1	ALC1 Output ≥ –10.1dBFS	–10.1dBFS > ALC1 Output ≥ –14.5dBFS	

Table 9. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

ZELMN	LMAT1	LMAT0	ALC1 Limiter ATT Step		
0	0	0	1 step	0.375dB	Default
	0	1	2 step	0.750dB	
	1	0	4 step	1.500dB	
	1	1	8 step	3.000dB	
1	x	x	1 step	0.375dB	

Table 10. ALC1 Limiter ATT Step (x: Don't care)

FS3	FS2	FS1	FS0	ALC1 Zero Cross Timeout				
				ZTM=00 (Default)	ZTM=01	ZTM=10	ZTM=11	
0	0	0	0	384/fs (8.7ms)	768/fs (17.4ms)	1536/fs (34.8ms)	3072/fs (69.7ms)	Default
0	0	0	1	256/fs (8.0ms)	512/fs (16.0ms)	1024/fs (32.0ms)	2048/fs (64.0ms)	
0	0	1	0	384/fs (8.0ms)	768/fs (16.0ms)	1536/fs (32.0ms)	3072/fs (64.0ms)	
1	0	0	0	192/fs (8.7ms)	384/fs (17.4ms)	768/fs (34.8ms)	1536/fs (69.7ms)	
1	0	0	1	128/fs (8.0ms)	256/fs (16.0ms)	512/fs (32.0ms)	1024/fs (64.0ms)	
1	0	1	0	192/fs (8.0ms)	384/fs (16.0ms)	768/fs (32.0ms)	1536/fs (64.0ms)	
1	1	0	0	96/fs (8.7ms)	192/fs (17.4ms)	384/fs (34.8ms)	768/fs (69.7ms)	
1	1	0	1	64/fs (8.0ms)	128/fs (16.0ms)	256/fs (32.0ms)	512/fs (64.0ms)	
1	1	1	0	96/fs (8.0ms)	192/fs (16.0ms)	384/fs (32.0ms)	768/fs (64.0ms)	
Others				N/A				

Table 11. ALC1 Zero Crossing Timeout Period

2. ALC1 Recovery Operation

The ALC1 recovery operation waits for WTM1-0 bits (Table 12) to be set after completing the ALC1 limiter operation. If the input signal does not exceed "ALC1 recovery waiting counter reset level" (Table 9) during the wait time, the ALC1 recovery operation is done. The IVOL value (same value for Lch and Rch) is automatically incremented by RGAIN1-0 bits (Table 13) up to the set reference level (Table 14) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 11). The ALC1 recovery operation is done at a period set by WTM1-0 bits. When zero cross is detected at both channels during the wait period set by WTM1-0 bits, the ALC1 recovery operation waits until WTM1-0 period and the next recovery operation is done. The setting period of WTM1-0 bits should be the same as ZTM1-0 bits or longer time.

For example, when the current IVOL value is 30H and RGAIN1-0 bits are set to "01", the IVOL is changed to 32H by the ALC1 limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REF7-0), the IVOL values are not increased.

When
"ALC1 recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC1 recovery operation, the waiting timer of ALC1 recovery operation is reset. When
"ALC1 recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC1 recovery operation starts.

The ALC1 operation corresponds to the impulse noise. When the impulse noise is input, the ALC1 recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation.

FS3	FS2	FS1	FS0	ALC1 Recovery Time				
				WTM=00 (Default)	WTM=01	WTM=10	WTM=11	
0	0	0	0	384/fs (8.7ms)	768/fs (17.4ms)	1536/fs (34.8ms)	3072/fs (69.7ms)	Default
0	0	0	1	256/fs (8.0ms)	512/fs (16.0ms)	1024/fs (32.0ms)	2048/fs (64.0ms)	
0	0	1	0	384/fs (8.0ms)	768/fs (16.0ms)	1536/fs (32.0ms)	3072/fs (64.0ms)	
1	0	0	0	192/fs (8.7ms)	384/fs (17.4ms)	768/fs (34.8ms)	1536/fs (69.7ms)	
1	0	0	1	128/fs (8.0ms)	256/fs (16.0ms)	512/fs (32.0ms)	1024/fs (64.0ms)	
1	0	1	0	192/fs (8.0ms)	384/fs (16.0ms)	768/fs (32.0ms)	1536/fs (64.0ms)	
1	1	0	0	96/fs (8.7ms)	192/fs (17.4ms)	384/fs (34.8ms)	768/fs (69.7ms)	
1	1	0	1	64/fs (8.0ms)	128/fs (16.0ms)	256/fs (32.0ms)	512/fs (64.0ms)	
1	1	1	0	96/fs (8.0ms)	192/fs (16.0ms)	384/fs (32.0ms)	768/fs (64.0ms)	
Others				N/A				

Table 12. ALC1 Recovery Operation Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.375dB	Default
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 13. ALC1 Recovery GAIN Step

REF7-0	GAIN(dB)	Step	
FFH	+41.25	0.375dB	
FEH	+40.875		
FDH	+40.5		
:	:		
E2H	+30.375		
E1H	+30.0		Default
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54.0		
00H	MUTE		

Table 14. Reference Level at ALC1 Recovery Operation

3. Example for ALC1 Operation

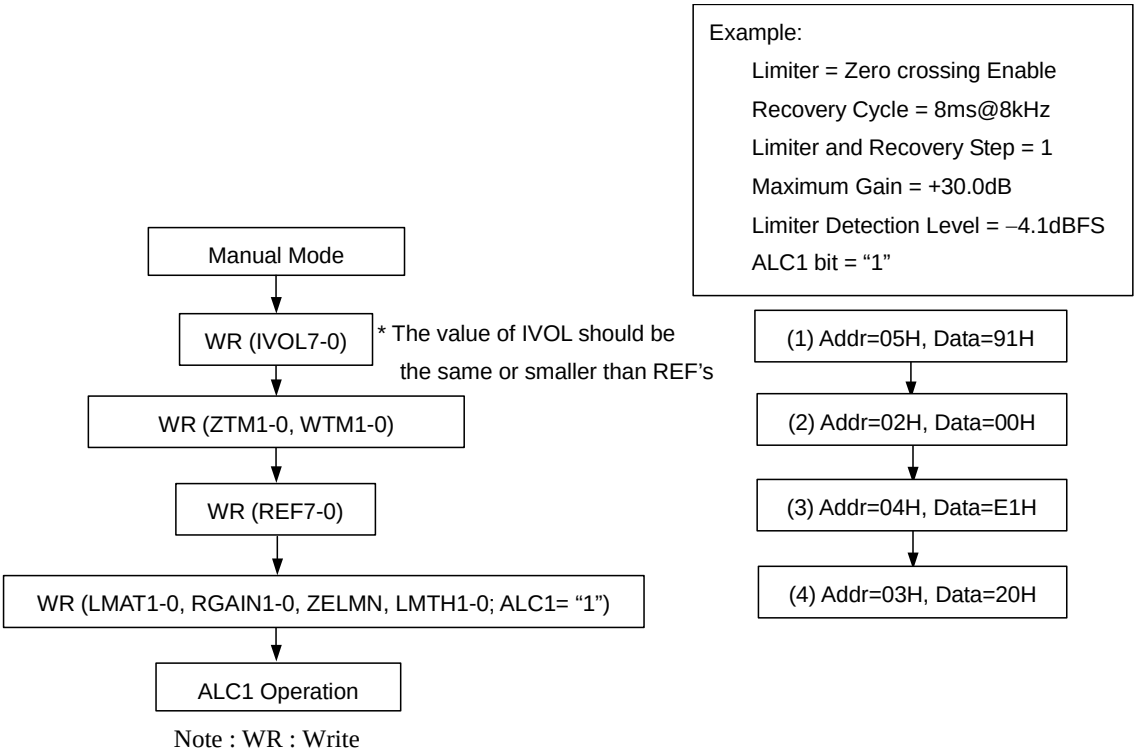
Table 15 shows the examples of the ALC1 setting.

Register Name	Comment	Data	fs		
			8kHz 16kHz 32kHz	11.025kHz 22.05kHz 44.1kHz	12kHz 24kHz 48kHz
LMTH	Limiter detection Level	00	–4.1dBFS	–4.1dBFS	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	Enable	Enable
ZTM1-0	Zero crossing timeout period	00	8ms	8.7ms	8ms
WTM1-0	Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits	00	8ms	8.7ms	8ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	+30dB	+30dB
IVOL7-0	Gain of IVOL	91H	0dB	0dB	0dB
LMAT1-0	Limiter ATT step	00	0.375dB	0.375dB	0.375dB
RGAIN1-0	Recovery GAIN step	00	0.375dB	0.375dB	0.375dB
ALC1	ALC1 enable	1	Enable	Enable	Enable

Table 15. Example for the ALC1 setting

The following registers should not be changed during the ALC1 operation. These bits should be changed after the ALC1 operation is finished by ALC1 bit = “0” or PMADC bit = “0”.

- LMTH, LMAT1-0, WTM1-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN



Note : WR : Write

Figure 13. Registers set-up sequence at ALC1 operation

■ Input Digital Volume (IVOL: Manual Mode)

The input digital volume becomes a manual mode when ALC1 bit is “0”. This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC1 operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC1 operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVOL7-0 bits set the gain of the volume control (Table 16). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits.

If IVOL7-0 bits are written during PMADC bit = “0”, IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADC bit is changed to “1”.

IVOL7-0	GAIN (dB)	Step	
FFH	+41.25	0.375dB	
FEH	+40.875		
FDH	+40.5		
:	:		
92H	+0.375		
91H	0.0		Default
90H	–0.375		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 16. Input Digital Volume

When writing to IVOL7-0 bits continuously, the control register should be written by an interval more than zero crossing timeout. If not, the IVOL is not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVOL, the write operation is ignored and zero crossing counter is not reset. Therefore, IVOL can be written by an interval less than zero crossing timeout.

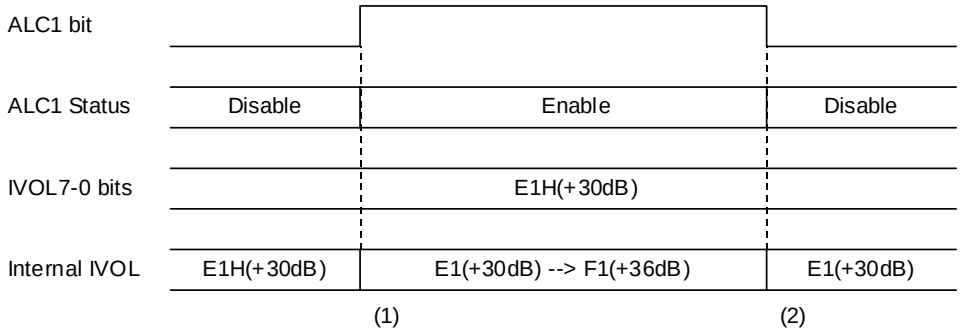


Figure 14. IVOL value during ALC1 operation

(1) ALC1 operation starts from the IVOL value when ALC1 bit is changed to "1". The wait time from ALC1 bit = "1" to ALC1 operation start by IVOL7-0 bits is at most recovery time (WTM1-0 bits) plus zero cross timeout period (ZTM1-0 bits).
(2) Writing to IVOL register (05H) is ignored during ALC1 operation. After ALC1 is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC1 is enabled again, ALC1 bit should be set to "1" by an interval more than zero crossing timeout period after ALC1 bit = "0".

■ ADC Output ON/OFF (SDTO pin)

SDTO pin becomes "L" when SDOD bit is "1".

SDOD bit	SDTO pin	
0	Output	Default
1	"L"	

Table 17. ADC Output ON/OFF

■ Digital Loopback

ADC output data is internally passed to DAC when LOOP bit is "1". The external input data to SDTI pin is ignored. This operation is independent of SDOD bit.

LOOP bit	DAC Input	
0	SDTI pin	Default
1	ADC Output	

Table 18. Digital Loopback

■ Digital Output Volume (DATT)

The AK4665A has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to –127dB or MUTE) for each channel (DATT). At DATTC bit = "1", ATTL7-0 bits control both Lch and Rch attenuation levels. At DATTC bit = "0", ATTL7-0 bits control the Lch level and ATTR7-0 bits control the Rch level.

ATTL/R7-0	Attenuation	
FFH	0dB	
FEH	–0.5dB	
FDH	–1.0dB	
FCH	–1.5dB	
:	:	
:	:	
02H	–126.5dB	
01H	–127.0dB	
00H	MUTE (–∞)	Default

Table 19. Digital Volume Code Table

The ATS bit sets the transition time between set values of ATTL/R7-0 bits as either 1061/fs or 256/fs (Table 20). When ATS bit is "0", a soft transition between the set values occurs (1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from "FFH" (0dB) to "00H" (MUTE). When PDN pin is "L", ATTL/R bits are initialized to "00H". The ATTL/R bits are "00H" when PMDAC bit is "0". When PMDAC bit returns to "1", the ATTL/R bits fade to their current value.

ATS bit	Transition time between ATTL/R7-0 bits = 00H and FFH			
	Setting	fs=8kHz	fs=44.1kHz	
0	1061/fs	133ms	24ms	Default
1	256/fs	32ms	6ms	

Table 20. Transition Time Setting of Digital Output Volume

■ Soft Mute (SMUTE)

Soft mute operation is performed in the digital domain. When SMUTE bit goes to "1", the output signal is attenuated by −∞ ("0") via the cycle set by ATS bit (Table 20). When SMUTE bit returns to "0", the mute is cancelled and the output attenuation gradually changes to 0dB via the cycle set by ATS bit. If the soft mute is cancelled within the cycle set by ATS bit after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

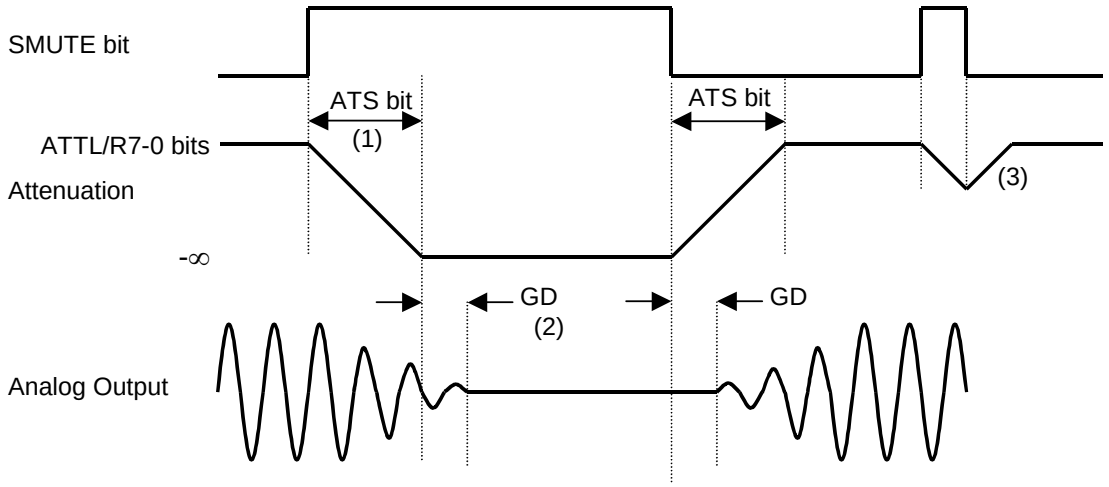


Figure 15. Soft Mute Function

Notes:

(1) The output signal is attenuated until −∞ ("0") by the cycle set by ATS bit.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle set by ATS bit, the attenuation is discontinued and returned to the setting value by the same cycle.

■ De-emphasis Filter (DEM)

The AK4665A includes a digital de-emphasis filter (tc = 50/15μs) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting DEM1-0 bits (Table 21).

DEM1	DEM0	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 21. De-emphasis Control

■ Bass Boost Function (BOOST)

By controlling BST1-0 bits, the bass boost signal can be output from DAC. The setting value is common in Lch and Rch (Table 22). The frequency of bass boost filter scales sampling frequency.

BST1	BST0	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 22. Bass Boost

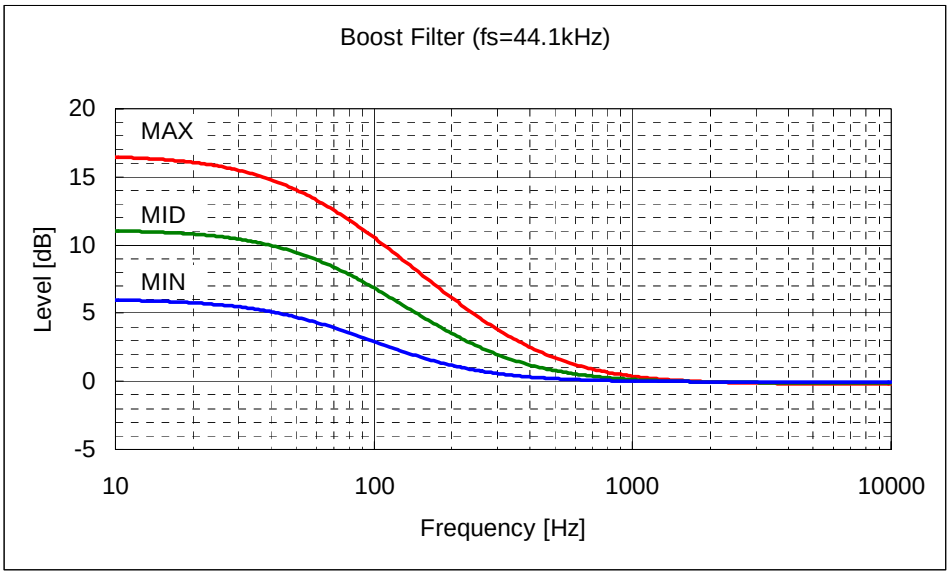


Figure 16. Bass Boost Frequency (fs=44.1kHz)

■ External Analog Input (LIN, RIN, MIN pins)

The input signals from LIN/RIN/MIN pins can be output from headphone and lineout. LIN/RIN/MIN input buffers are 2nd order LPF (fc=50kHz(typ)) in order to attenuate the high frequency noise of external analog input signals. DC component of input signal should be cut by external capacitor. The cut-off frequency (fc) of HPF depends on the internal input resistance (Ri) and the external capacitor value (C): $fc=1/(2\pi RiC)$. The input resistance is 200kΩ±50%, The gain is 0dB(typ) for both Lineout and HP-Amp (HPG=LING bits = "0").

When HPG bit = "1" and LING bit = "0", the gain of HP-Amp is –5.5dB(typ).

When HPG bit = "0" and LING bit = "1", the gain of LIN/RIN → HPL/HPR paths are –12dB(typ).

LIN/RIN/MIN input buffers powered-up when either bits of PMHPL, PMHPR and PMLO bits become "1".

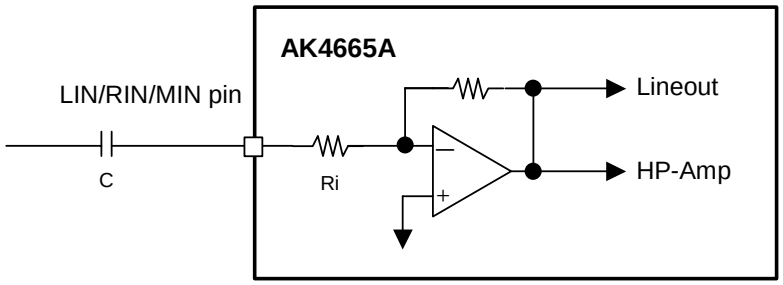


Figure 17. External Analog input circuit

■ ALC2 Operation (LOUT, ROUT pins)

The ALC2 (Automatic Level Control) of stereo line out is done by ALC2 block when ALC2 bit is "1". The gain of ALC2 block is fixed to 0dB when ALC2 bit is "0".

(1) ALC2 Limiter Operation

During the ALC2 limiter operation, when the ALC2 output level exceeds the ALC2 limiter detection level (LMTHP bit: Table 23), the volume value of ALC2 is attenuated automatically by the amount defined by the ALC2 limiter ATT step (LMATP1-0 bits: Table 24). The volume value is changed without zero crossing detection. LTMP1-0 bits (Table 25) set the ALC2 limiter operation period.

LMTHP	ALC2 Limiter Detection Level	ALC2 Recovery Waiting Counter Reset Level	
0	ALC2 Output ≥ –7.5dBV	–7.5dBV > ALC2 Output ≥ –9.5dBV	Default
1	ALC2 Output ≥ –11.5dBV	–11.5dBV > ALC2 Output ≥ –13.5dBV	

Table 23. ALC2 Limiter Detection Level / Recovery Waiting Counter Reset Level

LMATP1	LMATP0	ATT STEP		
0	0	1 step	0.5dB	Default
0	1	2 step	1.0dB	
1	0	3 step	1.5dB	
1	1	4 step	2.0dB	

Table 24. ALC2 Limiter ATT step

FS3	FS2	FS1	FS0	ALC2 Limiter Time				
				LTMP=00 (Default)	LTMP=01	LTMP=10	LTMP=11	
0	0	0	0	6/fs (136μs)	12/fs (272μs)	24/fs (544μs)	48/fs (1088μs)	Default
0	0	0	1	4/fs (125μs)	8/fs (250μs)	16/fs (500μs)	32/fs (1000μs)	
0	0	1	0	6/fs (125μs)	12/fs (250μs)	24/fs (500μs)	48/fs (1000μs)	
1	0	0	0	3/fs (136μs)	6/fs (272μs)	12/fs (544μs)	24/fs (1088μs)	
1	0	0	1	2/fs (125μs)	4/fs (250μs)	8/fs (500μs)	16/fs (1000μs)	
1	0	1	0	3/fs (125μs)	6/fs (250μs)	12/fs (500μs)	24/fs (1000μs)	
1	1	0	0	1.5/fs (136μs)	3/fs (272μs)	6/fs (544μs)	12/fs (1088μs)	
1	1	0	1	1/fs (125μs)	2/fs (250μs)	4/fs (500μs)	8/fs (1000μs)	
1	1	1	0	1.5/fs (125μs)	3/fs (250μs)	6/fs (500μs)	12/fs (1000μs)	
Others				N/A				

Table 25. ALC2 Limiter Operation Period

(2) ALC2 Recovery Operation

The ALC2 recovery operation waits for WTMP1-0 bits (Table 26) to be set after completing the ALC2 limiter operation. If the input signal does not exceed "ALC2 recovery waiting counter reset level" (LMTHP bit) during the wait time, the ALC2 recovery operation is done. The ALC2 value is automatically incremented by RGAINP bit (Table 27) up to the set reference level (REFP5-0 bits: Table 28). The ALC2 recovery operation is done at a period set by WTMP1-0 bits. When zero cross is detected at both channels during the wait period set by WTM1-0 bits, the ALC recovery operation waits until WTM1-0 period and the next recovery operation is done. The setting period of WTM1-0 bits should be the same as ZTM1-0 bits or longer time. When MOFF9 bit is "0", the volume value is incremented with soft transition. The soft transition time is set by PTS1-0 bits (Table 39). The WTMP1-0 bits should be set to the same period as PTS1-0 bits or longer. When MOFF9 bit is "1", the volume increase immediately.

During the ALC2 recovery operation, the ALC2 limiter operation starts immediately as soon as the ALC2 output level exceeds the ALC2 limiter detection level (LMTHP bit).

When
"ALC2 recovery waiting counter reset level ≤ ALC2 Output Signal Level < ALC2 limiter detection level" during the ALC2 recovery operation, the waiting timer of ALC2 recovery operation is reset. When
"ALC2 recovery waiting counter reset level > ALC2 Output Signal Level",
the waiting timer of ALC1 recovery operation starts.

FS3	FS2	FS1	FS0	ALC2 Recovery Time				
				WTMP=00 (Default)	WTMP=01	WTMP=10	WTMP=11	
0	0	0	0	768/fs (17.4ms)	1536/fs (34.8ms)	3072/fs (69.7ms)	24576/fs (557ms)	Default
0	0	0	1	512/fs (16.0ms)	1024/fs (32.0ms)	2048/fs (64.0ms)	16384/fs (512ms)	
0	0	1	0	768/fs (16.0ms)	1536/fs (32.0ms)	3072/fs (64.0ms)	24576/fs (512ms)	
1	0	0	0	384/fs (17.4ms)	768/fs (34.8ms)	1536/fs (69.7ms)	12288/fs (557ms)	
1	0	0	1	256/fs (16.0ms)	512/fs (32.0ms)	1024/fs (64.0ms)	8192/fs (512ms)	
1	0	1	0	384/fs (16.0ms)	768/fs (32.0ms)	1536/fs (64.0ms)	12288/fs (512ms)	
1	1	0	0	192/fs (17.4ms)	384/fs (34.8ms)	768/fs (69.7ms)	6144/fs (557ms)	
1	1	0	1	128/fs (16.0ms)	256/fs (32.0ms)	512/fs (64.0ms)	4096/fs (512ms)	
1	1	1	0	192/fs (16.0ms)	384/fs (32.0ms)	768/fs (64.0ms)	6144/fs (512ms)	
Others				N/A				

Table 26. ALC2 Recovery Operation Period

RGAINP	GAIN STEP		
0	1 step	0.5dB	Default
1	2 step	1.0dB	

Table 27. ALC2 Recovery Gain Step

REFP5-0	GAIN(dB)	Step	
3FH	+19.5	0.5dB	
3EH	+19.0		
3DH	+18.5		
3CH	+18.0		Default
:	:		
19H	+0.5		
18H	0.0		
17H	–0.5		
:	:		
02H	–11.0		
01H	–11.5		
00H	–12.0		

Table 28. Reference Level at ALC2 Recovery Operation

(3) Example for ALC2 Operation

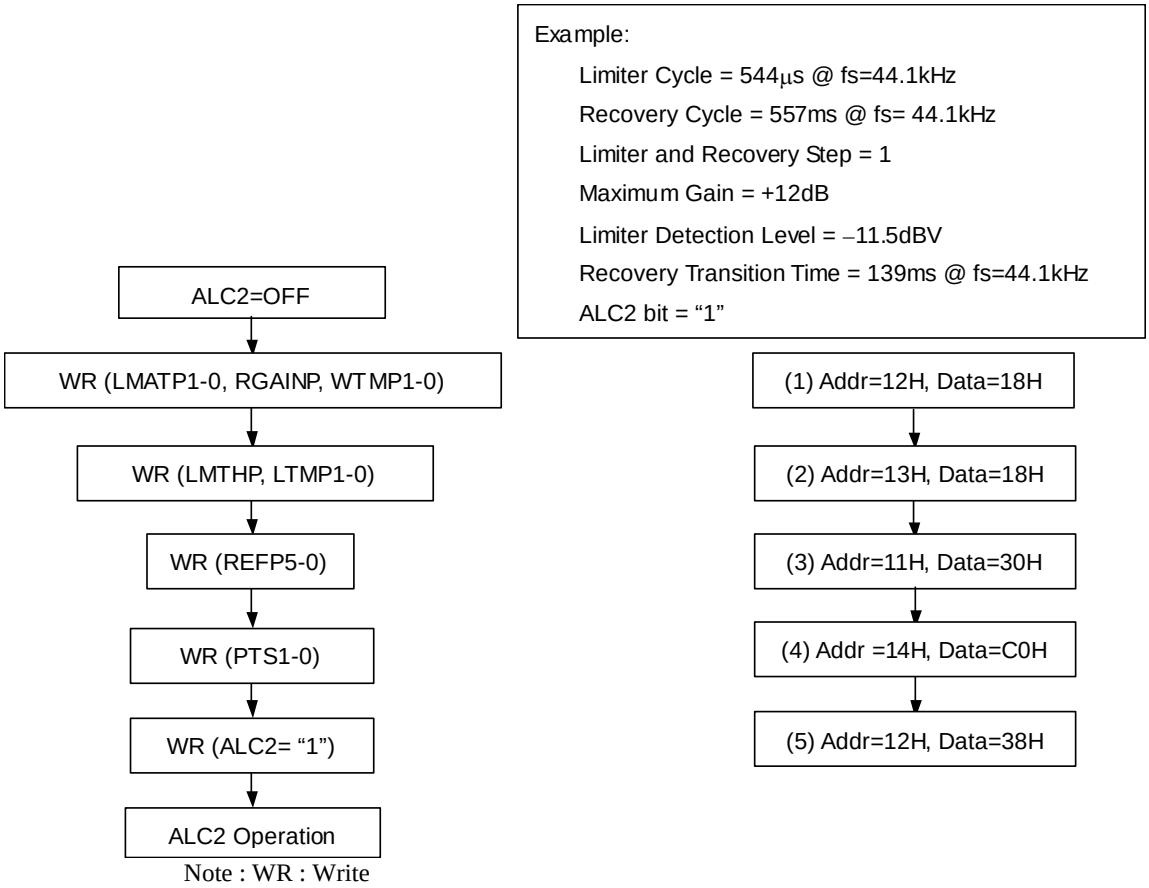
Table 29 shows the examples of the ALC2 setting. The ALC2 operation starts from 0dB.

Register Name	Comment	Data	fs		
			8kHz 16kHz 32kHz	11.025kHz 22.05kHz 44.1kHz	12kHz 24kHz 48kHz
LMTHP	Limiter detection Level	1	–11.5dBV	–11.5dBV	–11.5dBV
LTMP1-0	Maximum gain at recovery operation	10	500μs	544μs	500μs
WTMP1-0	Recovery waiting period	11	512ms	557ms	512ms
REFP7-0	Maximum gain at recovery operation	30H	+12dB	+12dB	+12dB
LMATP1-0	Limiter ATT Step	00	0.5dB	0.5dB	0.5dB
RGAINP	Recovery GAIN Step	0	0.5dB	0.5dB	0.5dB
PTS1-0	ALC2 recovery transition time	11	128ms	139ms	128ms
ALC2	ALC2 Enable bit	1	Enable	Enable	Enable

Table 29. Example for the ALC2 setting

The following registers should not be changed during the ALC2 operation. These bits should be changed after the ALC2 operation is finished by ALC2 bit is "0" or PMLO bit is "0".

- LMTHP, LTMP1-0, LMATP1-0, WTMP1-0, RGAINP, REFP5-0, PTS1-0



Note : WR : Write

Figure 18. Registers set-up sequence at ALC2 operation

■ Output Analog Volume (LOUT, ROUT pins)

When the LMUTE bit is "0", ATTS3-0 bits (0dB ~ –30dB, 2dB step, Table 30) control the LOUT/ROUT output level. Some pop noise occurs at the changing of output volume of LOUT/ROUT.

LMUTE	ATTS3-0	Attenuation	
0	FH	0dB	
	EH	–2dB	
	DH	–4dB	
	CH	–6dB	
	:	:	
	:	:	
	1H	–28dB	
	0H	–30dB	
1	x	MUTE	Default

Table 30. LOUT/ROUT Volume ATT (x: Don't care)

■ Stereo Line Output (LOUT, ROUT pins)

The common voltage is VCOM, and the load resistance is min. 10kΩ. Stereo Lineout is powered-up when PMLO bit is "1". The ON/OFF of each path is set by DACL, LINL, MINL, DACR, RINR and MINR bits. When ALC2 bit is "0" and ATTS3-0 bits is "FH"(0dB), the summation gain of each path is 0dB (typ).

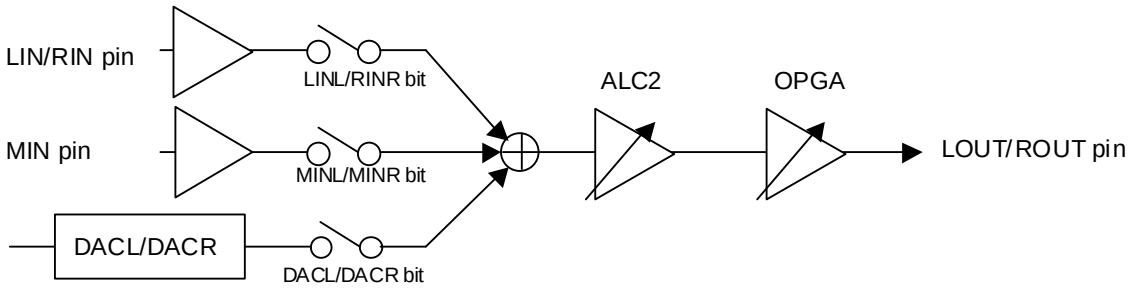


Figure 19. LOUT/ROUT Summation Circuit

(L+R)/2 signal of DAC is output from LOUT and ROUT pins when LOM bit is "1".

DACL	LOM bit	LOUT pin	
0	x	Path OFF	Default
1	0	L	
	1	(L+R)/2	

Table 31. Line Output Mode (Lch)

DACR	LOM bit	ROUT pin	
0	x	Path OFF	Default
1	0	R	
	1	(L+R)/2	

Table 32. Line Output Mode (Rch)

■ Headphone Output (HPL/HPR pins)

Power supply voltage for headphone amplifiers is applied from HVDD pin for the positive supply and the negative supply generated by the internal charge pump circuit. The headphone amplifier is single-ended outputs and centered on 0V (AVSS). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω. HPG bit set the output voltage (Table 33).

HPG bit	Output Voltage	Output Power	
0	1.5Vpp@0dBFS	17mW@16Ω	Default
1	2.0Vpp@−3dBFS	31mW@16Ω	

Table 33. Headphone Output Voltage / Power

The headphone output is enabled when HPMTN bit is "1" and muted when HPMTN bit is "0". The mute ON/OFF time are set by PTS1-0 bits (Table 39) when MOFF8 bit is "0". When MOFF8 bit is "1", the ON/OFF is done immediately.

When PMHPL and PMHPR bits are "0", the headphone amplifiers are powered-down completely. At that time, the HPL and HPR pins are AVSS voltage. The power-up/down time are set by PUT1-0 bits (Table 38) when MOFF0 bit is "0". When MOFF0 bit is "1", the power up/down is done immediately.

PMHPL/R bits	HPMTN bit	HP-Amp	
0	x	Power-down	Default
1	0	Power-up & Mute	
	1	Power-up & Output	

Table 34. Headphone output states

The ON/OFF of each path is set by DACHL, LINHL, MINHL, DACHR, RINHR and MINHR bits. The summation gain of each path is 0dB (typ) at HPG bit = "0" and +5.5dB (typ) at HPG bit = "1".

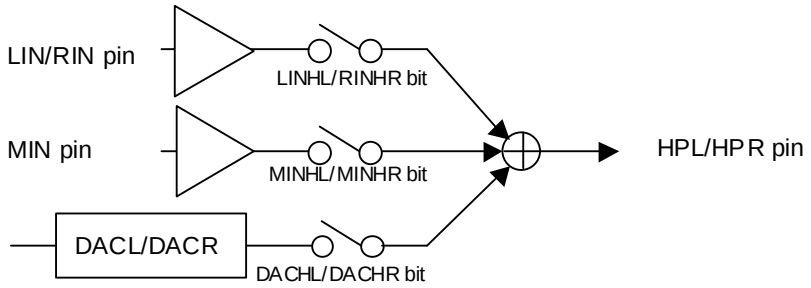


Figure 20. The Summation Circuit of Headphone Output

(L+R)/2 signal of DAC is output from HPL and HPR pins when HPM bit is "1".

DACHL	HPM bit	HPL pin	
0	x	Path OFF	Default
1	0	L	
	1	(L+R)/2	

Table 35. Headphone Output Mode (Lch)

DACHR	HPM bit	HPR pin	
0	x	Path OFF	Default
1	0	R	
	1	(L+R)/2	

Table 36. Headphone Output Mode (Rch)

■ Transition Time

The power-up/down time of HP-Amp at the change of PMHPL/R bits is set by PUT1-0 bits (Table 38).

The mute ON/OFF timing of HP-Amp, the ON/OFF timing of output path for HPL/HPR and LOUT/ROUT, and the gain changing at ALC2 recovery operation are changed by the soft transition respectively. The transition time is set by PTS1-0 bits (Table 39). The register value of same address must be changed by an interval more than transition time.

The Enable/Disable for the soft transition is set by MOFF0, MOFF8 and MOFF9 bits (Table 37). The soft transition is disabled while these bits are "1", and ON/OFF is done immediately.

As shown in Table 37, if the soft transition is enabled, the register value of same address must be changed by an interval more than transition time. The write operation is ignored if the same values are written as the previous write operation.

	Address	Register Name	Enable/Disable
PUT1-0 bits	00H	PMHPL, PMHPR bits	MOFF0 bit
PTS1-0 bits	08H	DACHL, LINHL, MINHL, DACHR, RINHR, MINHR, HPMTN bits	MOFF8 bit
	09H	DACL, LINL, RINR, MINL, DACR, MINR bits	MOFF9 bit

Table 37. Registers with Transition Time

FS3	FS2	FS1	FS0	Power-up/down Time				
				PUT=00 (Default)	PUT=01	PUT=10	PUT=11	
0	0	0	0	770/fs (17.5ms)	1538/fs (34.9ms)	3074/fs (69.7ms)	6146/fs (139ms)	Default
0	0	0	1	514/fs (16.1ms)	1026/fs (32.1ms)	2050/fs (64.1ms)	4098/fs (128ms)	
0	0	1	0	770/fs (16.1ms)	1538/fs (32.1ms)	3074/fs (64.1ms)	6146/fs (128ms)	
1	0	0	0	386/fs (17.5ms)	770/fs (34.9ms)	1538/fs (69.8ms)	3074/fs (139ms)	
1	0	0	1	258/fs (16.1ms)	514/fs (32.1ms)	1026/fs (64.1ms)	2050/fs (128ms)	
1	0	1	0	386/fs (16.1ms)	770/fs (32.1ms)	1538/fs (64.1ms)	3074/fs (128ms)	
1	1	0	0	194/fs (17.6ms)	386/fs (35.0ms)	770/fs (69.8ms)	1538/fs (140ms)	
1	1	0	1	130/fs (16.3ms)	258/fs (32.3ms)	514/fs (64.3ms)	1026/fs (128ms)	
1	1	1	0	194/fs (16.2ms)	386/fs (32.2ms)	770/fs (64.2ms)	1538/fs (128ms)	
Others				N/A				

Table 38. HP-Amp Power-up/down Time

FS3	FS2	FS1	FS0	Transition Time				
				PTS=00 (Default)	PTS=01	PTS=10	PTS=11	
0	0	0	0	768/fs (17.4ms)	1536/fs (34.8ms)	3072/fs (69.7ms)	6144/fs (139ms)	Default
0	0	0	1	512/fs (16.0ms)	1024/fs (32.0ms)	2048/fs (64.0ms)	4096/fs (128ms)	
0	0	1	0	768/fs (16.0ms)	1536/fs (32.0ms)	3072/fs (64.0ms)	6144/fs (128ms)	
1	0	0	0	384/fs (17.4ms)	768/fs (34.8ms)	1536/fs (69.7ms)	3072/fs (139ms)	
1	0	0	1	256/fs (16.0ms)	512/fs (32.0ms)	1024/fs (64.0ms)	2048/fs (128ms)	
1	0	1	0	384/fs (16.0ms)	768/fs (32.0ms)	1536/fs (64.0ms)	3072/fs (128ms)	
1	1	0	0	192/fs (17.4ms)	384/fs (34.8ms)	768/fs (69.7ms)	1536/fs (139ms)	
1	1	0	1	128/fs (16.0ms)	256/fs (32.0ms)	512/fs (64.0ms)	1024/fs (128ms)	
1	1	1	0	192/fs (16.0ms)	384/fs (32.0ms)	768/fs (64.0ms)	1536/fs (128ms)	
Others				N/A				

Table 39. HP-Amp Mute ON/OFF, Path ON/OFF & ALC2 Recovery Transition Time

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage from HVDD voltage. The generated voltage is used to headphone amplifier. When PMCP bit is set to "1", the charge pump circuit is powered-up. All clocks (MCLK, BICK and LRCK) should be supplied at this time. The power-up time of charge pump circuit depends on FS3-0 bits (Table 40).

FS3	FS2	FS1	FS0	fs	Power up time of Charge Pump Circuit	
0	0	0	0	44.1kHz	512/fs = 11.6ms	Default
0	0	0	1	32kHz	256/fs = 8.0ms	
0	0	1	0	48kHz	512/fs = 10.7ms	
1	0	0	0	22.05kHz	256/fs = 11.6ms	
1	0	0	1	16kHz	128/fs = 8.0ms	
1	0	1	0	24kHz	256/fs = 10.7ms	
1	1	0	0	11.025kHz	128/fs = 11.6ms	
1	1	0	1	8kHz	64/fs = 8.0ms	
1	1	1	0	12kHz	128/fs = 10.7ms	
Others				N/A	N/A	

Table 40. Power up time of Charge Pump Circuit

■ System Reset

The AK4665A should be reset once by bringing PDN pin "L" upon power-up. After exiting reset, all blocks (VCOM, ADC, DAC, HPL, HPR, Lineout and charge pump circuit) switch to the power-down state. The contents of the control register are maintained until the reset is done.

ADC exits reset and power down state after PMADC bit is changed to "1", and then ADC is powered-up and the internal timing starts clocking by LRCK edge. ADC is in power-down mode until MCLK and LRCK are input. DAC also exits reset and power down state when MCLK and LRCK are input after PMDAC bit is changed to "1".

■ Power-Up/Down Sequence

1) ADC (MICIN)

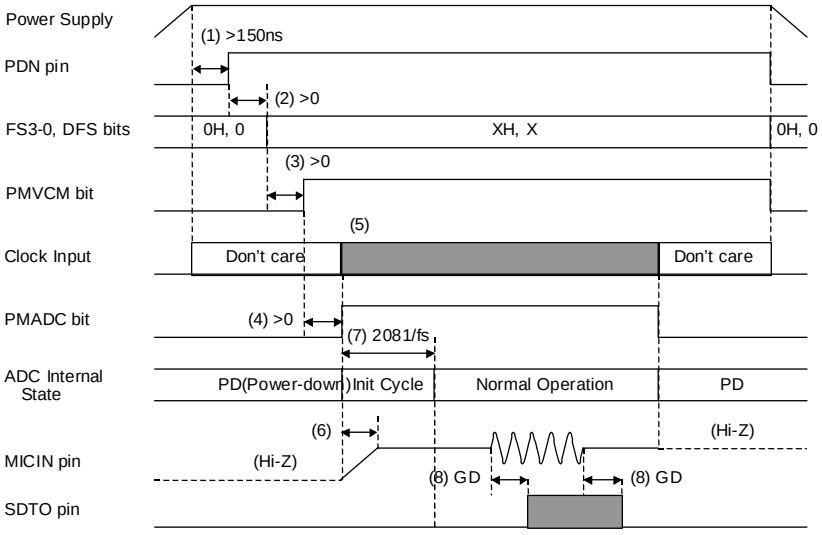


Figure 21. Power-up/down Sequence of ADC

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) FS3-0 and DFS bits should be set after PDN pin goes to "H".
(3) PMVCM bit should be changed to "1" after FS3-0 and DFS bits are set.
(4) PMADC bit should be changed to "1" after PMVCM bit is changed to "1".
(5) External clocks (MCLK, BICK and LRCK) are needed to operate ADC.
(6) When PMADC bit is changed to "1", MICIN pin is biased to VCOM voltage. Rising time constant is determined by input capacitor for AC coupling and input resistance. In case of 0.22µF input capacitor, time constant is
τ = 0.22µF x 30kΩ = 6.6ms (typ) at MGAIN1 bit = "1"
τ = 0.22µF x 60kΩ = 13.2ms (typ) at MGAIN1 bit = "0"
(7) The analog part of ADC is initialized during 2081/fs(=47ms@fs=44.1kHz) after exiting the power-down state. SDTO is "L" at that time.
(8) Digital output corresponding to analog input has the group delay (GD) of 17.0/fs(=385µs@fs=44.1kHz).

2) ADC (Line In: in case of common jack with headphone)

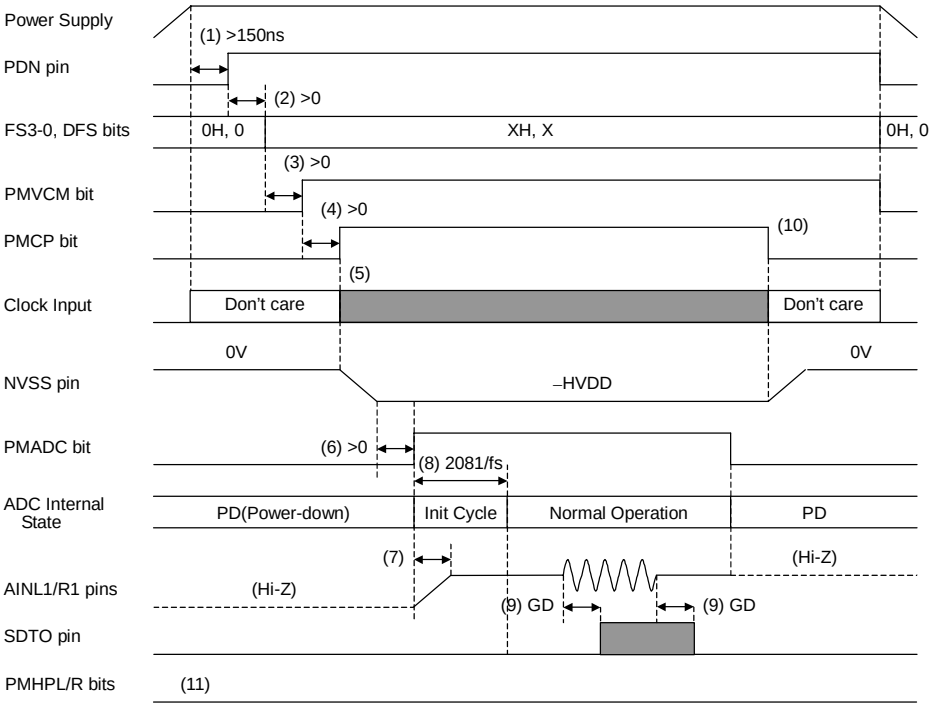


Figure 22. Power-up/down Sequence of ADC

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) FS3-0 and DFS bits should be set after PDN pin goes to "H".
(3) PMVCM bit should be changed to "1" after FS3-0 and DFS bits are set.
(4) PMCP bit should be changed to "1" after PMVCM bit is changed to "1". The charge pump circuit is powered-up and NVSS pin goes to –HVDD voltage according to the setting of FS3-0 and DFS bits.
(5) External clocks (MCLK, BICK and LRCK) are needed to operate the charge pump circuit and ADC.
(6) PMADC bit should be changed to "1" after NVSS pin goes to –HVDD voltage.
(7) When PMADC bit is changed to "1", AINL1/R1 pins are biased to VCOM voltage. Rising time constant is determined by input capacitor for AC coupling and input resistance. In case of 1μF input capacitor, time constant is

$$\tau = 1\mu F \times 60k\Omega = 60ms \text{ (typ)}$$

(8) The analog part of ADC is initialized during 2081/fs (=47ms@fs=44.1kHz) after exiting the power-down state. SDTO is "L" at that time.
(9) Digital output corresponding to analog input has the group delay (GD) of 17/fs (=385μs@fs=44.1kHz).
(10) When PMCP bit is changed to "0", the charge pump circuit is powered-down and NVSS pin becomes 0V. Falling time constant is determined by capacitor and internal resistance (typ 17.5kΩ). In case of 2.2μF capacitor, time constant is

$$\tau = 2.2\mu F \times 17.5k\Omega = 38.5ms \text{ (typ)}$$

(11) When PMHPL/R bits = "0", HPL/R pins are connected to AVSS with internal pull-down resistance (typ 100kΩ).

3) DAC → HP-Amp

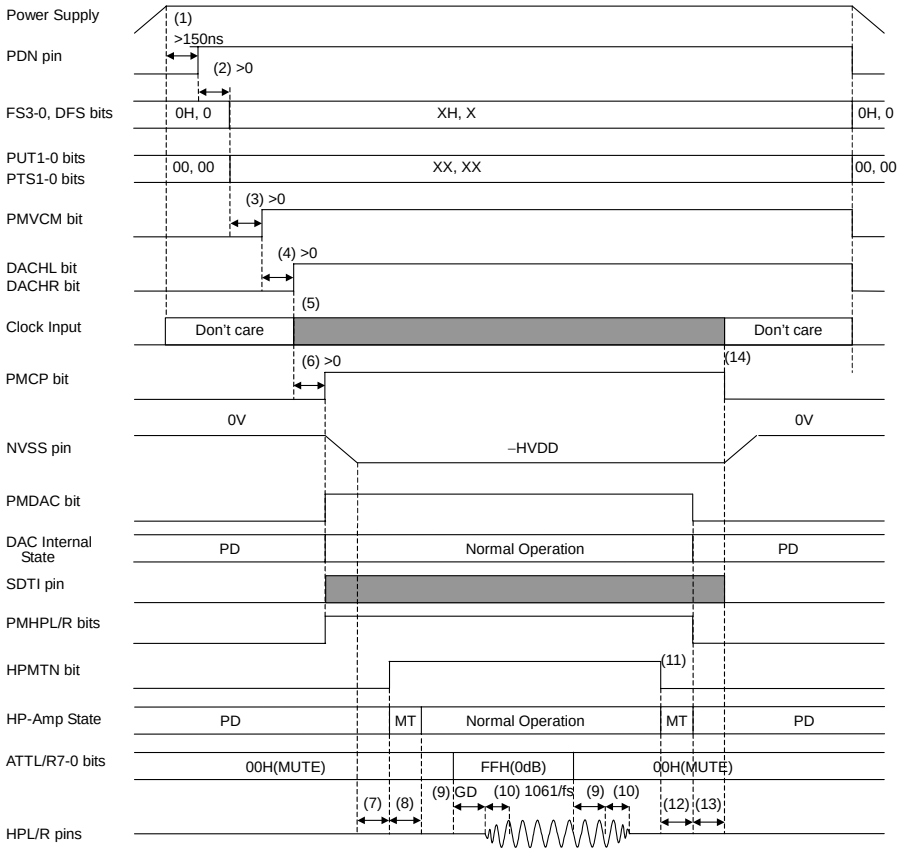


Figure 23. Power-up/down Sequence of DAC and HP-Amp

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) FS3-0, DFS, PUT1-0 and PTS1-0 bits should be set after PDN pin goes to "H".
(3) PMVCM bit should be changed to "1" after FS3-0, DFS, PUT1-0 and PTS1-0 bits are set.
(4) DACHL and DACHR bits should be changed to "1" after PMVCM bit is changed to "1". Each path is switched-on during the transition time set by FS3-0 and PTS1-0 bits.
(5) External clocks (MCLK, BICK and LRCK) are needed to operate the charge pump circuit, HP-Amp or DAC. External clocks are also needed for each path (DACHL, LINHL, MINHL, DACHR, RINHR, MINHR and HPMTN bits) setting.
(6) PMCP, PMDAC, PMHPL and PMHPR bits should be changed to "1" after DACHL and DACHR bits are changed to "1". When PMCP bit is changed to "1", the charge pump circuit is powered-up and NVSS pin goes to –HVDD voltage according to the setting of FS3-0 and DFS bits
(7) After power-up of the charge pump circuit, HP-Amp is powered-up. Rising time of HP-Amp is determined by FS3-0, DFS and PUT1-0 bits.
(8) HPMTN bit should be changed to "1" to release the mute after HP-Amp is powered-up. The transition time of mute release is determined by FS3-0,DFS and PTS1-0 bits.
(9) Digital output corresponding to analog input has the group delay (GD) of 17.5/fs (=397μs@fs=44.1kHz).
(10) The transition time for digital volume is set by ATS bit. The initial value is 1061/fs (=24ms@fs=44.1kHz).
(11) HPMTN bit should be changed to "0" to mute HP-Amp.
(12) After the transition time for mute, PMDAC, PMHPL and PMHPR bits should be changed to "0" to power-down of DAC and HP-Amp.
(13) After power-down of the HP-Amp, PMCP bit should be changed to "0" to power-down the charge pump circuit. Falling time constant is determined by external capacitor connected with NVSS pin and internal resistance (typ 17.5kΩ). In case of 2.2μF capacitor, time constant is

$$\tau = 2.2\mu F \times 17.5k\Omega = 38.5ms \text{ (typ)}$$

(14) Clocks should be stopped after PMCP bit is changed to "0".

4) DAC → Line Out

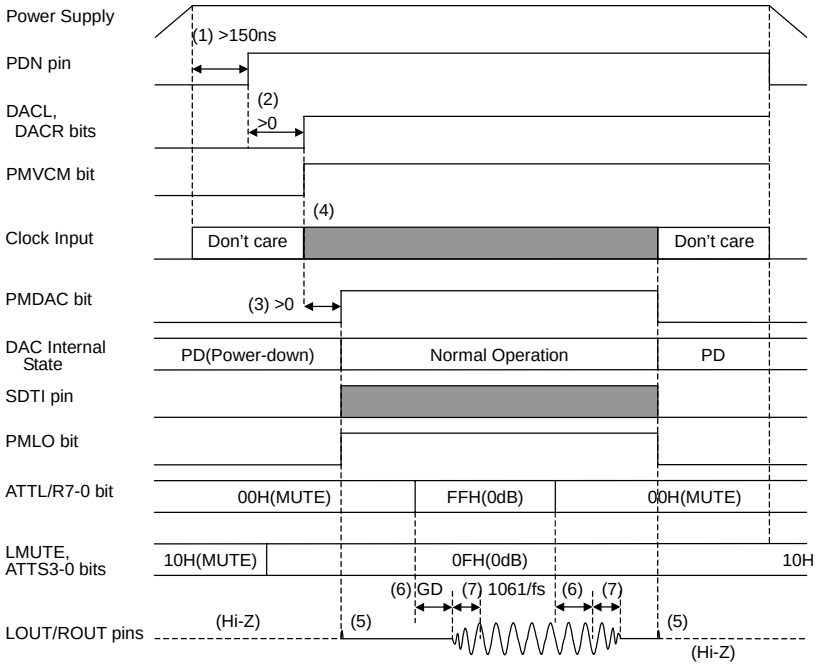


Figure 24. Power-up/down Sequence of DAC and Line Out

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) DACL and DACR bits should be changed to "1" after PDN pin goes to "H". Each path is switched-on during the transition time set by FS3-0 and PTS1-0 bits.
(3) PMDAC and PMLO bits should be changed to "1" after DACL and DACR pins are changed to "1".
(4) External clocks (MCLK, BICK and LRCK) are needed to operate DAC. External clocks are also needed for each path (DACL, LINL, MINL, DACR, RINR and MINR bits) setting.
(5) When PMLO bit is changed to "1", pop noise is output from LOUT/ROUT pins.
(6) Digital output corresponding to analog input has the group delay (GD) of 17.5/fs (=397μs@fs=44.1kHz).
(7) The transition time for digital volume is set by ATS bit. The initial value is 1061/fs (=24ms@fs=44.1kHz).

5) LIN/RIN/MIN → HP-Amp

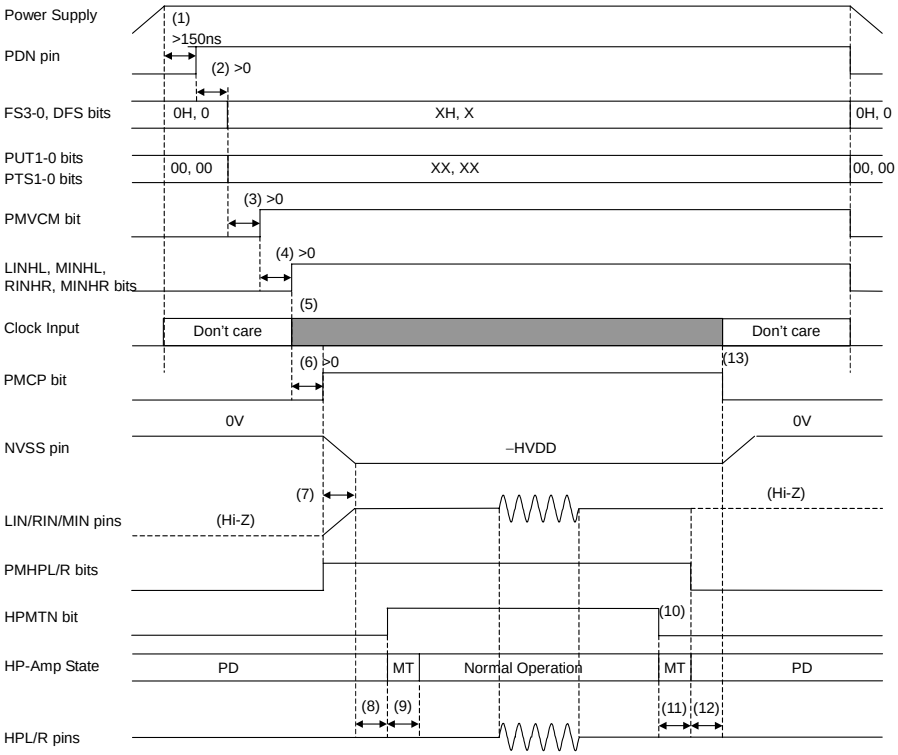


Figure 25. Power-up/down Sequence of LIN/RIN/MIN and HP-Amp

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) FS3-0, DFS, PUT1-0 and PTS1-0 bits should be set after PDN pin goes to "H".
(3) PMVCM bit should be changed to "1" after FS3-0, DFS, PUT1-0 and PTS1-0 bits are set.
(4) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1". Each path is switched-on during the transition time set by FS3-0 and PTS1-0 bits.
(5) External clocks (MCLK, BICK and LRCK) are needed to operate the charge pump circuit and HP-Amp. External clocks are also needed for each path (DACHL, LINHL, MINHL, DACHR, RINHR, MINHR and HPMTN bits) setting.
(6) PMCP, PMHPL and PMHPR bits should be changed to "1" after LINHL, MINHL, RINHR and MINHR bits are changed to "1". When PMCP bit is changed to "1", the charge pump circuit is powered-up and NVSS pin goes to –HVDD voltage according to the setting of FS3-0 and DFS bits.
(7) When PMHPL, PMHPR or PMLO bit is changed to "1", LIN, RIN and MIN pins are biased to VCOM voltage. Rising time constant is determined by capacitor for AC coupling and input resistance 200kΩ (typ). In case of 0.047μF input capacitor, time constant is

$$\tau = 0.047\mu F \times 200k\Omega = 9.4ms \text{ (typ)}$$

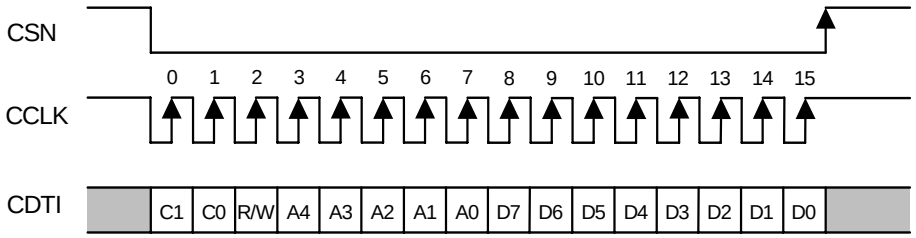
(8) After power-up the charge pump circuit, HP-Amp is powered-up. Rising time of HP-Amp is determined by FS3-0,DFS and PUT1-0 bits.
(9) HPMTN bit should be changed to "1" to release the mute after HP-Amp is powered-up. The transition time of mute release is determined by FS3-0,DFS and PTS1-0 bits.
(10) HPMTN bit should be changed to "0" to mute HP-Amp.
(11) After the transition time for mute, PMHPL and PMHPR bits should be changed to "0" to power-down of HP-Amp.
(12) After power-down of the HP-Amp, PMCP bit should be changed to "0" to power-down of the charge pump circuit. Falling time constant is determined by external capacitor connected with NVSS pin and internal resistance (typ 17.5kΩ). In case of 2.2μF capacitor, time constant is

$$\tau = 2.2\mu F \times 17.5k\Omega = 38.5ms \text{ (typ)}$$

(13) Clocks should be stopped after PMCP bit is changed to "0".

■ Serial Control Interface

Internal registers may be written via the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of Chip address (2bits, Fixed to “10”), Read/Write (1bit, Fixed to “1”, Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Data is clocked in on the rising edge of CCLK. For write operations, data is latched on the rising edge of 16th clock of CCLK. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN= “L”.



C1-C0: Chip Address (Fixed to “10”)
R/W: Read/Write (Fixed to “1”: Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 26. Control Interface

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	PMCP	0	PMLO	PMHPR	PMHPL	PMDAC	PMADC	PMVCM
01H	Input Select	MOFF0	0	PMMP	ADM	0	INR1	INL2	INL1
02H	Timer Select	MGAIN1	MGAIN0	ZTM1	ZTM0	WTM1	WTM0	0	0
03H	ALC1 Mode Control 1	RGAIN1	LMTH1	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
04H	ALC1 Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
05H	IVOL Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
06H	Mode Control 1	0	0	0	ATS	HPM	DIF1	DIF0	DFS
07H	DAC Control	0	0	SMUTE	DATTC	BST1	BST0	DEM1	DEM0
08H	HP Output Select	MOFF8	HPMTN	MINHR	RINHR	DACHR	MINHL	LINHL	DACHL
09H	Line Output Select	MOFF9	LOM	MINR	DACR	MINL	RINR	LINL	DACL
0AH	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0BH	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
0CH	Lineout ATT	0	0	0	LMUTE	ATTS3	ATTS2	ATTS1	ATTS0
0DH	Test 1	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
0EH	Test 2	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
0FH	Test 3	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
10H	Test 4	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
11H	ALC2 Mode Control 1	0	0	REFP5	REFP4	REFP3	REFP2	REFP1	REFP0
12H	ALC2 Mode Control 2	HPG	LING	ALC2	WTMP1	WTMP0	LMATP1	LMATP0	RGAINP
13H	Mode Control 2	0	0	0	LMTHP	LTMP1	LTMP0	SDOD	LOOP
14H	Mode Control 3	PTS1	PTS0	PUT1	PUT0	FS3	FS2	FS1	FS0

All registers inhibit writing at PDN pin = "L".

Note: Unused bits must contain a "0" value.
Note: For addresses from 0DH to 10H and from 15H to 1FH, "0"data must be written.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	PMCP	0	PMLO	PMHPR	PMHPL	PMDAC	PMADC	PMVCM
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (Default)
1: Power ON

PMADC: Power Management for MIC-Amp and ADC Blocks
0: Power OFF (Default)
1: Power ON
MCLK should be present when PMADC bit is “1”.

PMDAC: Power Management for DAC Block
0: Power OFF (Default)
1: Power ON
When PMDAC bit is changed from “0” to “1”, DAC is powered-up to the current register values (ATT value, sampling rate, etc).

PMHPL: Power Management for Lch of Headphone Amp
0: Power OFF (Default). HPL pin becomes AVSS (0V).
1: Power ON

PMHPR: Power Management for Rch of Headphone Amp
0: Power OFF (Default). HPR pin becomes AVSS (0V).
1: Power ON

PMLO: Power Management for Stereo Lineout
0: Power OFF (Default). LOUT and ROUT pins become Hi-Z.
1: Power ON

PMCP: Power Management for Charge Pump Circuit
0: Power OFF (Default)
1: Power ON

All blocks can be powered-down by setting PDN pin to “L” regardless of register values setting. In this case, all control register values are initialized.

When PMVCM, PMADC, PMDAC, PMHPL, PMHPR, PMLO and PMCP bits are “0”, all blocks are powered-down. The register values remain unchanged. Power supply current is 100μA(typ) in this case. For fully shut down (typ. 1μA), PDN pin should be “L”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Input Select	MOFF0	0	PMMP	ADM	0	INR1	INL2	INL1
Default		0	0	0	0	0	1	0	1

INL1: Select ON/OFF of Lch Line input
0: OFF
1: ON (Default)

INL2: Select ON/OFF of Mono Mic input
0: OFF (Default)
1: ON

INR1: Select ON/OFF of Rch Line input
0: OFF
1: ON (Default)

ADM: Mono Recording Mode (Table 8)
0: Stereo (Default)
1: MONO
When ADM bit is "1", ADC Lch data is output on both Lch and Rch of SDTO.

PMMP: Power Management for MPWR pin
0: Power down: Hi-Z (Default)
1: Power up

MOFF0: Soft transition for changing PMHPL, PMHPR bits
0: Enable (Default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Timer Select	MGAIN1	MGAIN0	ZTM1	ZTM0	WTM1	WTM0	0	0
Default		0	0	0	0	0	0	0	0

WTM1-0: ALC1 Recovery Waiting Period (Table 12)

ZTM1-0: ALC1 Zero Crossing Timeout Period (Table 11)

MGAIN1-0: MIC-Amp Gain (Table 5)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	ALC1 Mode Control 1	RGAIN1	LMTH1	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level (Table 9)

RGAIN1-0: ALC1 Recovery Gain Step (Table 13)

LMAT1-0: ALC1 Limiter ATT Step (Table 10)

ZELMN: Zero Crossing Detection Enable at ALC1 Limiter Operation
0: Enable (Default)
1: Disable

ALC1: ALC1 Enable
0: ALC1 Disable (Default)
1: ALC1 Enable
ALC1 is enabled at ALC1 bit is "1".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	ALC1 Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC1 Recovery Operation (Table 14)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	IVOL Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
Default		1	0	0	1	0	0	0	1

IVOL7-0: Input Digital Volume (Table 16)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control	0	0	0	ATS	HPM	DIF1	DIF0	DFS
Default		0	0	0	0	0	1	0	0

DFS: Sampling Speed Mode (Table 1)

DIF1-0: Audio Interface Format (Table 4)
Default: "10" (Mode 2)

HPM: Mono Output Select of Headphone (Table 35,Table 36)

ATS: Digital attenuator transition time setting (Table 20)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC Control	0	0	SMUTE	DATTC	BST1	BST0	DEM1	DEM0
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select (Table 21)

BST1-0: Bass Boost Function Select (Table 22)

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent (Default)
1: Dependent
When DATTC bit is "1", ATTL7-0 bits control both Lch and Rch attenuation level, while register values of ATTL7-0 bits are not written to ATTR7-0 bits. When DATTC bit is "0", ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level.

SMUTE: Soft Mute Control
0: Normal operation (Default)
1: DAC outputs soft-muted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Output Select 0	MOFF8	HPMTN	MINHR	RINHR	DACHR	MINHL	LINHL	DACHL
Default		0	0	0	0	0	0	0	0

DACHL: DAC Lch output signal is added to Lch of headphone amp.
0: OFF (Default)
1: ON

LINHL: Input signal to LIN pin is added to Lch of headphone amp.
0: OFF (Default)
1: ON

MINHL: Input signal to MIN pin is added to Lch of headphone amp.
0: OFF (Default)
1: ON

DACHR: DAC Rch output signal is added to Rch of headphone amp.
0: OFF (Default)
1: ON

RINHR: Input signal to RIN pin is added to Rch of headphone amp.
0: OFF (Default)
1: ON

MINHR: Input signal to MIN pin is added to Rch of headphone amp.
0: OFF (Default)
1: ON

HPMTN: Mute of headphone amp.
0: Mute (Default)
1: Normal operation.

MOFF8: Soft transition for changing of DACHL, LINHL, MINHL, DACHR, RINHR, MINHR and HPMTN bits
0: Enable (Default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Output Select 1	MOFF9	LOM	MINR	DACR	MINL	RINR	LINL	DACL
Default		0	0	0	0	0	0	0	0

DACL: DAC Lch output signal is added to buffer amp of LOUT.
0: OFF (Default)
1: ON

LINL: Input signal to LIN pin is added to buffer amp of LOUT.
0: OFF (Default)
1: ON

RINR: Input signal to RIN pin is added to buffer amp of ROUT.
0: OFF (Default)
1: ON

MINL: Input signal to MIN pin is added to buffer amp of LOUT.
0: OFF (Default)
1: ON

DACR: DAC Rch output signal is added to buffer amp of ROUT.
0: OFF (Default)
1: ON

MINR: Input signal to MIN pin is added to buffer amp of ROUT.
0: OFF (Default)
1: ON

LOM: Lineout MONO output (Table 31,Table 32)

MOFF9: Soft transition for changing of DACL, LINL, RINR, MINL, DACR and MINR bits
0: Enable (Default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0BH	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
Default		0	0	0	0	0	0	0	0

ATTL7-0: Setting of the attenuation value of output signal from DACL (Table 19)
ATTR7-0: Setting of the attenuation value of output signal from DACR (Table 19)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Lineout ATT	0	0	0	LMUTE	ATTS3	ATTS2	ATTS1	ATTS0
Default		0	0	0	1	0	0	0	0

ATTS3-0: Analog volume control for LOUT/ROUT (Table 30)

LMUTE: Mute control for LOUT/ROUT
0: Normal operation. ATTS3-0 bits control attenuation value.
1: Mute. ATTS3-0 bits are ignored. (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Test 1	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
0EH	Test 2	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
0FH	Test 3	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
10H	Test 4	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
Default		0	0	0	0	0	0	0	0

TEST7-0: Test bits, “0”data must be written.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	ALC2 Mode Control 1	0	0	REFP5	REFP4	REFP3	REFP2	REFP1	REFP0
Default		0	0	1	1	1	1	0	0

REFP7-0: Reference Value at ALC2 Recovery Operation (Table 28)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	ALC2 Mode Control 2	HPG	LING	ALC2	WTMP1	WTMP0	LMATP1	LMATP0	RGAINP
Default		0	0	0	0	0	0	0	0

RGAINP: ALC2 Recovery Gain Step (Table 27)

LMATP1-0: ALC2 Limiter ATT Step (Table 24)

WTMP1-0: ALC2 Recovery Operation period (Table 26)

ALC2: ALC2 Enable
0: ALC2 Disable (Default)
1: ALC2 Enable

LING: LIN/RIN → HPL/HPR Path Gain
0: 0dB (Default)
1: –12dB

HPG: HP-Amp Output Gain
0: 0dB (Default)
1: +5.5dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Mode Control 2	0	0	0	LMTHP	LTMP1	LTMP0	SDOD	LOOP
Default		0	0	0	0	0	0	0	0

LOOP: Internal Loopback (Table 18)
0: OFF (Default)
1: ON

SDOD: SDTO Output Disable (Table 17)
0: Enable (Default)
1: Disable

LTMP1-0: ALC2 Limiter Operation Period (Table 25)

LMTHP: ALC2 Limiter Detection Level (Table 23)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	Mode Control 3	PTS1	PTS0	PUT1	PUT0	FS3	FS2	FS1	FS0
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Setting (Table 1)

PUT1-0: HP-Amp Power-up/down Time (Table 38)

PTS1-0: HP-Amp Mute ON/OFF, Path ON/OFF and ALC2 Recovery Transition Time (Table 39)

SYSTEM DESIGN

Figure 27 shows the system connection diagram. An evaluation board [AKD4665A] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

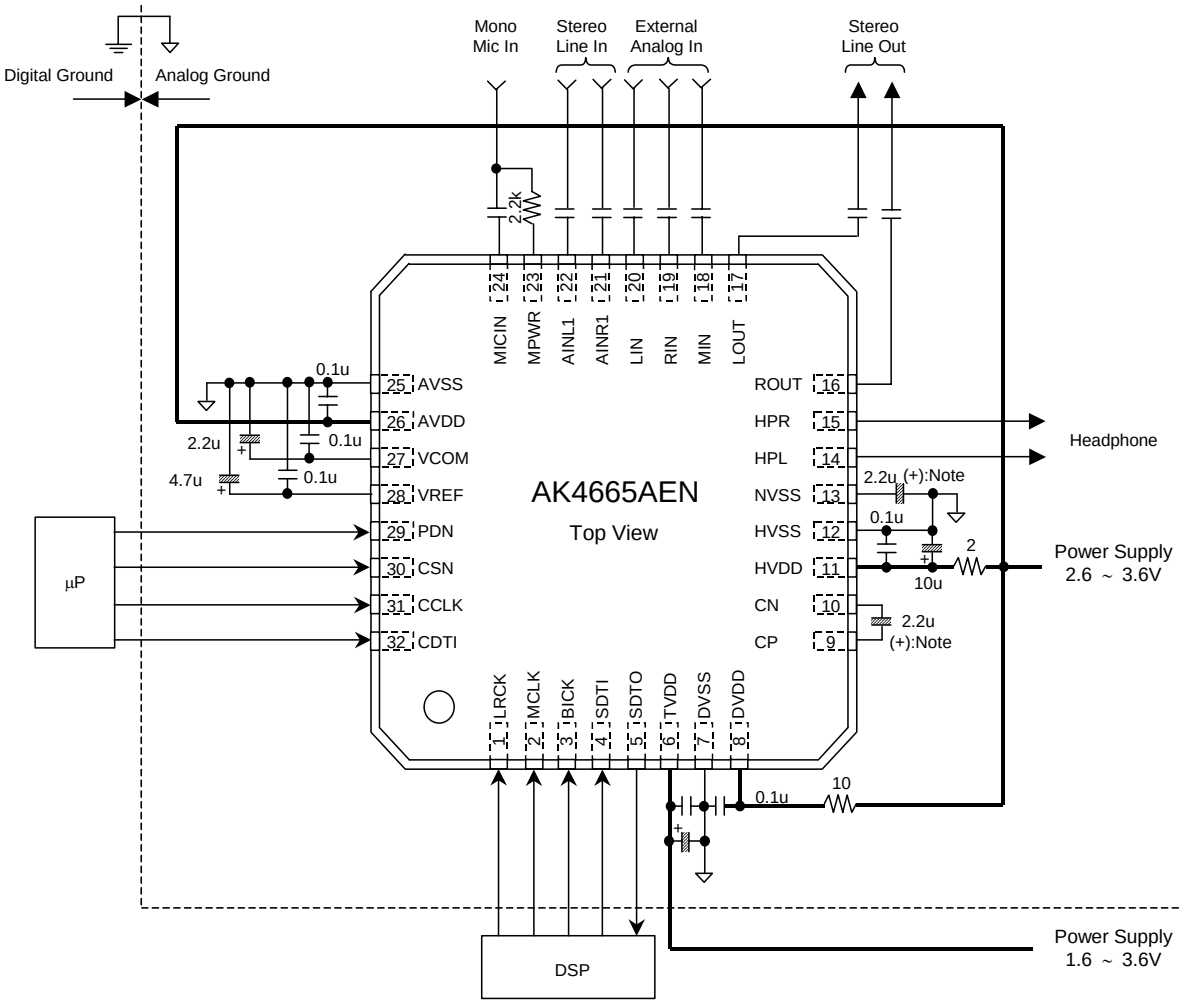


Figure 27. Typical Connection Diagram

Note:

- **A 2Ω resistor must be added in series between HVDD pin and power supply line in order to limit the current.**
- These capacitors at CP/CN pins and HVSS/NVSS pins require low ESR (Equivalent Series Resistance) over all temperature range. When these capacitors are not bipolar, the positive side should be connected to CP pin and HVSS respectively.
- AVSS, DVSS and HVSS of the AK4665A should be distributed separately from the ground of external controllers.
- All digital input should not be left floating.

1. Grounding and Power Supply Decoupling

The AK4665A requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the analog power supply in the system and DVDD&TVDD is supplied from AVDD via a 10Ω resistor. Alternatively if AVDD, DVDD, TVDD and HVDD are supplied separately, the power up sequence is not critical. AVSS, DVSS and HVSS must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4665A as possible, with the small value ceramic capacitors being the nearest.

2. Internal Voltage Reference

Internal voltage reference is output on the VREF pin (typ. 2.1V). An electrolytic capacitor 4.7μF in parallel with a 0.1μF ceramic capacitor is attached between VREF and AVSS to eliminate the effects of high frequency noise. VCOM is 1.2V(typ) and is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor should be connected between VCOM and AVSS to eliminate the effects of high frequency noise. A ceramic capacitor should be connected to VCOM pin and located as close as possible to the AK4665A. No load current may be drawn from VREF and VCOM pins. All signals, especially clocks, should be kept away from the VCOM and VREF pins in order to avoid unwanted coupling into the AK4665A.

3. Analog Inputs

The analog inputs are single-ended and the input resistance 60kΩ (typ) for AINL1/AINR1 pins and 60kΩ (typ)@0dB/–6dB or 30kΩ (typ)@+6dB/+30dB for MICIN pin. The input signal range is 1.5Vpp (typ) centered on VCOM voltage. Usually, the input signal cuts DC with a capacitor. The cut-off frequency is fc=(1/2πRC). The AK4665A can accept input voltages from AVSS to AVDD. The ADC output data format is 2's complement. The ADC's DC offset is removed by the internal HPF (fc=3.4Hz@fs=44.1kHz).

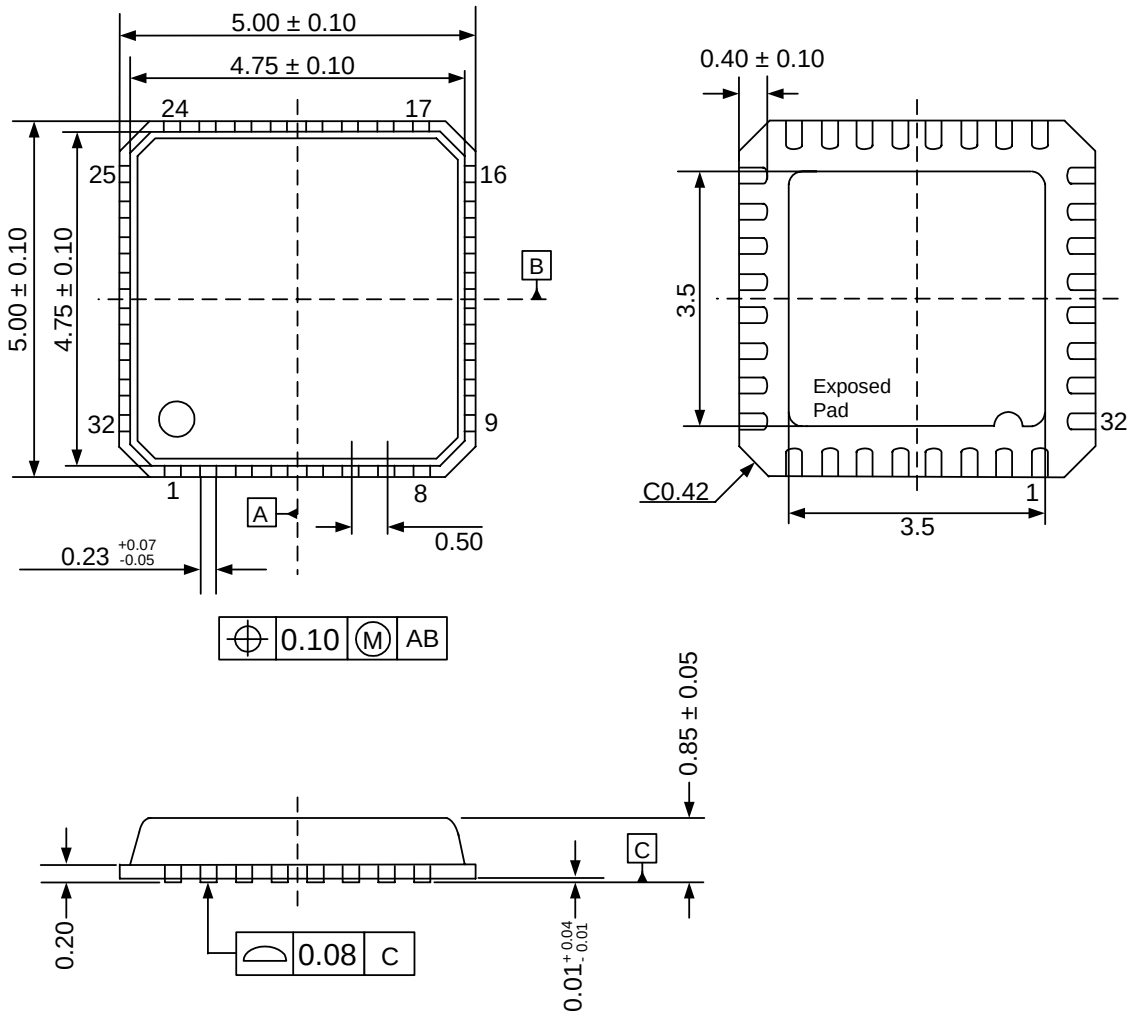
4. Analog Outputs

The analog outputs are single-ended outputs. The output signal range of lineout is 1.5Vpp(typ) centered on the VCOM voltage. The output signal range of headphone is 1.5Vpp(typ)@HPG bit = "0" or 2.83Vpp(typ)@HPG bit = "1" centered on AVSS voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFH(@20bit) and negative full scale for 80000H(@20bit). The ideal output is VCOM voltage (lineout) or AVSS voltage (headphone) for 00000H(@20bit).

DC offsets on the lineout outputs is eliminated by AC coupling since the lineout outputs have a DC offset equal to VCOM plus a few mV.

PACKAGE

● 32pin QFN (Unit: mm)

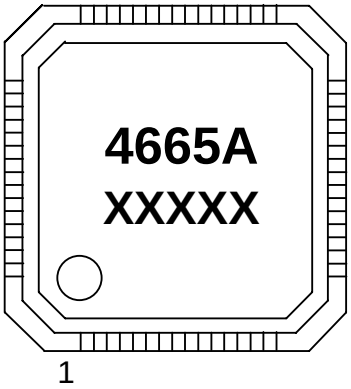


Note: The exposed pad on the bottom surface of package must be open or connected to ground.

■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXXX : Date code identifier (5 digits)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
05/11/22	00	First Edition		
06/05/11	01	Spec change	1,13,14	MCLK=256fs/384fs/512fs → 256fs/512fs
			49	System Design 2Ω series resistor was added at HVDD pin.