TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

# TLCS-900/L Series

## TMP93PW32

TOSHIBA CORPORATION

Semiconductor Company

# Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

**CAUTION**

**How to release the HALT mode**

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{NMI}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of $f_{FPH}$) with IDLE1 or STOP mode (IDLE2/RUN are not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low Voltage/Low Power CMOS

16-bit Microcontrollers

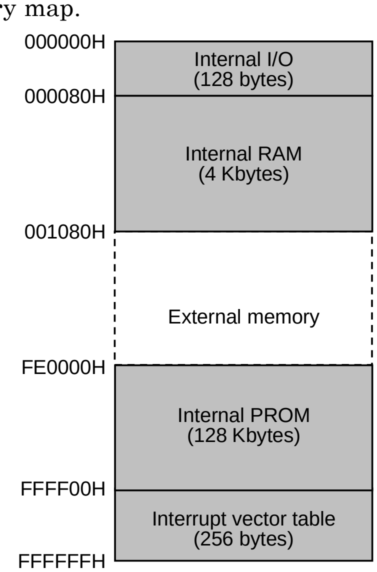
# TMP93PW32F

## 1. Outline and Device Characteristics

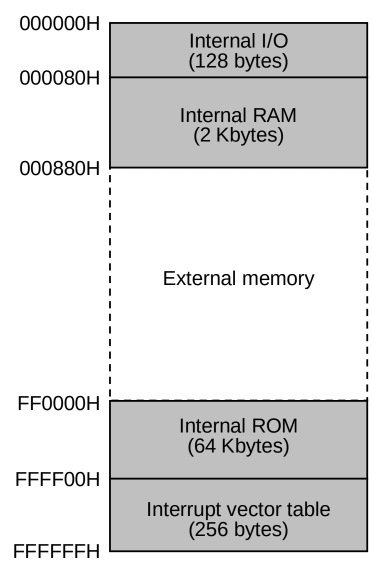
The TMP93PW32 is OTP type MCU which includes 128-Kbyte One-time PROM. Using the adapter-socket (BM11132), you can write and verify the data for the TMP93PW32. The TMP93PW32F has the same pin-assignment as TMP93CS32 (Mask ROM type).

Writing the program to Built-in PROM, the TMP93PW32 operates as the same way as the TMP93CS32.

The memory map and capacity of built in ROM and RAM are different between TMP93CS32 and TMP93PW32. The TMP93PW32 has the PROM of 128 Kbytes and the RAM of 4 Kbytes, and the TMP93CS32 has the ROM of 64 Kbytes and the RAM of 2 Kbytes. Following figure shows each memory map.

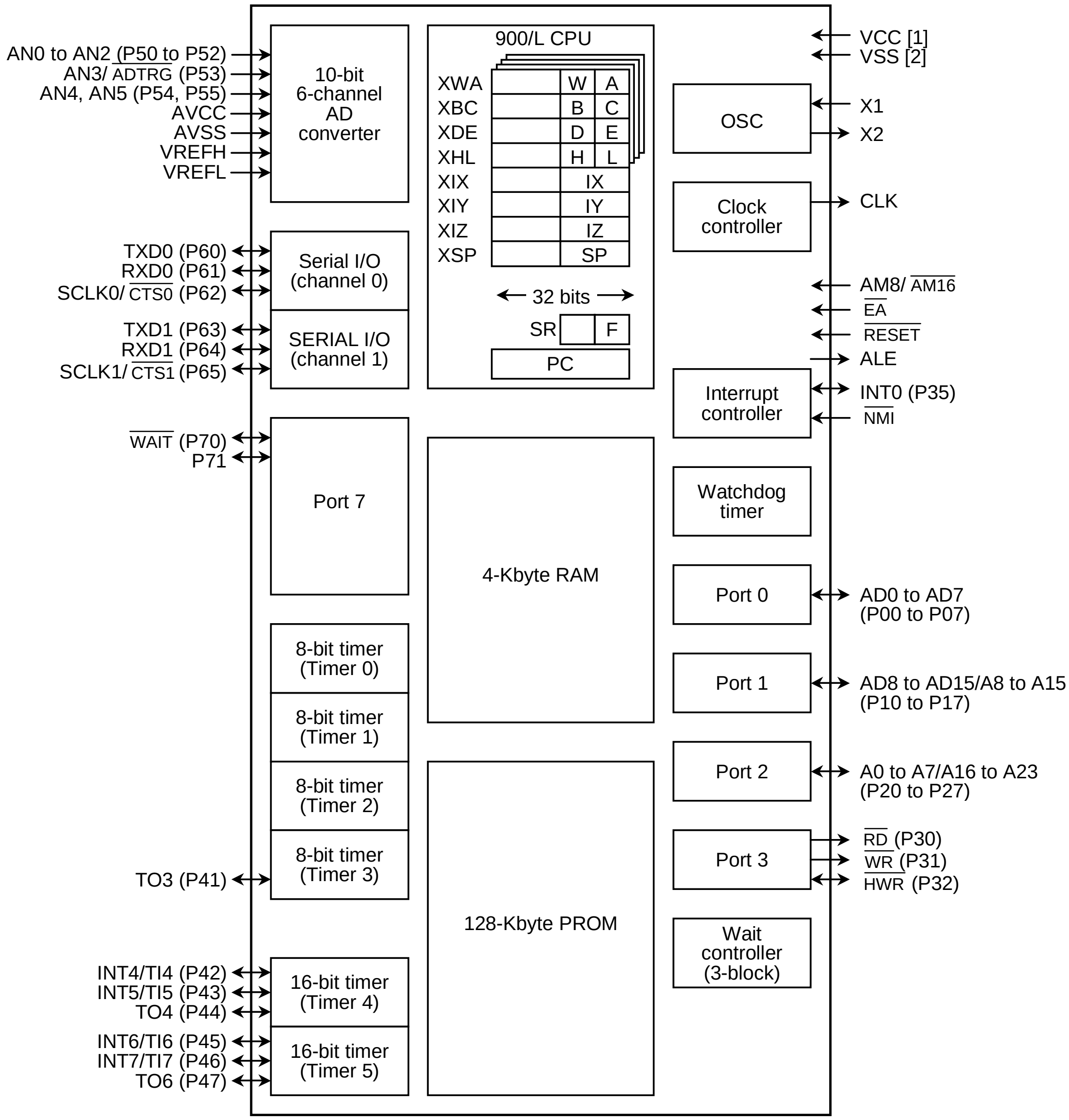



TMP93PW32 memory map




TMP93CS32 memory map

| Product No. | ROM | RAM | Package | Adapter Socket |
|---|---|---|---|---|
| TMP93PW32F | OTP 128 Kbytes | 4 Kbytes | P-QFP64-1414-0.80A | BM11132 |




Note: The items in parentheses ( ) are the initial setting after reset.

Figure 1.1 TMP93PW32 Block Diagram

# 2. Pin Assignment and Functions

The assignment of input/output pins for the TMP93PW32, their names and functions are described below.

## 2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PW32F.

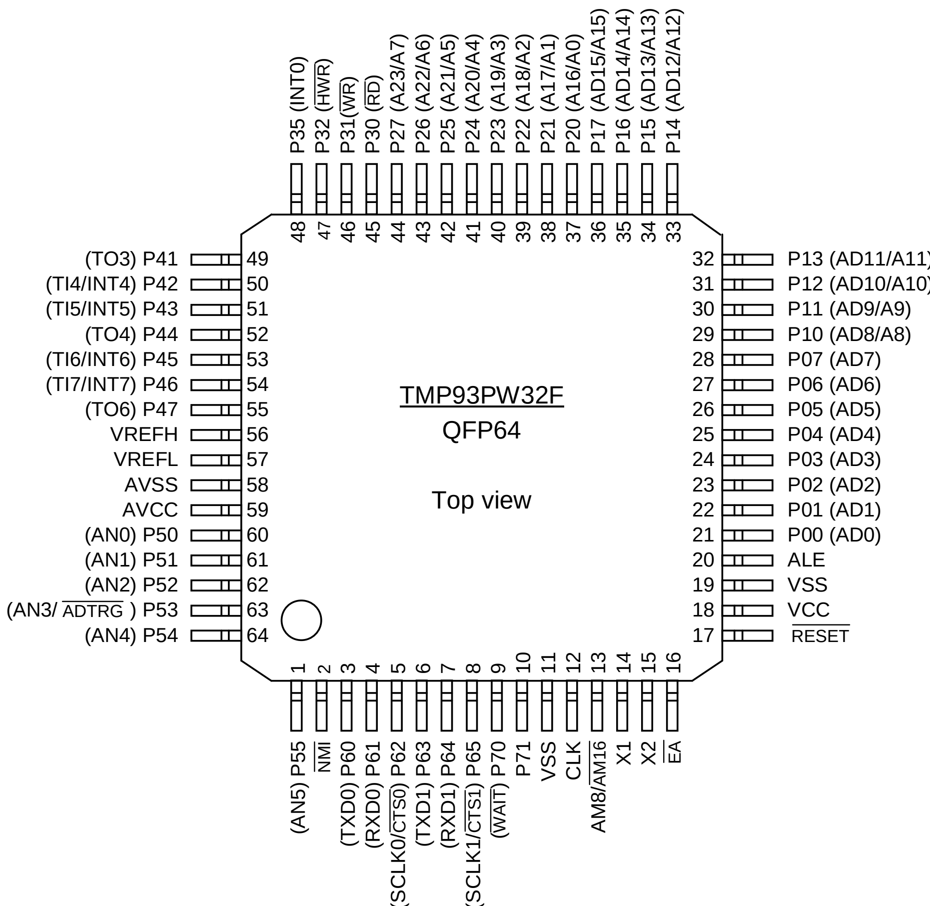



Figure 2.1.1 Pin Assignment (64-pin QFP)

## 2.2 Pin Names and Functions

The TMP93PW32 has MCU mode and PROM mode.

(1) Table 2.2.1 and Table 2.2.2 show pin function of TMP93PW32 in MCU mode.

Table 2.2.1 Pin Names and Function (1/2)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P00 to P07<br>AD0 to AD7 | 8 | I/O | Port 0: I/O port that allows selection of I/O on a bit basis |
| | | 3 states | Address/Data (lower): Bits 0 to 7 for address/data bus |
| P10 to P17<br>AD8 to AD15<br>A8 to A15 | 8 | I/O | Port 1: I/O port that allows selection of I/O on a bit basis |
| | | 3 states | Address/Data (upper): Bits 8 to 15 for address/data bus |
| | | Output | Address: Bits 8 to 15 for address bus |
| P20 to P27<br>A0 to A7<br>A16 to A23 | 8 | I/O | Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor) |
| | | Output | Address: Bits 0 to 7 for address bus |
| | | Output | Address: Bits 16 to 23 for address bus |
| P30<br>$\overline{RD}$ | 1 | Output | Port 30: Output port |
| | | Output | Read: Strobe signal for reading external memory |
| P31<br>$\overline{WR}$ | 1 | Output | Port 31: Output port |
| | | Output | Write: Strobe signal for writing data on pins AD0 to AD7 |
| P32<br>$\overline{HWR}$ | 1 | I/O | Port 32: I/O port (with pull-up resistor) |
| | | Output | High write: Strobe signal for writing data on pins AD8 to AD15 |
| P35<br>INT0 | 1 | I/O | Port 35: I/O port |
| | | Input | Interrupt request pin 0: Interrupt request pin with programmable level/rising edge |
| P41<br>TO3 | 1 | I/O | Port 41: I/O port |
| | | Output | PWM output 3: 8-bit PWM timer 3 output |
| P42<br>TI4<br>INT4 | 1 | I/O | Port 42: I/O port |
| | | Input | Timer input 4: Timer 4 count/capture trigger signal input |
| | | Input | Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge |
| P43<br>TI5<br>INT5 | 1 | I/O | Port 43: I/O port |
| | | Input | Timer input 5: Timer 4 count/capture trigger signal input |
| | | Input | Interrupt request pin 5: Interrupt request pin with rising edge |
| P44<br>TO4 | 1 | I/O | Port 44: I/O port |
| | | Output | Timer output 4: Timer 4 output pin |
| P45<br>TI6<br>INT6 | 1 | I/O | Port 45: I/O port |
| | | Input | Timer input 6: Timer 5 count/capture trigger signal input |
| | | Input | Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge |
| P46<br>TI7<br>INT7 | 1 | I/O | Port 46: I/O port |
| | | Input | Timer input 7: Timer 5 count/capture trigger signal input |
| | | Input | Interrupt request pin 7: Interrupt request pin with rising edge |
| P47<br>TO6 | 1 | I/O | Port 47: I/O port |
| | | Output | Timer output 6: Timer 5 output pin |

Table 2.2.2 Pin Names and Function (2/2)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P50 to P52, P54, P55 | 5 | Input | Port 50 to Port 52, Port 54, Port 55: Input port |
| AN0 to AN2, AN4, AN5 | | Input | Analog input: Analog signal input for AD converter |
| P53 | 1 | Input | Port 53: Input Port |
| AN3 | | Input | Analog input: Analog signal input for AD converter |
| $\overline{\text{ADTRG}}$ | | Input | AD converter external start trigger input |
| P60 | 1 | I/O | Port 60: I/O port (with pull-up resistor) |
| TXD0 | | Output | Serial send data 0 |
| P61 | 1 | I/O | Port 61: I/O port (with pull-up resistor) |
| RXD0 | | Input | Serial receive data 0 |
| P62 | 1 | I/O | Port 62: I/O port (with pull-up resistor) |
| SCLK0 | | I/O | Serial clock I/O 0 |
| $\overline{\text{CTS0}}$ | | Input | Serial data send enable 0 (clear to send) |
| P63 | 1 | I/O | Port 63: I/O port (with pull-up resistor) |
| TXD1 | | Output | Serial send data 1 |
| P64 | 1 | I/O | Port 64: I/O port (with pull-up resistor) |
| RXD1 | | Input | Serial receive data 1 |
| P65 | 1 | I/O | Port 65: I/O port (with pull-up resistor) |
| SCLK1 | | I/O | Serial clock I/O 1 |
| $\overline{\text{CTS1}}$ | | Input | Serial data send enable 1 (clear to send) |
| P70 | 1 | I/O | Port 70: I/O port (High current output available) |
| $\overline{\text{WAIT}}$ | | Input | Wait: Pin used to request CPU bus wait (It is active in (1 + N) waits mode. Set by the bus-width/wait control register.) |
| P71 | 1 | I/O | Port 71: I/O port (High current output available) |
| $\overline{\text{NMI}}$ | 1 | Input | Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program. |
| CLK | 1 | Output | Clock output: Outputs "$f_{SYS} \div 2$" Clock. Pulled-up during reset. Can be disabled for reducing noise. |
| $\overline{\text{EA}}$ | 1 | Input | "1" should be inputted with TMP93PW32. |
| AM8/ $\overline{\text{AM16}}$ | 1 | Input | Address mode: Selects external data bus width. "1" should be inputted. The data bus width for external access is set by chip select/wait control register and Port 1 control register. |
| ALE | 1 | Output | Address Latch Enable Can be disabled for reducing noise. |
| $\overline{\text{RESET}}$ | 1 | Input | Reset: Initializes TMP93PW32. (with pull-up resistor) |
| VREFH | 1 | Input | Pin for high level reference voltage input to AD converter |
| VREFL | 1 | Input | Pin for low level reference voltage input to AD converter |
| AVCC | 1 | Input | Power supply pin for AD converter |
| AVSS | 1 | Input | GND pin for AD converter (0 V) |
| X1 | 1 | Input | Oscillator connecting pin |
| X2 | 1 | Output | Oscillator connecting pin |
| VCC | 1 | Input | Power supply pin |
| VSS | 2 | Input | GND pin (All VSS pins are connected to the GND (0 V).) |

Note: Built-in pull-up resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

(2) PROM mode

Table 2.2.3 shows pin function of the TMP93PW32 in PROM mode.

Table 2.2.3 Pin Name and Function of PROM Mode

| Pin Function | Number of Pins | Input/ Output | Function | Pin Name (MCU Mode) |
|---|---|---|---|---|
| A7 to A0 | 8 | Input | Memory address of program | P27 to P20 |
| A15 to A8 | 8 | Input | | P17 to P10 |
| A16 | 1 | Input | | P71 |
| D7 to D0 | 8 | I/O | Memory data of program | P07 to P00 |
| $\overline{\text{CE}}$ | 1 | Input | Chip enable | P32 |
| $\overline{\text{OE}}$ | 1 | Input | Output control | P30 |
| $\overline{\text{PGM}}$ | 1 | Input | Program control | P31 |
| VPP | 1 | Power supply | 12.75 V/5 V (Power supply of program) | $\overline{\text{EA}}$ |
| VCC | 2 | Power supply | 6.25 V/5 V | VCC, AVCC |
| VSS | 3 | Power supply | 0 V | VSS, AVSS |

| Pin Function | Number of Pins | Input/ Output | Disposal of Pin |
|---|---|---|---|
| P60 | 1 | Input | Fix to low level (security pin) |
| $\overline{\text{RESET}}$ | 1 | Input | Fix to low level (PROM mode) |
| CLK | 1 | Input | |
| ALE | 1 | Output | Open |
| X1 | 1 | Input | Self oscillation with resonator |
| X2 | 1 | Output | |
| P65 to P61<br>AM8/ $\overline{\text{AM16}}$ | 6 | Input | Fix to high level |
| P35<br>P47 to P41<br>P55 to P50<br>P70<br>VREFH<br>VREFL<br>$\overline{\text{NMI}}$ | 18 | I/O | Open |

# 3. Operation

This section describes the functions and basic operational blocks of the TMP93PW32.

The TMP93PW32 has PROM in place of the mask ROM which is included in the TMP93CS32. The other configuration and functions are the same as the TMP93CS32. Regarding the functions of the TMP93PW32 (Not described), see the part of TMP93CS32.

The TMP93PW32 has two operational modes: MCU mode and PROM mode.

## 3.1 MCU Mode

(1) Mode-setting and function

The MCU mode is set by opening the CLK pin (Pin open). In the MCU mode, the operation is same as TMP93CS32 except the followings.

(2) Memory map

The memory map of TMP93PW32 is not same as that of TMP93CS32.

Figure 3.1.1 shows the memory map in MCU mode. Figure 3.1.2 show that in PROM mode.

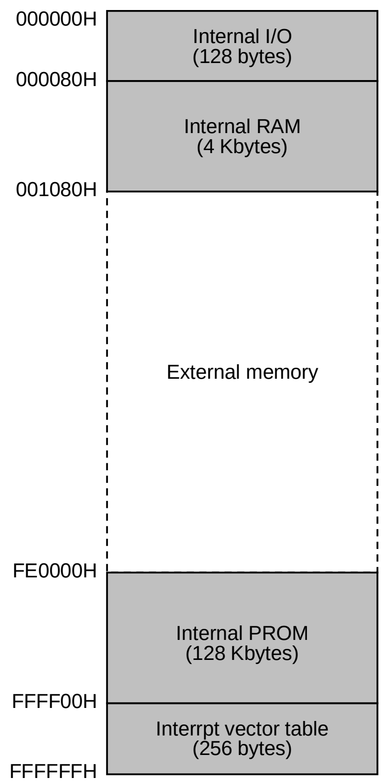



Figure 3.1.1 Memory Map in MCU Mode

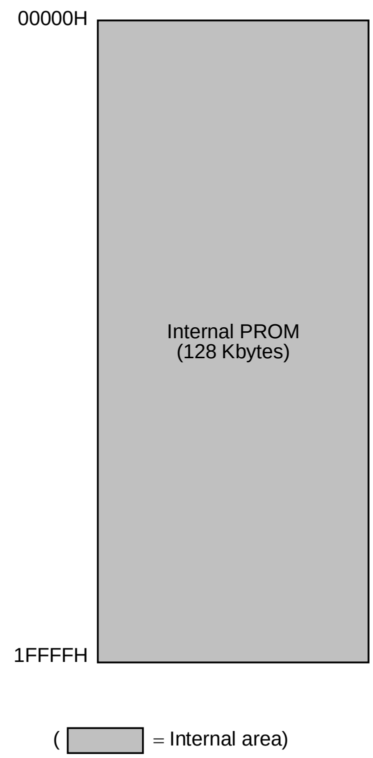



Figure 3.1.2 Memory Map in PROM Mode

(3) Care point of bus width/wait controller

The built in RAM capacity of the TMP93PW32 is larger than that of the TMP93CS32, therefore the following point is different about the accessing area of WAITC1.

Setting WAITC1<B1C1:0> to “00”

| TMP93PW32 | TMP93CS32 |
|---|---|
| 1080H to 7FFFH | 880 to 7FFFH |

WAITC0 and WAITC2 addressing area are the same as TMP93CS32.

## 3.2 PROM Mode

(1) Mode setting and function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level. The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket.

1. Preparation of OTP adaptor

   BM11132: for TMP93PW32

2. Setting of OTP adaptor

   The switch (SW1) is set to N side.

3. Setting of PROM writer

   i) Set PROM type to TC 571000D.

      Size: 1 Mbits (128 K × 8 bits)

      VPP: 12.75 V

      $t_{PW}$: 100 μs

      Electric signature mode: none

   ii) Data transmittion

      In TMP93PW32F, PROM is placed on addresses 00000 to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode. (See instruction manual of PROM programmer.)

   iii) Setting of the program address

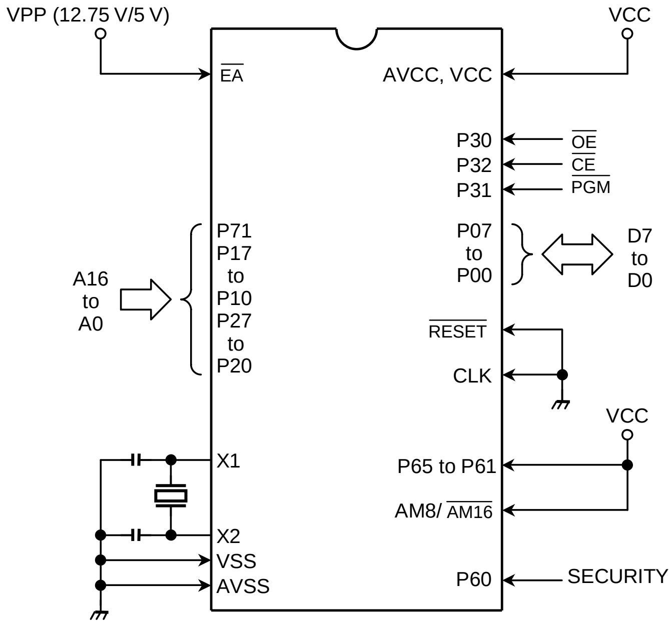
      Start address: 00000H

      End address: 1FFFFH

4. Programming

   Program and verify according to operating process of PROM programmer.

Figure 3.2.1 shows the setting of the pins in PROM mode.




For other pins, refer to the section on pin functions (Table 2.2.2 ).

* Use the 10 MHz resonator in case of programming and verification by a general PROM programmer.

Figure 3.2.1 PROM Mode Pin Setting

(2) Caution for electric signature

The TMP93PW32 dose not support the electric signature mode (hereinafter referred to as "signature"). If PROM programmer used the signature, the device would be damaged because of applying voltage of 12 ± 0.5 V to pin 9 (A9) of the address.

Please use without setting the signature.

(3) Program mode

All bits of the TMP93PW32 are "1" when delivered (the erase state). Data "0" is written in the necessary bit location during program operating.

Writing function can be operated at $V_{PP}$ = 12.5 V, $\overline{OE}$ = $V_{IH}$, $\overline{CE}$ = $V_{IL}$. Built-in one time PROM can be written in any sequence. It is possible to write only special address.

(4) Adopter socket (BM11132)

BM11132 is the adapter sockets to write data into the TMP93PW32F. The TMP93PW32F has built-in one time PROM using a general EPROM programmer.

(5) Program storing area of PROM mode

The TMP93PW32 has the program space (FE0000H to FFFFFFH) of 128 Kbytes. The address 00000H to 1FFFFH of PROM mode equals to the address FE0000H to FFFFFFH of MCU mode.

(6) Program write setting method using a general PROM programmer

PROM to be prepared should equal to TC571000D functions.

1. Set the switch (SW1) of BM11132 (hereinafter referred to as “adapter”) to the program side (NOR) (Note 1).
2. Connect MCU to the adapter (Note 2).
3. Connect the adapter to PROM programmer (Note 2).
4. Set the PROM type of PROM programmer to TC571000D.
5. Set the start address for writing PROM to 00000H, and the end address to 1FFFFH (Note 3).
6. Writing to built-in one time PROM and verifying should be operated according to the operation procedures of PROM programmer.

Note 1: If data is written to built-in one time PROM without setting the switch (SW1) to the program side, the device would be damaged.

Note 2: Please set with the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or programmer would be damaged.

Note 3: If data “0” is written to the address which is over 1FFFFH, the contents of the original program would be damaged because of writing “0” to the addresses 00000H to 1FFFFH.

(7) Programming flow chart

The programming mode is set by applying 12.75 V (Programming voltage) to the VPP pin when the following pins are set as follows,
(VCC: 6.25 V, $\overline{\text{RESET}}$ : “L” level, CLK: “L” level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to “L” level, 0.1 ms of “L” level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of VPP = VCC = 5 V after all data were written.

Figure 3.2.2 shows the programming flow chart.

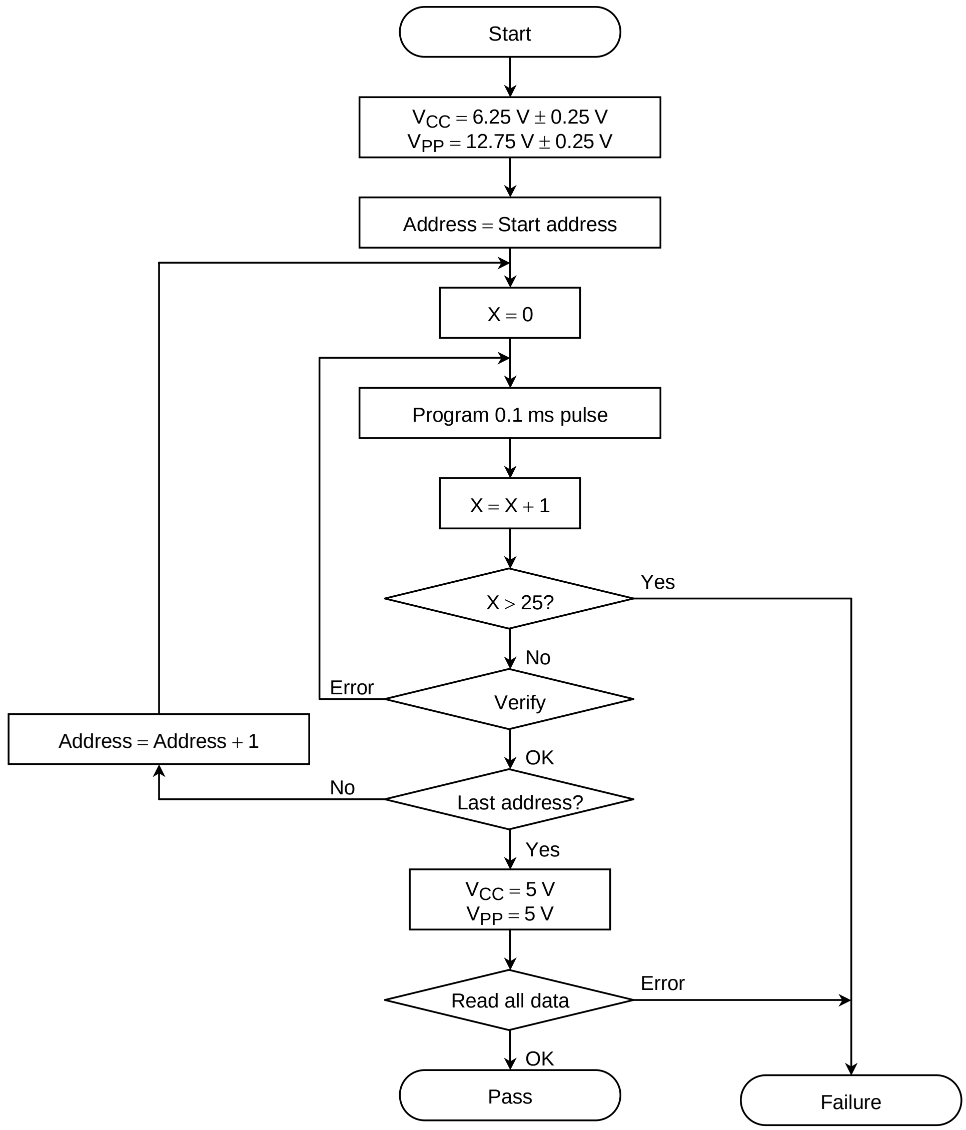



Figure 3.2.2 Flow Chart (High-speed program writing)

(8) Security bit

The TMP93PW32 has a security bit in PROM cell.

If the security bit is programmed to “0”, the content of the PROM is disable to be read (FFH data) in PROM mode.

(How to program the security bit.)

The difference from the programming procedures described in section 3.2 (1) are follows.

1. Setting OTP adaptor

   Set the switch (SW1) to S side.

2. Setting PROM programmer

   i) Transferring the data

   ii) Setting of programming address

   The security bit is in bit0 of address 00000H.

   Set the start address 00000H and the end address 00000H.

   Set the data FEH at the address 00000H.

# 4. Electrical Characteristics

"X" used in an expression shows a cycle of clock $f_{FPH}$. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is gear = 1/fc (SYSCR1<GEAR2:0> = "000").

## 4.1 Absolute Maximum Ratings (TMP93PW32)

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | −0.5 to 6.5 | | V |
| Input voltage | $V_{IN}$ | Except $\overline{EA}$ pin | −0.5 to $V_{CC}$ + 0.5 | V |
| | | $\overline{EA}$ pin | −0.5 to 14.0 | V |
| Output current (per 1 pin) P7 | $I_{OL1}$ | 20 | | mA |
| Output current (per 1 pin) except P7 | $I_{OL2}$ | 2 | | mA |
| Output current (total) | $\Sigma I_{OL}$ | 120 | | mA |
| Output current (total) | $\Sigma I_{OH}$ | −80 | | mA |
| Power dissipation (Ta = 85°C) | $P_D$ | 350 | | mW |
| Soldering temperature (10 s) | $T_{SOLDER}$ | 260 | | °C |
| Storage temperature | $T_{STG}$ | −65 to 150 | | °C |
| Operating temperature | $T_{OPR}$ | −40 to 85 | | °C |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 4.2 DC Characteristics

Ta = −40 to 85°C

| Parameter | | Symbol | Condition | Min | Typ. (Note) | Max | Unit |
|---|---|---|---|---|---|---|---|
| Power supply voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$ = 0 V) | | $V_{CC}$ | fc = 4 to 20 MHz | 4.5 | | 5.5 | V |
| | | | fc = 4 to 12.5 MHz | 2.7 | | 5.5 | V |
| Input low voltage | AD0 to AD15 | $V_{IL}$ | $V_{CC}$ ≥ 4.5 V | −0.3 | | 0.8 | V |
| | | | $V_{CC}$ < 4.5 V | −0.3 | | 0.6 | V |
| | Port 2 to 7 (except P35) | $V_{IL1}$ | $V_{CC}$ = 2.7 to 5.5 V | −0.3 | | 0.3 $V_{CC}$ | V |
| | $\overline{RESET}$, $\overline{NMI}$, INT0 | $V_{IL2}$ | $V_{CC}$ = 2.7 to 5.5 V | −0.3 | | 0.25 $V_{CC}$ | V |
| | $\overline{EA}$, AM8/$\overline{AM16}$ | $V_{IL3}$ | $V_{CC}$ = 2.7 to 5.5 V | −0.3 | | 0.3 | V |
| | X1 | $V_{IL4}$ | $V_{CC}$ = 2.7 to 5.5 V | −0.3 | | 0.2 $V_{CC}$ | V |
| Input high voltage | AD0 to AD15 | $V_{IH}$ | $V_{CC}$ ≥ 4.5 V | 2.2 | | $V_{CC}$ + 0.3 | V |
| | | | $V_{CC}$ < 4.5 V | 2.0 | | $V_{CC}$ + 0.3 | V |
| | Port 2 to 7 (except P35) | $V_{IH1}$ | $V_{CC}$ = 2.7 to 5.5 V | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| | $\overline{RESET}$, $\overline{NMI}$, INT0 | $V_{IH2}$ | $V_{CC}$ = 2.7 to 5.5 V | 0.75 $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| | $\overline{EA}$, AM8/$\overline{AM16}$ | $V_{IH3}$ | $V_{CC}$ = 2.7 to 5.5 V | $V_{CC}$ − 0.3 | | $V_{CC}$ + 0.3 | V |
| | X1 | $V_{IH4}$ | $V_{CC}$ = 2.7 to 5.5 V | 0.8 $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| Output low voltage | | $V_{OL}$ | $I_{OL}$ = 1.6 mA ($V_{CC}$ = 2.7 to 5.5 V) | | | 0.45 | V |
| Output low current (P7) | | $I_{OL7}$ | $V_{OL}$ = 1.0 V ($V_{CC}$ = 5 V ± 10%) | 16 | | | mA |
| | | | $V_{OL}$ = 1.0 V ($V_{CC}$ = 3 V ± 10%) | 7 | | | mA |
| Output high voltage | | $V_{OH1}$ | $I_{OH}$ = −400 μA ($V_{CC}$ = 3 V ± 10%) | 2.4 | | | V |
| | | $V_{OH2}$ | $I_{OH}$ = −400 μA ($V_{CC}$ = 5 V ± 10%) | 4.2 | | | V |

Note: Typical values are for Ta = 25°C and $V_{CC}$ = 5 V unless otherwise noted.

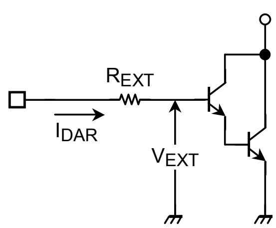
| Parameter | Symbol | Condition | Min | Typ. (Note1) | Max | Unit |
|---|---|---|---|---|---|---|
| Darlington drive current (8 output pins max) | $I_{DAR}$ (Note2) | $V_{EXT}$ = 1.5 V<br>$R_{EXT}$ = 1.1 kΩ<br>($V_{CC}$ = 5 V ± 10% only) | −1.0 | | −3.5 | mA |
| Input leakage current | $I_{LI}$ | $0.0 \le V_{IN} \le V_{CC}$ | | 0.02 | ±5 | μA |
| Output leakage current | $I_{LO}$ | $0.2 \le V_{IN} \le V_{CC} - 0.2$ | | 0.05 | ±10 | |
| Power down voltage (at STOP, RAM back up) | $V_{STOP}$ | $V_{IL2}$ = 0.2 $V_{CC}$,<br>$V_{IH2}$ = 0.8 $V_{CC}$ | 2.0 | | 6.0 | V |
| $\overline{RESET}$ pull-up resistor | $R_{RST}$ | $V_{CC}$ = 5.5 V | 45 | | 130 | kΩ |
| | | $V_{CC}$ = 4.5 V | 50 | | 160 | |
| | | $V_{CC}$ = 3.3 V | 70 | | 280 | |
| | | $V_{CC}$ = 2.7 V | 90 | | 400 | |
| Pin capacitance | $C_{IO}$ | fc = 1 MHz | | | 10 | pF |
| Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0 | $V_{TH}$ | | 0.4 | 1.0 | | V |
| Programmable pull-up resistor | $R_{KH}$ | $V_{CC}$ = 5.5 V | 45 | | 130 | kΩ |
| | | $V_{CC}$ = 4.5 V | 50 | | 160 | |
| | | $V_{CC}$ = 3.3 V | 70 | | 280 | |
| | | $V_{CC}$ = 2.7 V | 90 | | 400 | |
| NORMAL (Note 3) | $I_{CC}$ | $V_{CC}$ = 5 V ± 10%<br>fc = 20 MHz | | 25 | 30 | mA |
| RUN | | | | 22 | 27 | |
| IDLE2 | | | | 13 | 17 | |
| IDLE1 | | | | 3.4 | 5 | |
| NORMAL (Note 3) | | $V_{CC}$ = 3 V ± 10%<br>fc = 12.5 MHz<br>(Typ.: $V_{CC}$ = 3.0 V) | | 8.0 | 11 | |
| RUN | | | | 7.0 | 10 | |
| IDLE2 | | | | 4.2 | 6 | |
| IDLE1 | | | | 1.2 | 1.8 | |
| STOP | | Ta ≤ 50°C, $V_{CC}$ = 2.7 V to 5.5 V | | 0.2 | 10 | μA |
| | | Ta ≤ 70°C | | | 20 | |
| | | Ta ≤ 85°C | | | 50 | |

Note 1: Typical values are for Ta = 25°C and $V_{CC}$ = 5 V unless otherwise noted.

Note 2: $I_{DAR}$ is guranteed for total of up to 8 ports.

Note 3: $I_{CC}$ measurement conditions (NORMAL):
Only CPU is operational; output pins are open and input pins are fixed.

(Reference) Definition of $I_{DAR}$



## 4.3 AC Electrical Characteristics

(1) $V_{CC}$ = 5 V ± 10%

| No. | Parameter | Symbol | Variable | | 16 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | Osc. period (= x) | $t_{OSC}$ | 50 | 31250 | 62.5 | | 50 | | ns |
| 2 | CLK pulse width | $t_{CLK}$ | 2x – 40 | | 85 | | 60 | | ns |
| 3 | A0 to A23 valid → CLK hold | $t_{AK}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 4 | CLK valid → A0 to A23 hold | $t_{KA}$ | 1.5x – 70 | | 24 | | 5 | | ns |
| 5 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 6 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 7 | ALE high pulse width | $t_{LL}$ | x – 40 | | 23 | | 10 | | ns |
| 8 | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall | $t_{LC}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 9 | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise | $t_{CL}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 10 | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACL}$ | x – 25 | | 38 | | 25 | | ns |
| 11 | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 44 | | 25 | | ns |
| 12 | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold | $t_{CA}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 13 | A0 to A15 valid → D0 to D15 input | $t_{ADL}$ | | 3.0x – 55 | | 133 | | 95 | ns |
| 14 | A0 to A23 valid → D0 to D15 input | $t_{ADH}$ | | 3.5x – 65 | | 154 | | 110 | ns |
| 15 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 60 | | 65 | | 40 | ns |
| 16 | $\overline{RD}$ low pulse width | $t_{RR}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 17 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | 0 | | ns |
| 18 | $\overline{RD}$ rise → A0 to A15output | $t_{RAE}$ | x – 15 | | 48 | | 35 | | ns |
| 19 | $\overline{WR}$ low pulse width | $t_{WW}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 20 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 55 | | 70 | | 45 | | ns |
| 21 | $\overline{WR}$ rise → D0 to D15 hold | $t_{WD}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 22 | A0 to A23 valid → $\overline{WAIT}$ input (1 + n WAIT mode) | $t_{AWH}$ | | 3.5x – 90 | | 129 | | 85 | ns |
| 23 | A0 to A15 valid → $\overline{WAIT}$ input (1 + n WAIT mode) | $t_{AWL}$ | | 3.0x – 80 | | 108 | | 70 | ns |
| 24 | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + n WAIT mode) | $t_{CW}$ | 2.0x + 0 | | 125 | | 100 | | ns |
| 25 | A0 to A23 valid → Port input | $t_{APH}$ | | 2.5x – 120 | | 36 | | 5 | ns |
| 26 | A0 to A23 valid → Port hold | $t_{APH2}$ | 2.5x + 50 | | 206 | | 175 | | ns |
| 27 | $\overline{WR}$ rise → Port valid | $t_{CP}$ | | 200 | | 200 | | 200 | ns |

AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × $V_{CC}$/Low 0.2 × $V_{CC}$ (Except for AD0 to AD15)

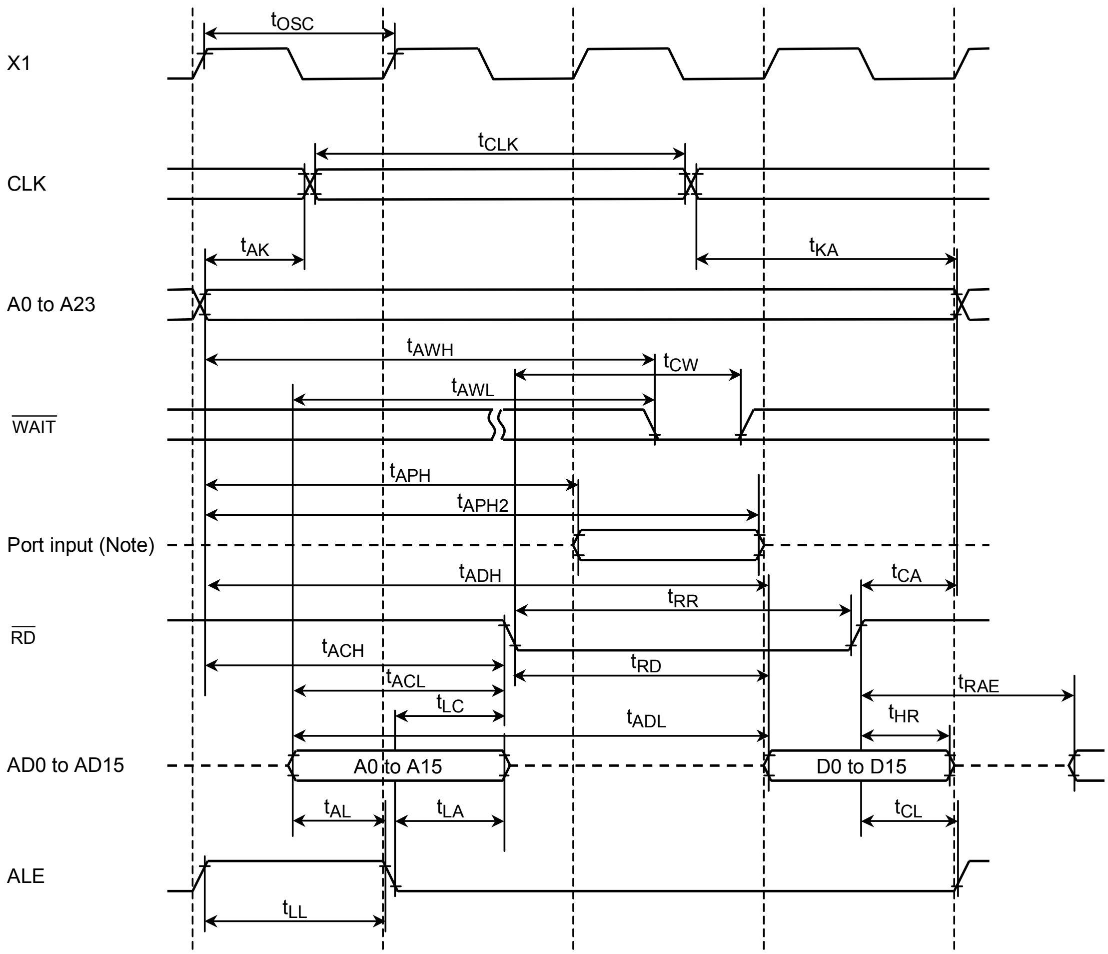
(2) $V_{CC}$ = 3 V ± 10%

| No. | Parameter | Symbol | Variable | | 12.5 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | Osc. period (= x) | $t_{OSC}$ | 80 | 31250 | 80 | | ns |
| 2 | CLK pulse width | $t_{CLK}$ | 2x – 40 | | 120 | | ns |
| 3 | A0 to A23 valid → CLK hold | $t_{AK}$ | 0.5x – 30 | | 10 | | ns |
| 4 | CLK valid → A0 to A23 hold | $t_{KA}$ | 1.5x – 80 | | 40 | | ns |
| 5 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 35 | | 5 | | ns |
| 6 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 35 | | 5 | | ns |
| 7 | ALE high pulse width | $t_{LL}$ | x – 60 | | 20 | | ns |
| 8 | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall | $t_{LC}$ | 0.5x – 35 | | 5 | | ns |
| 9 | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise | $t_{CL}$ | 0.5x – 40 | | 0 | | ns |
| 10 | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACL}$ | x – 50 | | 30 | | ns |
| 11 | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 70 | | ns |
| 12 | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold | $t_{CA}$ | 0.5x – 40 | | 0 | | ns |
| 13 | A0 to A15 valid → D0 to D15 input | $t_{ADL}$ | | 3.0x – 110 | | 130 | ns |
| 14 | A0 to A23 valid → D0 to D15 input | $t_{ADH}$ | | 3.5x – 125 | | 155 | ns |
| 15 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 115 | | 45 | ns |
| 16 | $\overline{RD}$ low pulse width | $t_{RR}$ | 2.0x – 40 | | 120 | | ns |
| 17 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | ns |
| 18 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 25 | | 55 | | ns |
| 19 | $\overline{WR}$ low pulse width | $t_{WW}$ | 2.0x – 40 | | 120 | | ns |
| 20 | D0 to D15 Valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 120 | | 40 | | ns |
| 21 | $\overline{WR}$ rise → D0 to D15 hold | $t_{WD}$ | 0.5x – 40 | | 0 | | ns |
| 22 | A0 to A23 valid → $\overline{WAIT}$ input (1 + n WAIT mode) | $t_{AWH}$ | | 3.5x – 130 | | 150 | ns |
| 23 | A0 to A15 valid → $\overline{WAIT}$ input (1 + n WAIT mode) | $t_{AWL}$ | | 3.0x – 100 | | 140 | ns |
| 24 | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + n WAIT mode) | $t_{CW}$ | 2.0x + 0 | | 160 | | ns |
| 25 | A0 to A23 valid → Port input | $t_{APH}$ | | 2.5x – 195 | | 5 | ns |
| 26 | A0 to A23 valid → Port hold | $t_{APH2}$ | 2.5x + 50 | | 250 | | ns |
| 27 | $\overline{WR}$ rise → Port valid | $t_{CP}$ | | 200 | | 200 | ns |

AC measuring conditions

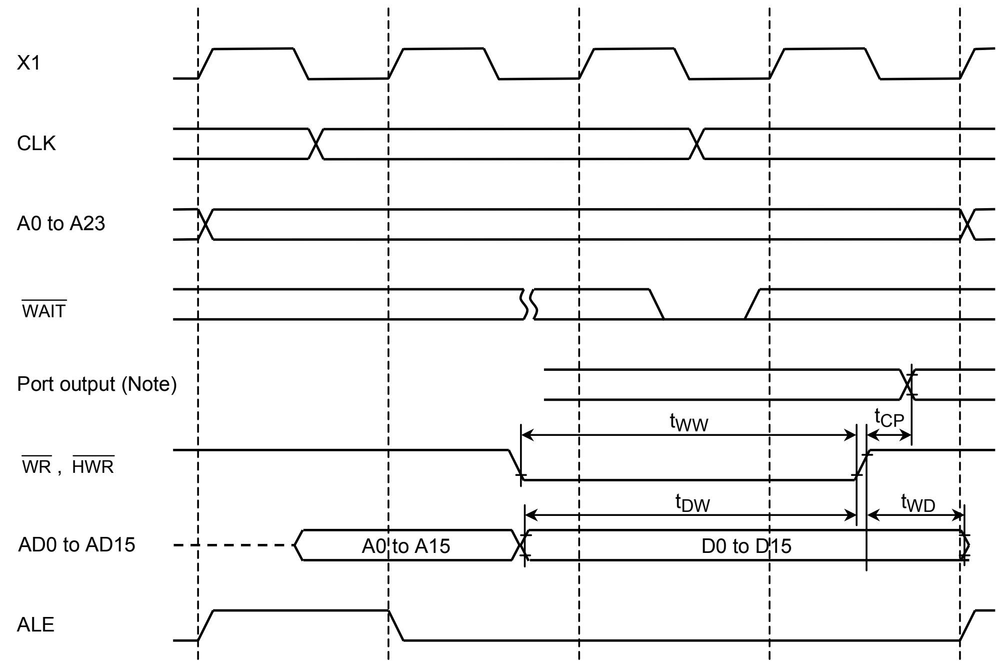
- Output level: High 0.7 × $V_{CC}$/Low 0.3 × $V_{CC}$, CL = 50 pF
- Input level: High 0.9 × $V_{CC}$/Low 0.1 × $V_{CC}$

(3) Read cycle




Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(4) Write cycle




Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

## 4.4 Serial Channel Timing

(1) I/O interface mode

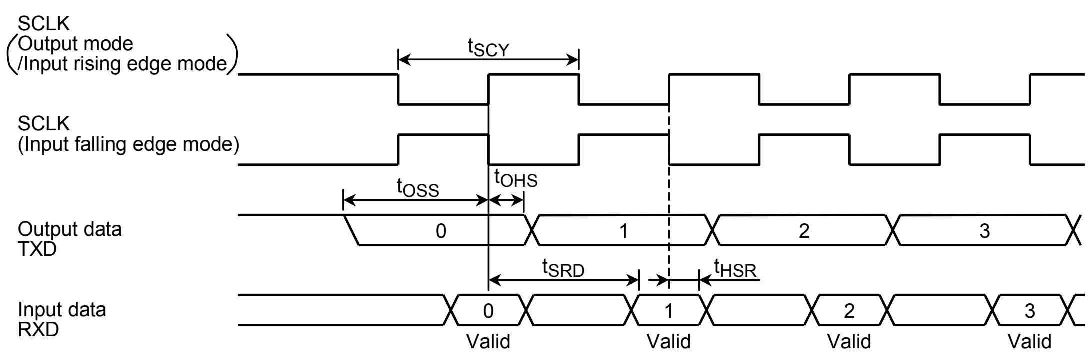
a. SCLK input mode

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCLK cycle | $t_{SCY}$ | 16x | | 1.28 μs | | 0.8 μs | | ns |
| Output data → Rising/falling edge of SCLK | $t_{OSS}$ | $t_{SCY}$/2 − 5x − 50 | | 190 | | 100 | | ns |
| SCLK rising/falling edge → Output data hold | $t_{OHS}$ | 5x − 100 | | 300 | | 150 | | ns |
| SCLK rising/falling edge → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | ns |
| SCLK rising/falling edge → Effective data input | $t_{SRD}$ | | $t_{SCY}$ − 5x − 100 | | 780 | | 450 | ns |

Note: SCLK rising/falling timing ; SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

b. SCLK output mode

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCLK cycle (programmable) | $t_{SCY}$ | 16x | 8192x | 1.28 μs | 655.36 μs | 0.8 μs | 409.6 μs | ns |
| Output data → SCLK rising edge | $t_{OSS}$ | $t_{SCY}$ − 2x − 150 | | 970 | | 550 | | ns |
| SCLK rising edge → Output data hold | $t_{OHS}$ | 2x − 80 | | 80 | | 20 | | ns |
| SCLK rising edge → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | ns |
| SCLK rising edge → Effective data input | $t_{SRD}$ | | $t_{SCY}$ − 2x − 150 | | 970 | | 550 | ns |




(2) UART mode (SCLK0 and SCLK1 are external input)

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCLK cycle | $t_{SCY}$ | 4x + 20 | | 340 | | 220 | | ns |
| SCLK low level pulse width | $t_{SCYL}$ | 2x + 5 | | 165 | | 105 | | ns |
| SCLK high level pulse width | $t_{SCYH}$ | 2x + 5 | | 165 | | 105 | | ns |

## 4.5 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

| Parameter | Symbol | Power Supply | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Analog reference voltage (+) | $V_{REFH}$ | $V_{CC}$ = 5 V ± 10% | $V_{CC}$ − 1.5 | $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC}$ = 3 V ± 10% | $V_{CC}$ − 0.2 | $V_{CC}$ | $V_{CC}$ | |
| Analog reference voltage (−) | $V_{REFL}$ | $V_{CC}$ = 5 V ± 10% | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.2 | |
| | | $V_{CC}$ = 3 V ± 10% | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.2 | |
| Analog input voltage range | $V_{AIN}$ | | $V_{REFL}$ | | $V_{REFH}$ | |
| Analog current for analog reference voltage <VREFON> = 1 | $I_{REF}$ ($V_{REFL}$ = 0 V) | $V_{CC}$ = 5 V ± 10% | | 0.5 | 1.5 | mA |
| | | $V_{CC}$ = 3 V ± 10% | | 0.3 | 0.9 | |
| <VREFON> = 0 | | $V_{CC}$ = 2.7 to 5.5 V | | 0.02 | 5.0 | μA |
| Error (except quantization errors) | − | $V_{CC}$ = 5 V ± 10% | | ±1.0 | ±3.0 | LSB |
| | | $V_{CC}$ = 3 V ± 10% | | ±1.0 | ±5.0 | |

Note 1: 1LSB = $(V_{REFH} - V_{REFL})/2^{10}$ [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value $I_{CC}$ includes the current which flows through the AVCC pin.

## 4.6 Event Counter Input Clock (External Input Clock: TI4, TI5, TI6, TI7)

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Clock cycle | $t_{VCK}$ | 8X + 100 | | 740 | | 500 | | ns |
| Low level clock pulse width | $t_{VCKL}$ | 4X + 40 | | 360 | | 240 | | ns |
| High level clock pulse width | $t_{VCKH}$ | 4X + 40 | | 360 | | 240 | | ns |

## 4.7 Interrupt and Capture Operation

(1) $\overline{\text{NMI}}$ and INT0 Interrupts

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $\overline{\text{NMI}}$, INT0 low level pulse width | $t_{INTAL}$ | 4X | | 320 | | 200 | | ns |
| $\overline{\text{NMI}}$, INT0 high level pulse width | $t_{INTAH}$ | 4X | | 320 | | 200 | | ns |

(2) INT4 to INT7 Interrupts and Capture

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| INT4 to INT7 low level pulse width | $t_{INTBL}$ | 4X + 100 | | 420 | | 300 | | ns |
| INT4 to INT7 high level pulse width | $t_{INTBH}$ | 4X + 100 | | 420 | | 300 | | ns |

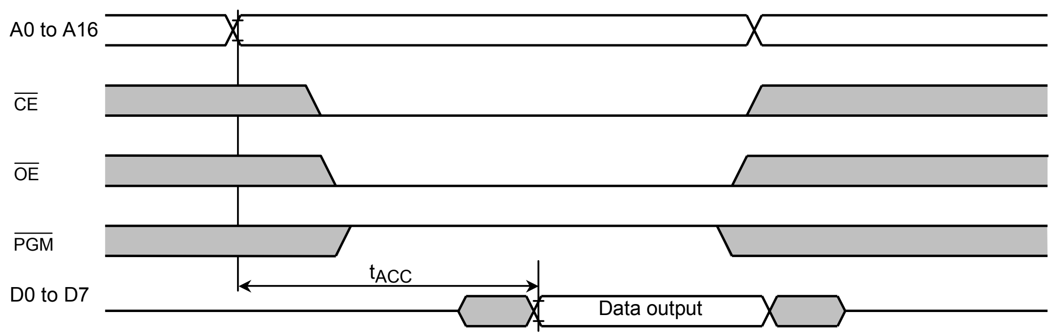
## 4.8 Read Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C, $V_{CC}$ = 5 V ± 10%

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{PP}$ read voltage | $V_{PP}$ | – | 4.5 | 5.5 | V |
| Input high voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IH1}$ | – | 2.2 | $V_{CC}$ + 0.3 | |
| Input low voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IL1}$ | – | −0.3 | 0.8 | |
| Address to output delay | $t_{ACC}$ | CL = 50 pF | – | 2.25 $T_{CYC}$ + α | ns |

$T_{CYC}$ = 400 ns (10 MHz Clock)
α = 200 ns

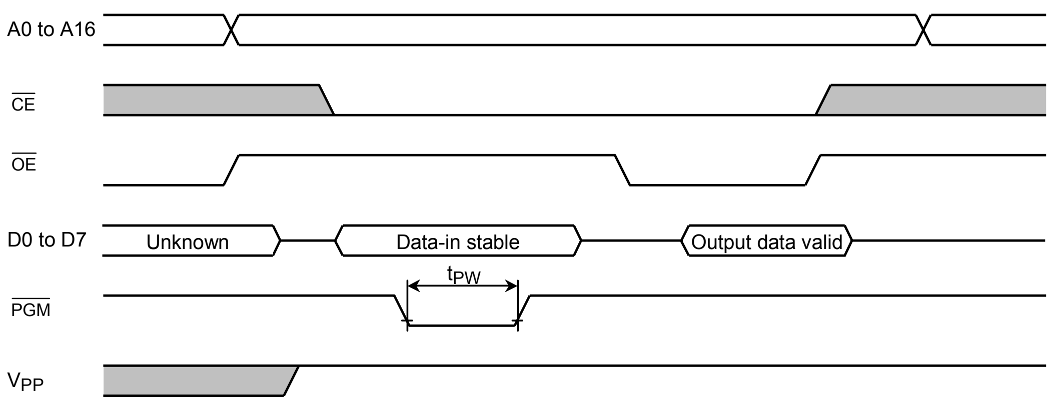


## 4.9 Program operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C, $V_{CC}$ = 6.25 V ± 0.25 V

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Programming supply voltage | $V_{PP}$ | – | 12.50 | 12.75 | 13.00 | V |
| Input high voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IH}$ | – | 2.6 | | $V_{CC}$ + 0.3 | |
| Input low voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IL}$ | – | –0.3 | | 0.8 | |
| $V_{CC}$ supply current | $I_{CC}$ | fc = 10 MHz | – | | 50 | mA |
| $V_{PP}$ supply current | $I_{PP}$ | $V_{PP}$ = 13.00 V | – | | 50 | |
| $\overline{PGM}$ program pulse width | $t_{PW}$ | $C_L$ = 50 pF | 0.095 | 0.1 | 0.105 | ms |




Note 1: The power supply of $V_{PP}$ (12.75 V) must be set power on at the same time or the later time for a power supply of $V_{CC}$ and must be clear power on at the same time or early time for a power supply of $V_{CC}$.

Note 2: The pulling up/down device on condition of $V_{PP}$ = 12.75 V suffer a damage for the device.

Note 3: The maximum spec of $V_{PP}$ pin is 14.0 V. Be carefull a overshoot at the program writing.

# 5. Package Dimensions

P-QFP64-1414-0.80A

Unit: mm