TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

288Mbits Network FCRAM2
– 2,097,152-WORDS × 4 BANKS × 36-BITS

DESCRIPTION

Network FCRAM™ is Double Data Rate Fast Cycle Random Access Memory. TC59LM836DKB is Network FCRAM™ containing 301,989,888 memory cells. TC59LM836DKB is organized as 2,097,152-words × 4 banks × 36 bits. TC59LM836DKB feature a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. TC59LM836DKB can operate fast core cycle compared with regular DDR SDRAM.

TC59LM836DKB is suitable for Network and other applications where large memory density and low power consumption are required. The Output Driver for Network FCRAM™ is capable of high quality fast data transfer under light loading condition.

FEATURES

PARAMETER			TC59LM836DKB		
			-30	-33	-40
t_{CK}	Clock Cycle Time (min)	CL = 4	4.0 ns	4.5 ns	5.0 ns
		CL = 5	3.5 ns	3.75 ns	4.5 ns
		CL = 6	3.0 ns	3.33 ns	4.0 ns
t_{RC}	Random Read/Write Cycle Time (min)		20.0 ns	22.5 ns	25 ns
t_{RAC}	Random Access Time (max)		20.0 ns	22.5 ns	25 ns
I_{DD1S}	Operating Current (single bank) (max)		380 mA	360 mA	340 mA
I_{DD2P}	Power Down Current (max)		100 mA	95 mA	90 mA
I_{DD6}	Self-Refresh Current (max)		15 mA	15 mA	15 mA

- Fully Synchronous Operation
  - Double Data Rate (DDR)
    Data input/output are synchronized with both edges of DS / QS.
  - Differential Clock (CLK and $\overline{\text{CLK}}$) inputs
    $\overline{\text{CS}}$, FN and all address input signals are sampled on the positive edge of CLK.
    Output data (DQs and QS) is aligned to the crossings of CLK and $\overline{\text{CLK}}$.
- Fast clock cycle time of 3.0 ns minimum
  Clock: 333 MHz maximum
  Data: 666 Mbps/pin maximum
- Quad Independent Banks operation
- Fast cycle and Short Latency
- Selectable Data Strobe
- Distributed Auto-Refresh cycle in 3.9 μs
- Self-Refresh
- Power Down Mode
- Variable Write Length Control
- Write Latency = $\overline{\text{CAS}}$ Latency-1
- Programable $\overline{\text{CAS}}$ Latency and Burst Length
  $\overline{\text{CAS}}$ Latency = 4, 5, 6
  Burst Length = 2, 4
- Organization: 2,097,152 words × 4 banks × 36 bits
- Power Supply Voltage V_{DD}: 2.5 V ± 0.125V
  V_{DDQ}: 1.4 V ~ 1.9 V
- Low voltage CMOS I/O covered with SSTL_18 (Half strength driver) and HSTL.
- JTAG boundary scan
- Package: 144Ball BGA, 1mm × 0.8mm Ball pitch (P-TFBGA144-1119-0.80BZ)

Notice: FCRAM is trademark of Fujitsu limited, Japan.

PIN NAMES

PIN	NAME
A0~A13	Address Input
BA0, BA1	Bank Address
DQ0~DQ35	Data Input/Output
$\overline{CS}$	Chip Select
FN	Function Control
$\overline{PD}$	Power Down Control
CLK, $\overline{CLK}$	Clock Input
LDS, UDS	Write Data Strobe
LQS, UQS	Read Data Strobe
V_{DD}	Power (+2.5 V)
V_{SS}	Ground
V_{DDQ}	Power (+1.5V / +1.8 V) (for DQ buffer)
V_{SSQ}	Ground (for DQ buffer)
V_{REF}	Reference Voltage
NC	Not Connected
TMS, TDI, TCK, TDO	Boundary Scan Test Access Ports

PIN ASSIGNMENT (TOP VIEW)

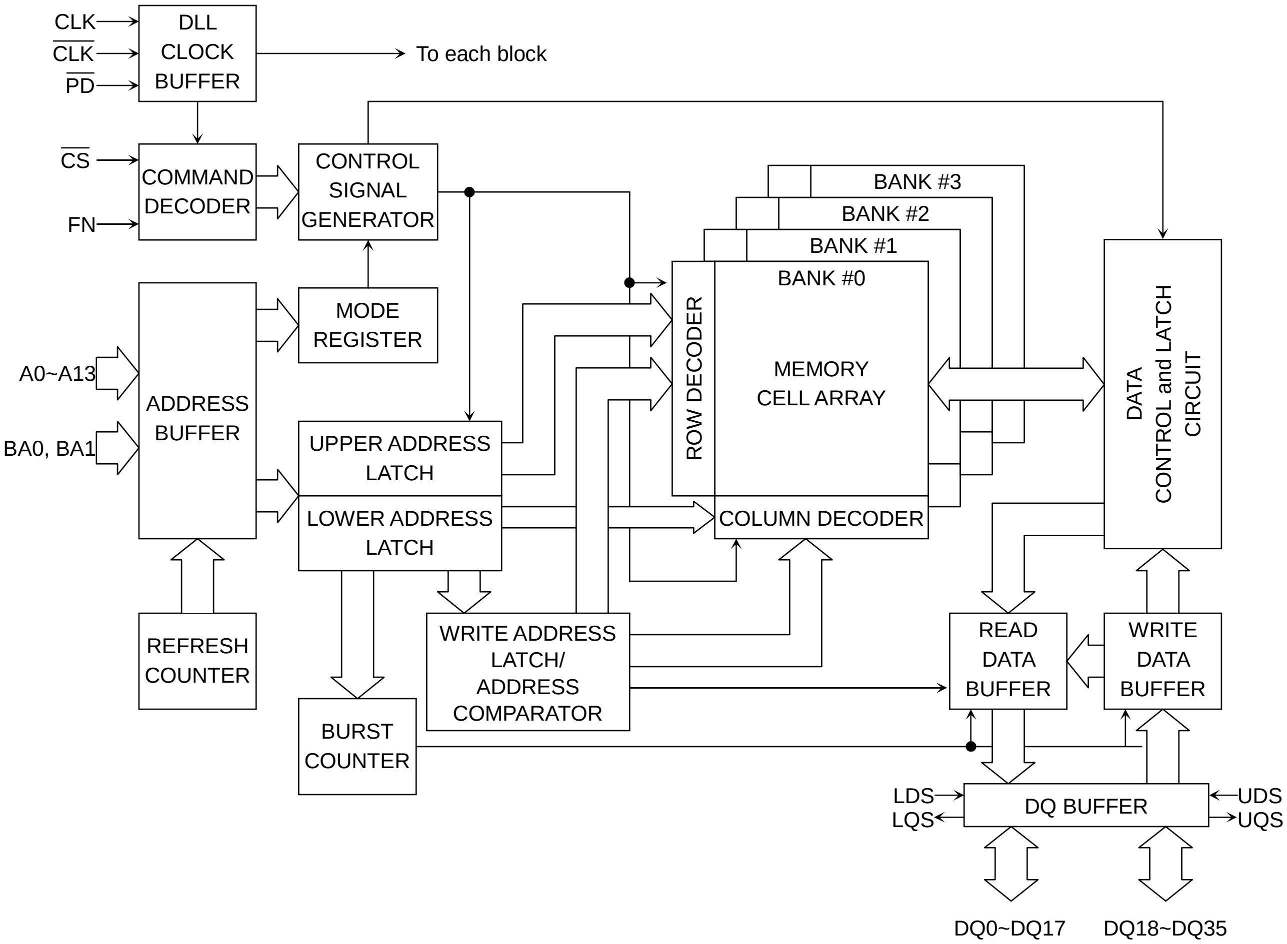
ball pitch=1.0 x 0.8mm

Index; ball pitch 0.8mm (columns) x 1mm (rows)

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{DD}	V_{SS}	V_{SS}	V_{DD}					V_{DD}	V_{SS}	V_{SS}	V_{DD}
B	$V_{DD}Q$	DQ16	DQ17	$V_{DD}Q$					$V_{DD}Q$	DQ0	DQ1	$V_{DD}Q$
C	$V_{SS}Q$	DQ14	DQ15	$V_{SS}Q$					$V_{SS}Q$	DQ2	DQ3	$V_{SS}Q$
D	$V_{DD}Q$	DQ12	DQ13	$V_{DD}Q$					$V_{DD}Q$	DQ4	DQ5	$V_{DD}Q$
E	$V_{SS}Q$	DQ10	DQ11	$V_{SS}Q$					$V_{SS}Q$	DQ6	DQ7	$V_{SS}Q$
F	$V_{DD}Q$	LDS	DQ9	$V_{DD}Q$					$V_{DD}Q$	DQ8	LQS	$V_{DD}Q$
G	$V_{SS}Q$	V_{REF}	$\overline{CLK}$	$V_{SS}Q$					$V_{SS}Q$	A13	FN	$V_{SS}Q$
H	V_{SS}	$\overline{PD}$	CLK	V_{SS}					V_{SS}	$\overline{CS}$	NC	V_{SS}
J	V_{DD}	A12	A11	V_{DD}					V_{DD}	BA1	BA0	V_{DD}
K	V_{SS}	A9	A8	V_{SS}					V_{SS}	A0	A10	V_{SS}
L	V_{DD}	A7	A6	V_{DD}					V_{DD}	A2	A1	V_{DD}
M	$V_{DD}Q$	A5	A4	$V_{DD}Q$					$V_{DD}Q$	NC	A3	$V_{DD}Q$
N	$V_{SS}Q$	UDS	DQ26	$V_{SS}Q$					$V_{SS}Q$	DQ27	UQS	$V_{SS}Q$
P	$V_{DD}Q$	DQ25	DQ24	$V_{DD}Q$					$V_{DD}Q$	DQ29	DQ28	$V_{DD}Q$
R	$V_{SS}Q$	DQ23	DQ22	$V_{SS}Q$					$V_{SS}Q$	DQ31	DQ30	$V_{SS}Q$
T	$V_{DD}Q$	DQ21	DQ20	$V_{DD}Q$					$V_{DD}Q$	DQ33	DQ32	$V_{DD}Q$
U	$V_{SS}Q$	DQ19	DQ18	$V_{SS}Q$					$V_{SS}Q$	DQ35	DQ34	$V_{SS}Q$
V	TMS	TCK	V_{SS}	V_{DD}					V_{DD}	V_{SS}	TDO	TDI

(empty cells) : Depopulated ball

BLOCK DIAGRAM



Note: The TC59LM836DKB configuration is 4 Bank of 16384 × 128 × 36 of cell array with the DQ pins numbered DQ0~DQ35.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT	NOTES
V_{DD}	Power Supply Voltage	−0.3~ 3.3	V	
V_{DDQ}	Power Supply Voltage (for DQ buffer)	$-0.3 \sim V_{DD} + 0.3$	V	
V_{IN}	Input Voltage	$-0.3 \sim V_{DD} + 0.3$	V	
V_{OUT}	Output and DQ pin Voltage	$-0.3 \sim V_{DDQ} + 0.3$	V	
V_{REF}	Input Reference Voltage	$-0.3 \sim V_{DD} + 0.3$	V	
T_{opr}	Operating Temperature (case)	0~85	°C	
T_{stg}	Storage Temperature	−55~150	°C	
T_{solder}	Soldering Temperature (10 s)	260	°C	
P_D	Power Dissipation	2.5	W	
I_{OUT}	Short Circuit Output Current	±50	mA	

Caution: Conditions outside the limits listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.
Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may affect device reliability.

RECOMMENDED DC, AC OPERATING CONDITIONS (Notes: 1)(T_{CASE} = 0~85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.375	2.5	2.625	V	
V_{DDQ}	Power Supply Voltage (for DQ buffer)	1.4	—	1.9	V	
V_{REF}	Reference Voltage	$V_{DDQ}/2 \times 95\%$	$V_{DDQ}/2$	$V_{DDQ}/2 \times 105\%$	V	2
V_{IH} (DC)	Input DC High Voltage	$V_{REF} + 0.125$	—	$V_{DDQ} + 0.2$	V	5
V_{IL} (DC)	Input DC Low Voltage	−0.1	—	$V_{REF} - 0.125$	V	5
V_{ICK} (DC)	Differential Clock DC Input Voltage	−0.1	—	$V_{DDQ} + 0.1$	V	10
V_{ID} (DC)	Differential Input Voltage. CLK and $\overline{CLK}$ inputs (DC)	0.4	—	$V_{DDQ} + 0.2$	V	7, 10
V_{IH} (AC)	Input AC High Voltage	$V_{REF} + 0.2$	—	$V_{DDQ} + 0.2$	V	3, 6
V_{IL} (AC)	Input AC Low Voltage	−0.1	—	$V_{REF} - 0.2$	V	4, 6
V_{ID} (AC)	Differential Input Voltage. CLK and $\overline{CLK}$ inputs (AC)	0.55	—	$V_{DDQ} + 0.2$	V	7, 10
V_X (AC)	Differential AC Input Cross Point Voltage	$V_{DDQ}/2 - 0.125$	—	$V_{DDQ}/2 + 0.125$	V	8, 10
V_{ISO} (AC)	Differential Clock AC Middle Level	$V_{DDQ}/2 - 0.125$	—	$V_{DDQ}/2 + 0.125$	V	9, 10

NOTES:

(1) All voltages referenced to V_{SS}, V_{SSQ}.

(2) V_{REF} is expected to track variations in V_{DDQ} DC level of the transmitting device.
Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).

(3) Overshoot limit: $V_{IH\ (max)} = V_{DDQ} + 0.7$ V with a pulse width ≤ 5 ns.

(4) Undershoot limit: $V_{IL\ (min)} = -0.7$ V with a pulse width ≤ 5 ns.

(5) V_{IH} (DC) and V_{IL} (DC) are levels to maintain the current logic state.

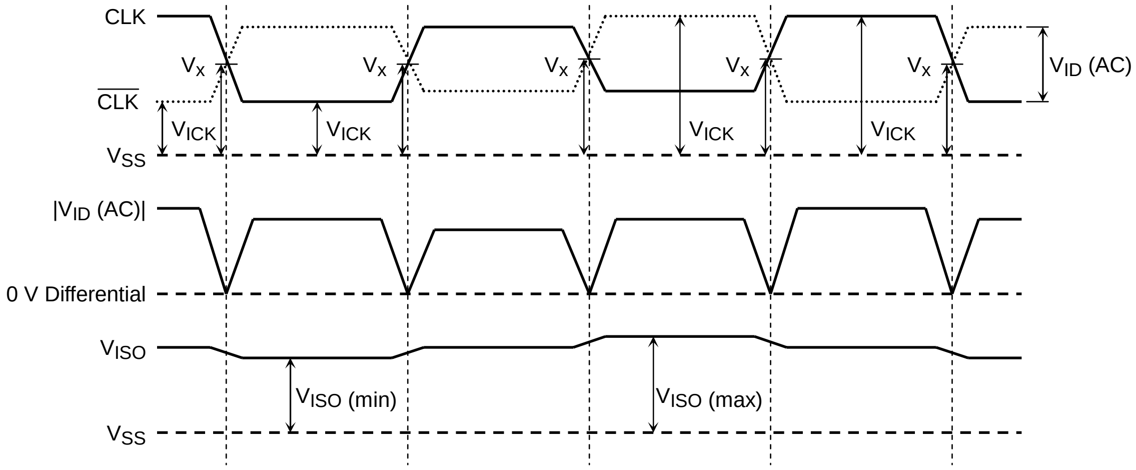
(6) V_{IH} (AC) and V_{IL} (AC) are levels to change to the new logic state.

(7) V_{ID} is differential voltage of CLK input level and $\overline{CLK}$ input level.

(8) The value of V_X (AC) is expected to equal $V_{DDQ}/2$ of the transmitting device.

(9) V_{ISO} means {V_{ICK} (CLK) + V_{ICK} ($\overline{CLK}$)} /2

(10) Refer to the figure below.



(11) In the case of external termination, VTT (termination voltage) should be gone in the range of V_{REF} (DC) ± 0.04 V.

CAPACITANCE (V_{DD} = 2.5V, V_{DDQ} = 1.8 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	Delta	UNIT
C_{IN}	Input pin Capacitance	1.5	3.0	0.25	pF
C_{INC}	Clock pin (CLK, $\overline{CLK}$) Capacitance	1.5	3.0	0.25	pF
$C_{I/O}$	DQ, LDS, UDS, LQS, UQS Capacitance	2.5	3.5	0.5	pF
C_{NC}	NC pin Capacitance	—	1.5	—	pF

Note: These parameters are periodically sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = 2.5 V ± 0.125 V, V_{DDQ} = 1.4 V ~ 1.9 V, T_{CASE} = 0 ~ 85°C)

SYMBOL	PARAMETER	MAX			UNIT	NOTES
		-30	-33	-40		
I_{DD1S}	Operating Current One bank read or write operation ; t_{CK} = min; I_{RC} = min, I_{OUT} = 0mA ; Burst Length = 4, CAS Latency = 6, Free running QS mode ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ}, Address inputs change up to 2 times during minimum I_{RC}, Read data change twice per clock cycle	380	360	340	mA	1, 2
I_{DD2N}	Standby Current All banks: inactive state ; t_{CK} = min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IH} ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Other input signals change one time during 4 × t_{CK}, DQ and DS inputs change twice per clock cycle	120	110	100	mA	1, 2
I_{DD2P}	Standby (power down) Current All banks: inactive state ; t_{CK} = min, $\overline{PD}$ = V_{IL} (power down) ; CAS Latency = 6, Free running QS mode ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Other input signals change one time during 4 × t_{CK}, DQ and DS inputs are floating (V_{DDQ}/2)	100	95	90	mA	1, 2
I_{DD4W}	Write Operating Current (4Banks) 4 Bank interleaved continuous burst write operation ; t_{CK} = min, I_{RC} = min ; Burst Length = 4, CAS Latency = 6, Free running QS mode ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Address inputs change once per clock cycle, DQ and DS inputs change twice per clock cycle	850	800	750	mA	1, 2
I_{DD4R}	Read Operating Current (4Banks) 4 Bank interleaved continuous burst read operation ; t_{CK} = min, I_{RC} = min, I_{OUT} = 0mA ; Burst Length = 4, CAS Latency = 6, Free running QS mode ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Address inputs change once per clock cycle, Read data change twice per clock cycle	850	800	750	mA	1, 2
I_{DD5B}	Burst Auto Refresh Current Refresh command at every I_{REFC} interval ; t_{CK} = min; I_{REFC} = min ; CAS Latency = 6, Free running QS mode ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ}, Address inputs change up to 2 times during minimum I_{REFC}, DQ and DS inputs change twice per clock cycle	380	360	340	mA	1, 2, 3
I_{DD6}	Self-Refresh Current $\overline{PD}$ = 0.2 V ; Other input signals are floating (V_{DDQ}/2), DQ and DS inputs are floating (V_{DDQ}/2)	15	15	15	mA	2

Notes: 1. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK}, t_{RC} and I_{RC}.
2. These parameters define the current between V_{DD} and V_{SS}.
3. I_{DD5B} is specified under burst refresh condition. Actual system should use distributed refresh that meet to t_{REFI} specification.

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = 2.5 V ± 0.125 V, V_{DDQ} = 1.4 V ~ 1.9 V, T_{CASE} = 0 ~ 85°C)

SYMBOL	PARAMETER			MIN	MAX	UNIT	NOTES
I_{LI}	Input Leakage Current (0 V ≤ V_{IN} ≤ V_{DDQ}, all other pins not under test = 0 V)			−5	5	μA	
I_{LO}	Output Leakage Current (Output disabled, 0 V ≤ V_{OUT} ≤ V_{DDQ})			−5	5	μA	
I_{REF}	V_{REF} Current			−5	5	μA	
I_{OH} (DC)	Normal Output Driver	Output DC Current (V_{DDQ} = 1.7V~1.9V)	V_{OH} = 1.420 V	−5.6	—	mA	1
I_{OL} (DC)			V_{OL} = 0.280 V	5.6	—		
I_{OH} (DC)	Strong Output Driver		V_{OH} = 1.420 V	−9.8	—		
I_{OL} (DC)			V_{OL} = 0.280 V	9.8	—		
I_{OH} (DC)	Weak Output Driver		V_{OH} = 1.420 V	−2.8	—		
I_{OL} (DC)			V_{OL} = 0.280 V	2.8			
I_{OH} (DC)	Normal Output Driver	Output DC Current (V_{DDQ} = 1.4V~1.6V)	V_{OH} = V_{DDQ} – 0.4V	−4	—	mA	1
I_{OL} (DC)			V_{OL} = 0.4V	4	—		
I_{OH} (DC)	Strong Output Driver		V_{OH} = V_{DDQ} – 0.4V	−8	—		
I_{OL} (DC)			V_{OL}= 0.4V	8	—		
I_{OH} (DC)	Weak Output Driver		Not defined	—	—		
I_{OL} (DC)			Not defined	—	—		

Notes: 1. Refer to output driver characteristics for the detail. Output Driver Strength is selected by Extended Mode Register.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 1, 2)
(V_{DD} = 2.5 ± 0.125V, V_{DDQ} = 1.4 ~ 1.9V, T_{CASE} = 0 ~ 85°C)

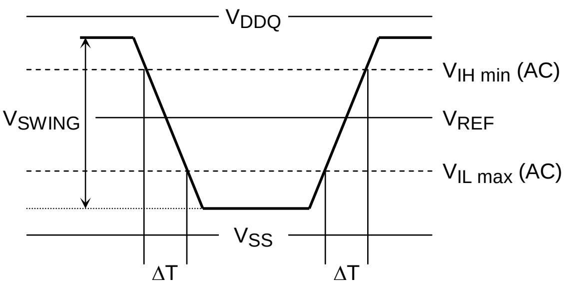
SYMBOL	PARAMETER		-30 MIN	-30 MAX	-33 MIN	-33 MAX	-40 MIN	-40 MAX	UNIT	NOTES
t_{RC}	Random Cycle Time		20.0	—	22.5	—	25	—	ns	3
t_{CK}	Clock Cycle Time	C_L = 4	4.0	5.0	4.5	7.5	5.0	7.5	ns	3
		C_L = 5	3.5	5.0	3.75	7.5	4.5	7.5	ns	3
		C_L = 6	3.0	5.0	3.33	7.5	4.0	7.5	ns	3
t_{RAC}	Random Access Time		—	20.0	—	22.5	—	25	ns	3
t_{CH}	Clock High Time		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—	ns	3
t_{CL}	Clock Low Time		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—	ns	3
t_{CKQS}	QS Access Time from CLK		–0.45	0.45	–0.45	0.45	–0.5	0.5	ns	3, 8,10
t_{QSQ}	Data Output Skew from QS		—	0.2	—	0.25	—	0.3	ns	
t_{QSQA}	Data Output Skew from QS to All DQ		—	0.3	—	0.35	—	0.4	ns	
t_{AC}	Data Access Time from CLK		–0.5	0.5	–0.5	0. 5	–0.6	0.6	ns	3, 8,10
t_{OH}	Data Output Hold Time from CLK		–0.5	0.5	–0.5	0.5	–0.6	0.6	ns	3, 8
t_{HP}	CLK half period (minimum of Actual t_{CH}, t_{CL})		min(t_{CH}, t_{CL})	—	min(t_{CH}, t_{CL})	—	min(t_{CH}, t_{CL})	—	ns	3
t_{QSP}	QS (read) Pulse Width		t_{HP}– t_{QHS}	—	t_{HP}– t_{QHS}	—	t_{HP}– t_{QHS}	—	ns	4, 8
t_{QSQV}	Data Output Valid Time from QS		t_{HP}– t_{QHS}	—	t_{HP}– t_{QHS}	—	t_{HP}– t_{QHS}	—	ns	4, 8
t_{QHS}	DQ, QS Hold Skew factor		—	$0.055 \times t_{CK} + 0.17$	—	$0.055 \times t_{CK} + 0.17$	—	$0.055 \times t_{CK} + 0.17$	ns	
t_{DQSS}	DS (write) Low to High Setup Time		$0.8 \times t_{CK}$	$1.2 \times t_{CK}$	$0.8 \times t_{CK}$	$1.2 \times t_{CK}$	$0.8 \times t_{CK}$	$1.2 \times t_{CK}$	ns	3
t_{DSPRE}	DS (write) Preamble Pulse Width		$0.4 \times t_{CK}$	—	$0.4 \times t_{CK}$	—	$0.4 \times t_{CK}$	—	ns	4
t_{DSPRES}	DS First Input Setup Time		0	—	0	—	0	—	ns	3
t_{DSPREH}	DS First Low Input Hold Time		$0.3 \times t_{CK}$	—	$0.3 \times t_{CK}$	—	$0.3 \times t_{CK}$	—	ns	3
t_{DSP}	DS High or Low Input Pulse Width		$0.45 \times t_{CK}$	$0.55 \times t_{CK}$	$0.45 \times t_{CK}$	$0.55 \times t_{CK}$	$0.45 \times t_{CK}$	$0.55 \times t_{CK}$	ns	4
t_{DSS}	DS Input Falling Edge to Clock Setup Time	C_L = 4	0.75	—	0.8	—	1.0	—	ns	3, 4
		C_L = 5	0.75	—	0.8	—	1.0	—	ns	3, 4
		C_L = 6	0.75	—	0.8	—	1.0	—	ns	3, 4
t_{DSPST}	DS (write) Postamble Pulse Width		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—	ns	4
t_{DSPSTH}	DS (write) Postamble Hold Time	C_L = 4	0.75	—	0.8	—	1.0	—	ns	3, 4
		C_L = 5	0.75	—	0.8	—	1.0	—	ns	3, 4
		C_L = 6	0.75	—	0.8	—	1.0	—	ns	3, 4
t_{DSSK}	UDS – LDS Skew		$-0.4 \times t_{CK}$	$0.4 \times t_{CK}$	$-0.4 \times t_{CK}$	$0.4 \times t_{CK}$	$-0.4 \times t_{CK}$	$0.4 \times t_{CK}$	ns	
t_{DS}	Data Input Setup Time from DS		0.3	—	0.35	—	0.4	—	ns	4, 11
t_{DH}	Data Input Hold Time from DS		0.3	—	0.35	—	0.4	—	ns	4, 11
t_{IS}	Command/Address Input Setup Time		0.6	—	0.6	—	0.7	—	ns	3
t_{IH}	Command/Address Input Hold Time		0.6	—	0.6	—	0.7	—	ns	3

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 1, 2) (continued)

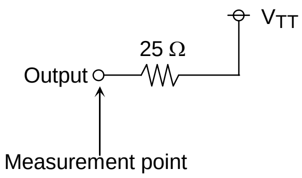
SYMBOL	PARAMETER		-30		-33		-40		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{LZ}	Data-out Low Impedance Time from CLK		–0.5	—	–0.5	—	–0.6	—	ns	3, 6, 8
t_{HZ}	Data-out High Impedance Time from CLK		—	0.5	—	0.5	—	0.6	ns	3, 7, 8
t_{QPDH}	Last output to $\overline{PD}$ High Hold Time		0	—	0	—	0	—	ns	
t_{PDEX}	Power Down Exit Time		0.6	—	0.6	—	0.7	—	ns	3
t_T	Input Transition Time		0.1	1	0.1	1	0.1	1	ns	
t_{FPDL}	$\overline{PD}$ Low Input Window for Self-Refresh Entry		$-0.5 \times t_{CK}$	5	$-0.5 \times t_{CK}$	5	$-0.5 \times t_{CK}$	5	ns	3
t_{REFI}	Auto-Refresh Average Interval		0.4	3.9	0.4	3.9	0.4	3.9	µs	5
t_{PAUSE}	Pause Time after Power-up		200	—	200	—	200	—	µs	
l_{RC}	Random Read/Write Cycle Time (applicable to same bank)	$C_L = 4$	5	—	5	—	5	—	cycle	
		$C_L = 5$	6	—	6	—	6	—	cycle	
		$C_L = 6$	7	—	7	—	7	—	cycle	
l_{RCD}	RDA/WRA to LAL Command Input Delay (applicable to same bank)		1	1	1	1	1	1	cycle	
l_{RAS}	LAL to RDA/WRA Command Input Delay (applicable to same bank)	$C_L = 4$	4	—	4	—	4	—	cycle	
		$C_L = 5$	5	—	5	—	5	—	cycle	
		$C_L = 6$	6	—	6	—	6	—	cycle	
l_{RBD}	Random Bank Access Delay (applicable to other bank)		2	—	2	—	2	—	cycle	
l_{RWD}	LAL following RDA to WRA Delay (applicable to other bank)	$B_L = 2$	2	—	2	—	2	—	cycle	
		$B_L = 4$	3	—	3	—	3	—	cycle	
l_{WRD}	LAL following WRA to RDA Delay (applicable to other bank)		1	—	1	—	1	—	cycle	
l_{RSC}	Mode Register Set Cycle Time	$C_L = 4$	7	—	7	—	7	—	cycle	
		$C_L = 5$	7	—	7	—	7	—	cycle	
		$C_L = 6$	7	—	7	—	7	—	cycle	
l_{PD}	$\overline{PD}$ Low to Inactive State of Input Buffer		—	2	—	2	—	2	cycle	
l_{PDA}	$\overline{PD}$ High to Active State of Input Buffer		1	—	1	—	1	—	cycle	
l_{PDV}	Power down mode valid from REF command	$C_L = 4$	19	—	19	—	19	—	cycle	
		$C_L = 5$	23	—	23	—	23	—	cycle	
		$C_L = 6$	25	—	25	—	25	—	cycle	
l_{REFC}	Auto-Refresh Cycle Time	$C_L = 4$	19	—	19	—	19	—	cycle	
		$C_L = 5$	23	—	23	—	23	—	cycle	
		$C_L = 6$	25	—	25	—	25	—	cycle	
l_{CKD}	REF Command to Clock Input Disable at Self-Refresh Entry		l_{REFC}	—	l_{REFC}	—	l_{REFC}	—	cycle	
l_{LOCK}	DLL Lock-on Time (applicable to RDA command)		200	—	200	—	200	—	cycle	

AC TEST CONDITIONS

SYMBOL	PARAMETER	VALUE	UNIT	NOTES
$V_{IH\ (min)}$	Input High Voltage (minimum)	V_{REF} + 0.2	V	
$V_{IL\ (max)}$	Input Low Voltage (maximum)	V_{REF} − 0.2	V	
V_{REF}	Input Reference Voltage	V_{DDQ}/2	V	
V_{TT}	Termination Voltage	V_{REF}	V	
V_{SWING}	Input Signal Peak to Peak Swing	0.8	V	
Vr	Differential Clock Input Reference Level	V_X (AC)	V	
V_{ID} (AC)	Input Differential Voltage	1.0	V	
SLEW	Input Signal Minimum Slew Rate	2.5	V/ns	
V_{OTR}	Output Timing Measurement Reference Voltage	V_{DDQ}/2	V	9



SLEW = ($V_{IH\ min}$ (AC) − $V_{IL\ max}$ (AC))/ΔT



AC Test Load

NOTES:

(1) Transition times are measured between $V_{IH\ min}$ (DC) and $V_{IL\ max}$ (DC).
Transition (rise and fall) of input signals have a fixed slope.

(2) If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., t_{DQSS} = 0.8 × t_{CK}, t_{CK} = 3.3 ns, 0.8 × 3.3 ns = 2.64 ns is rounded up to 2.7 ns.)

(3) These parameters are measured from the differential clock (CLK and $\overline{CLK}$) AC cross point.

(4) These parameters are measured from signal transition point of DS crossing V_{REF} level.

(5) The $t_{REFI\ (max)}$ applies to equally distributed refresh method.
The $t_{REFI\ (min)}$ applies to both burst refresh method and distributed refresh method.
In such case, the average interval of eight consecutive Auto-Refresh commands has to be more than 400 ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 μs (8 × 400 ns) is to 8 times in the maximum.

(6) Low Impedance State is specified at V_{DDQ}/2 ± 0.1 V from steady state.

(7) High Impedance State is specified where output buffer is no longer driven.

(8) These parameters depend on the clock jitter. These parameters are measured at stable clock.

(9) Output timing is measured by using Normal driver strength at V_{DDQ} = 1.7 V ~ 1.9 V.
Output timing is measured by using Strong driver strength at V_{DDQ} = 1.4 V~1.6 V.

(10) These parameters are measured at t_{CK} = minimum ~ 6.0ns. When t_{CK} is longer than 6.0ns, these parameters are specified as below for all speed version.
t_{CKQS} (MIN/MAX) = −0.6ns / 0.6ns, t_{AC} (MIN/MAX) = −0.65ns / 0.65ns

(11) These parameters are measured at V_{DDQ} = 1.7 V~1.9 V. Both t_{DS} and t_{DH} at V_{DDQ} = 1.4 V~1.6 V are specified as below for all speed version.
t_{DS} (MIN) = 0.4 ns , t_{DH} (MIN) = 0.4 ns

POWER UP SEQUENCE

(1) As for $\overline{PD}$, being maintained by the low state (≤ 0.2 V) is desirable before a power-supply injection.

(2) Apply V_{DD} before or at the same time as V_{DDQ}.

(3) Apply V_{DDQ} before or at the same time as V_{REF}.

(4) Start clock (CLK, $\overline{CLK}$) and maintain stable condition for 200 μs (min).

(5) After stable power and clock, apply DESL and take $\overline{PD}$ =H.

(6) Issue EMRS to enable DLL and to define driver strength and data strobe type. (Note: 1)

(7) Issue MRS for set $\overline{CAS}$ latency (CL), Burst Type (BT), and Burst Length (BL). (Note: 1)

(8) Issue two or more Auto-Refresh commands (Note: 1).

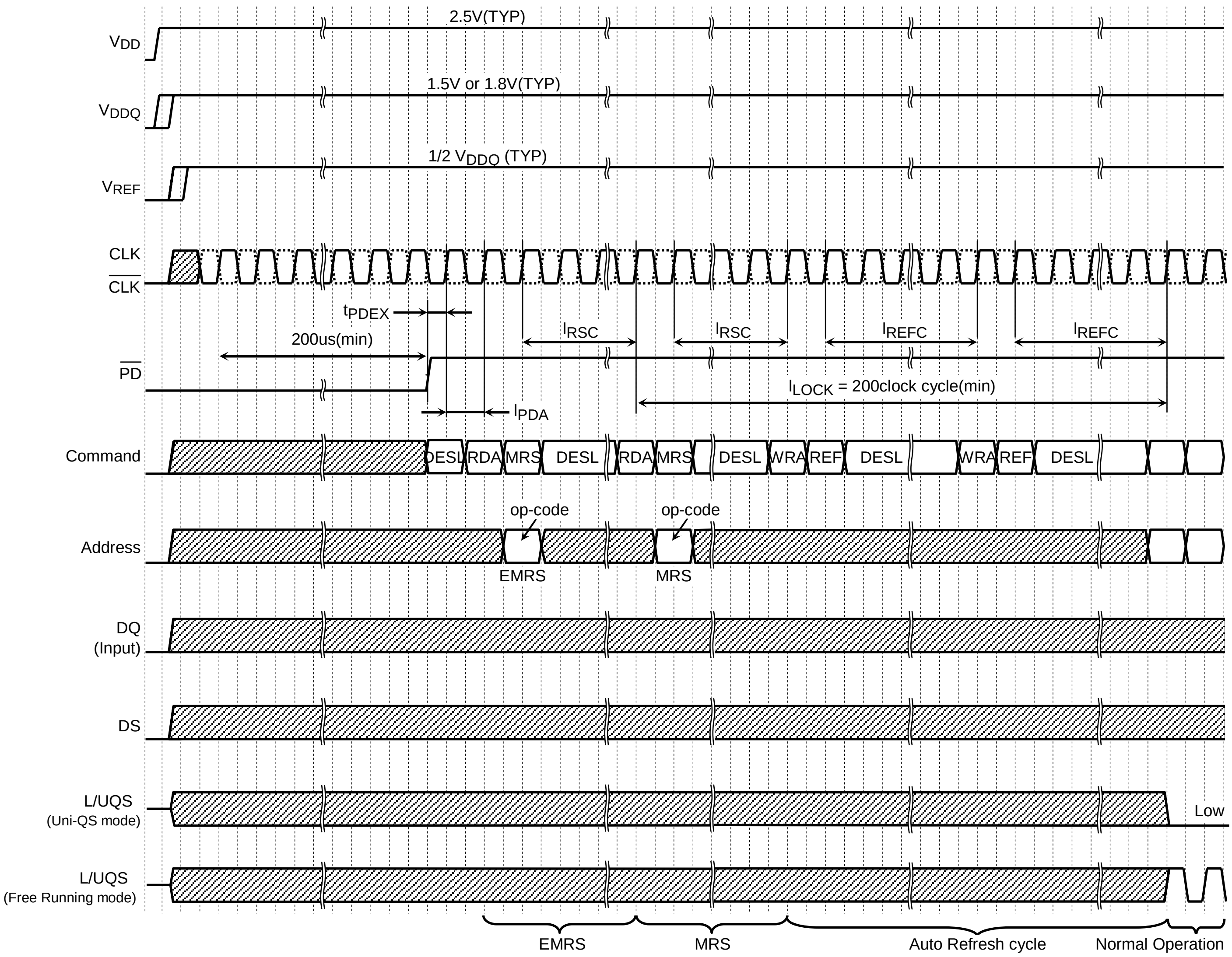
(9) Ready for normal operation after 200 clocks from Extended Mode Register programming.

NOTES:

(1) Sequence 6, 7 and 8 can be issued in random order.

(2) L = Logic Low, H = Logic High

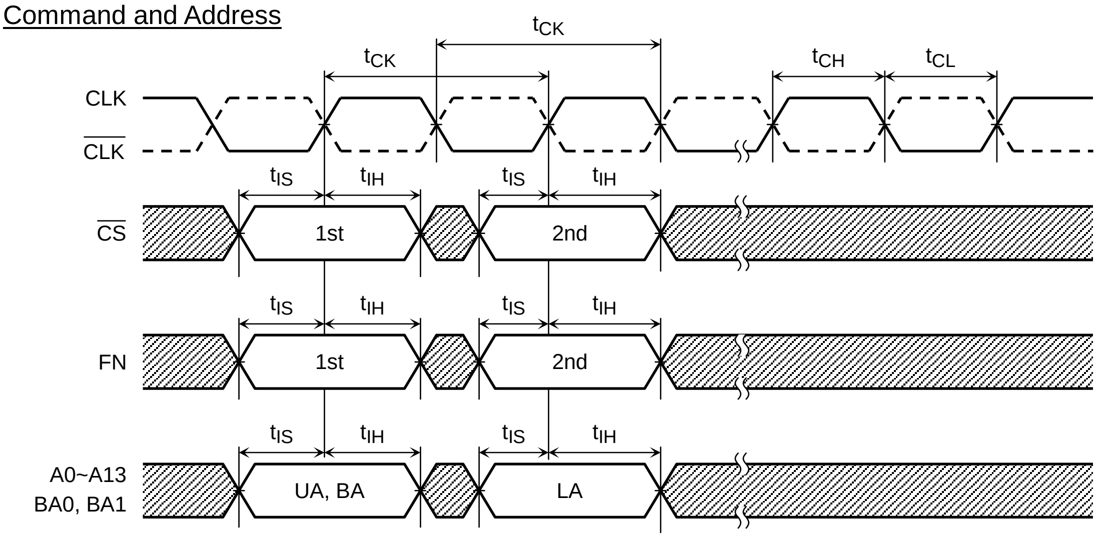
(3) DQ output is Hi-Z state during power upsequence.



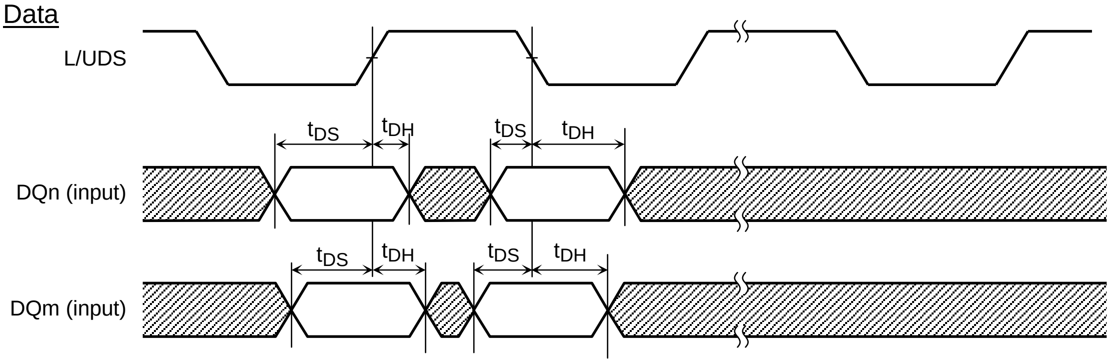
TIMING DIAGRAMS

Input Timing

Command and Address

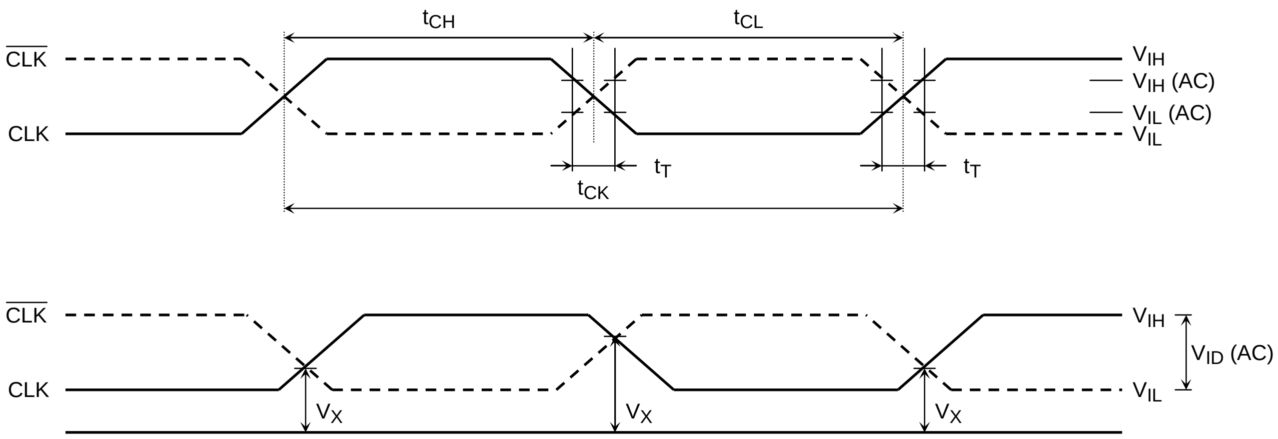


Data



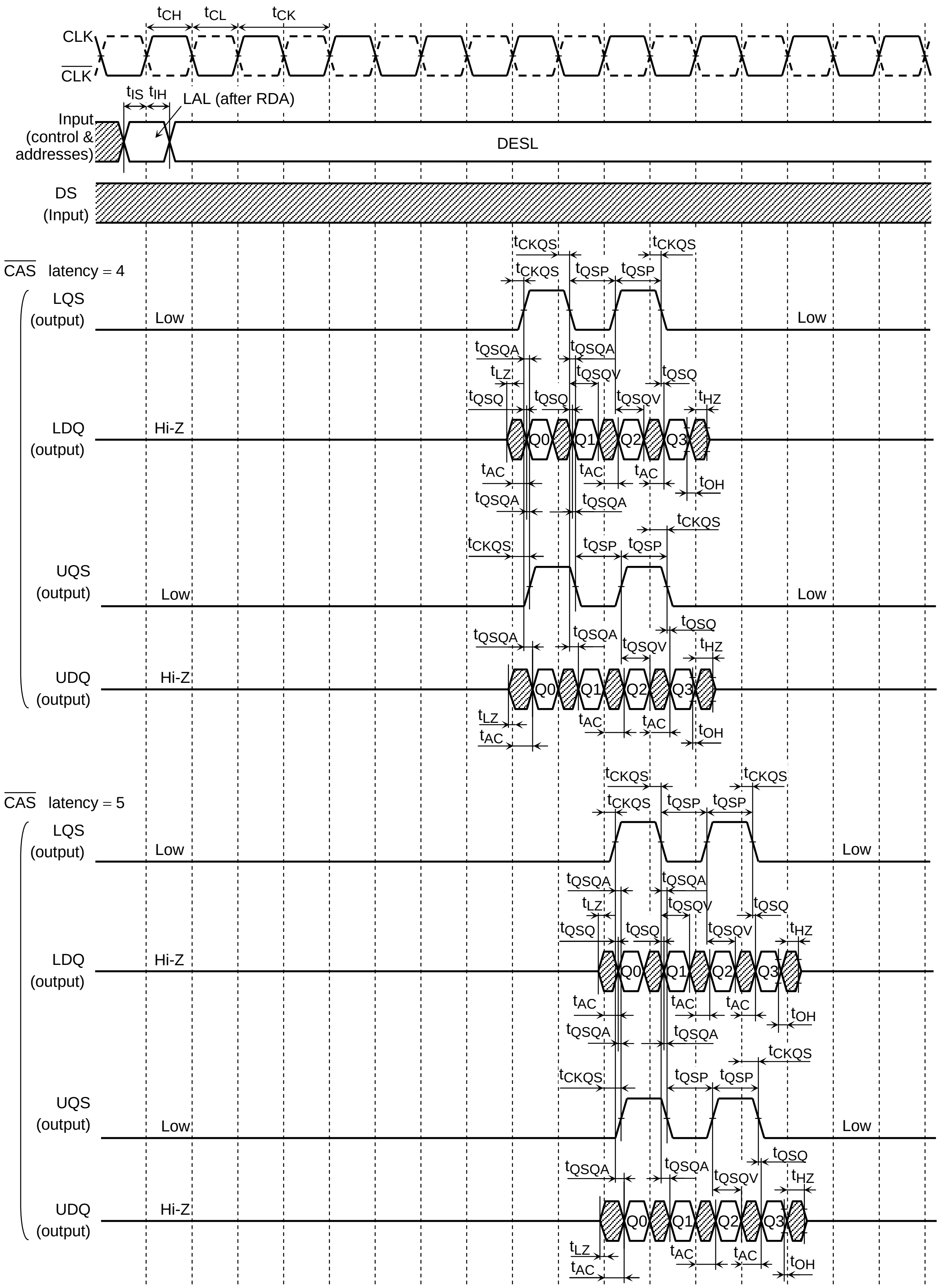
Refer to the Command Truth Table.

Timing of the CLK, $\overline{\text{CLK}}$



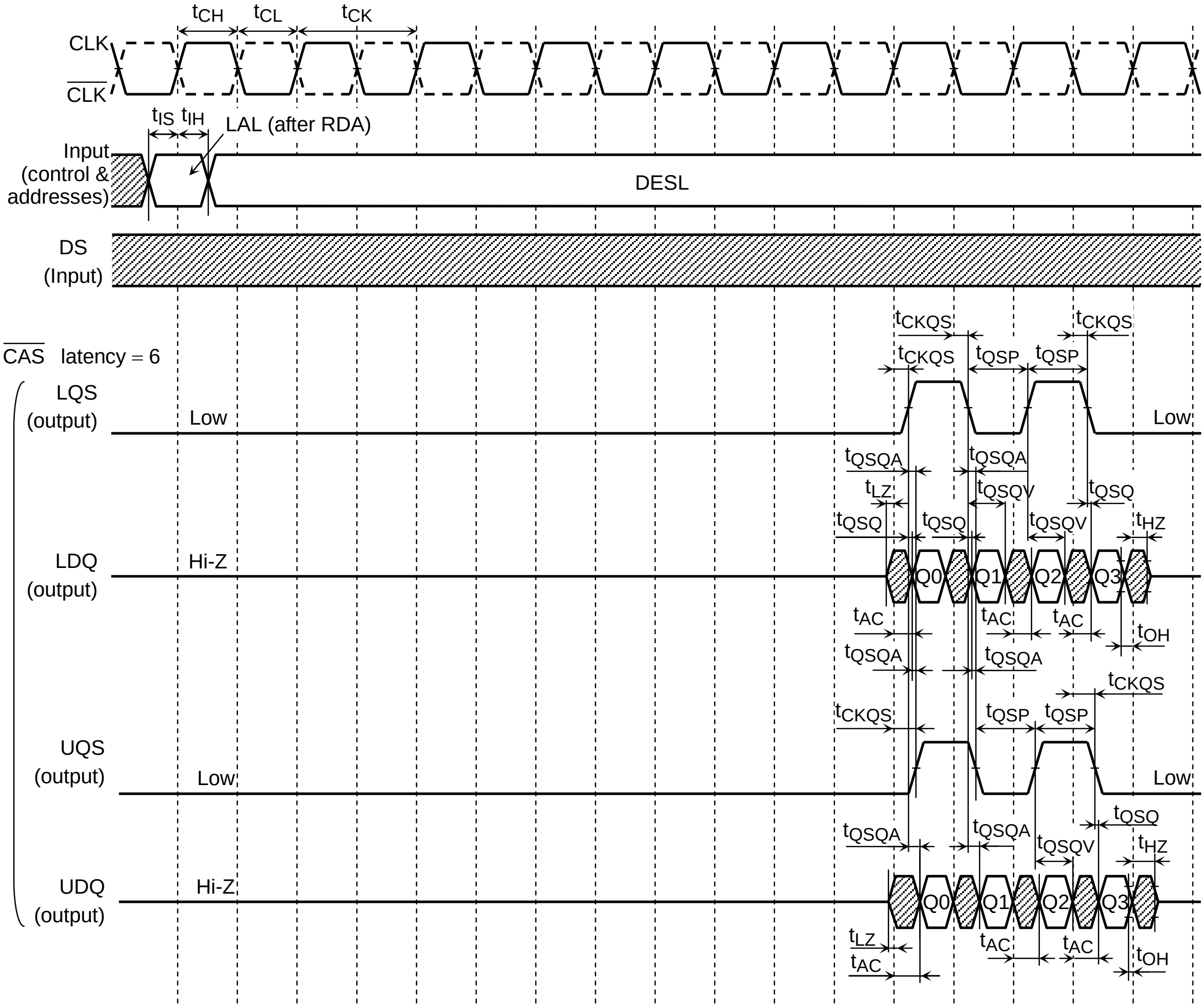
Read Timing (Burst Length = 4)

Unidirectional DS/QS mode



Read Timing (Burst Length = 4)

Unidirectional DS/QS mode

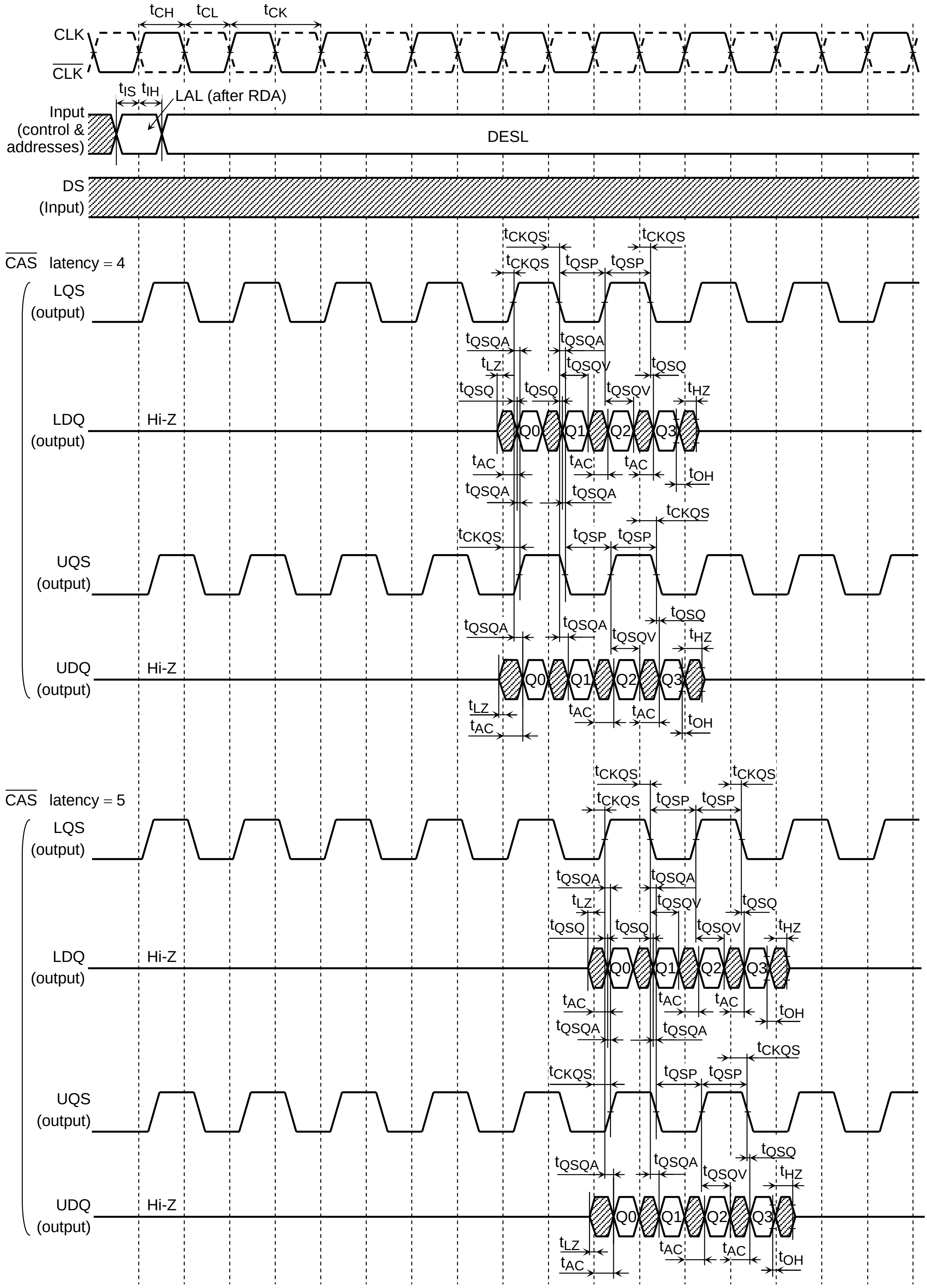


Note: DQ0 to DQ35 are aligned with QS.
The correspondence of LQS, UQS to DQ.

LQS	DQ0~DQ17
UQS	DQ18~DQ35

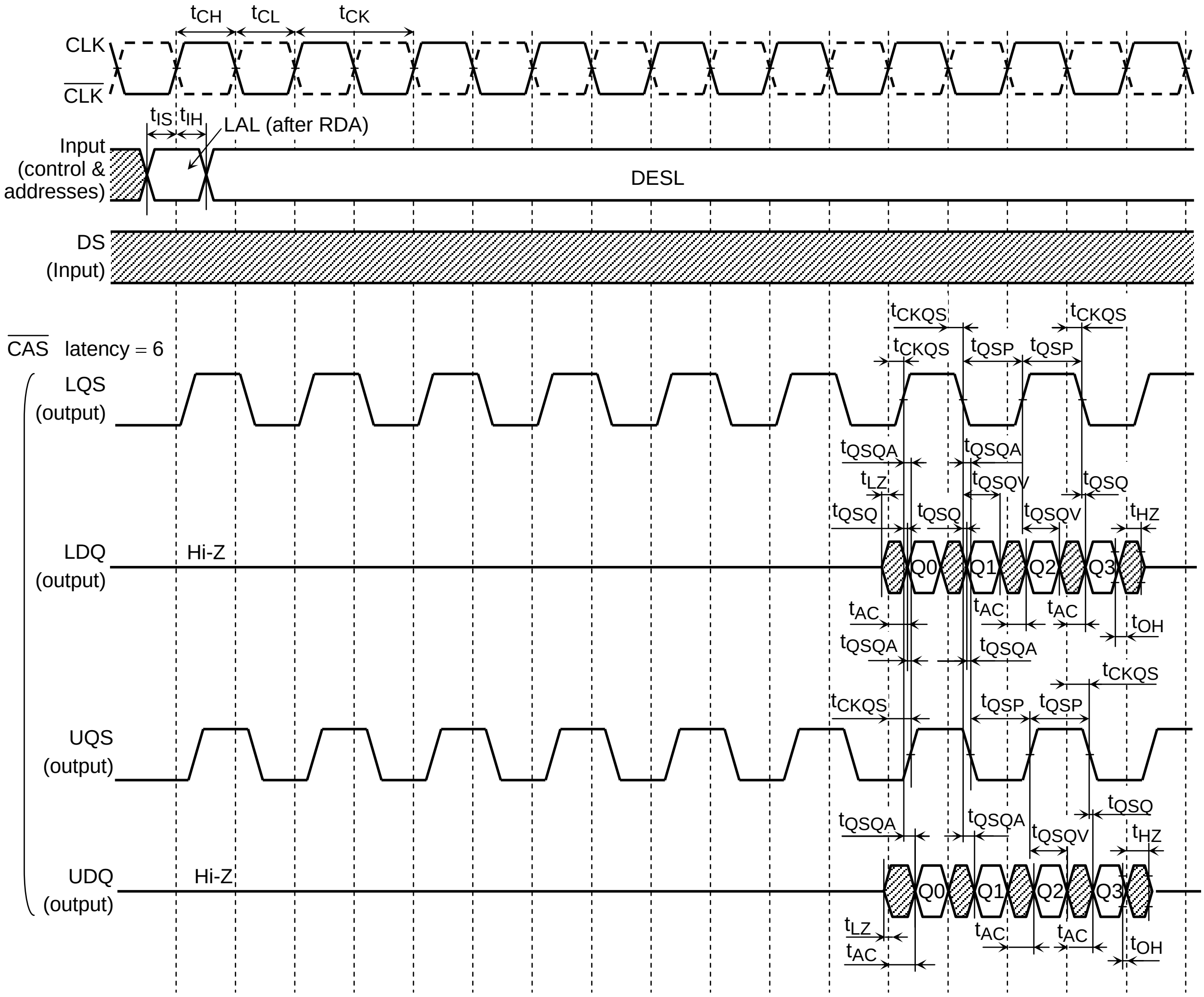
Read Timing (Burst Length = 4)

Unidirectional DS/Free Running QS mode



Read Timing (Burst Length = 4)

Unidirectional DS/Free Running QS mode

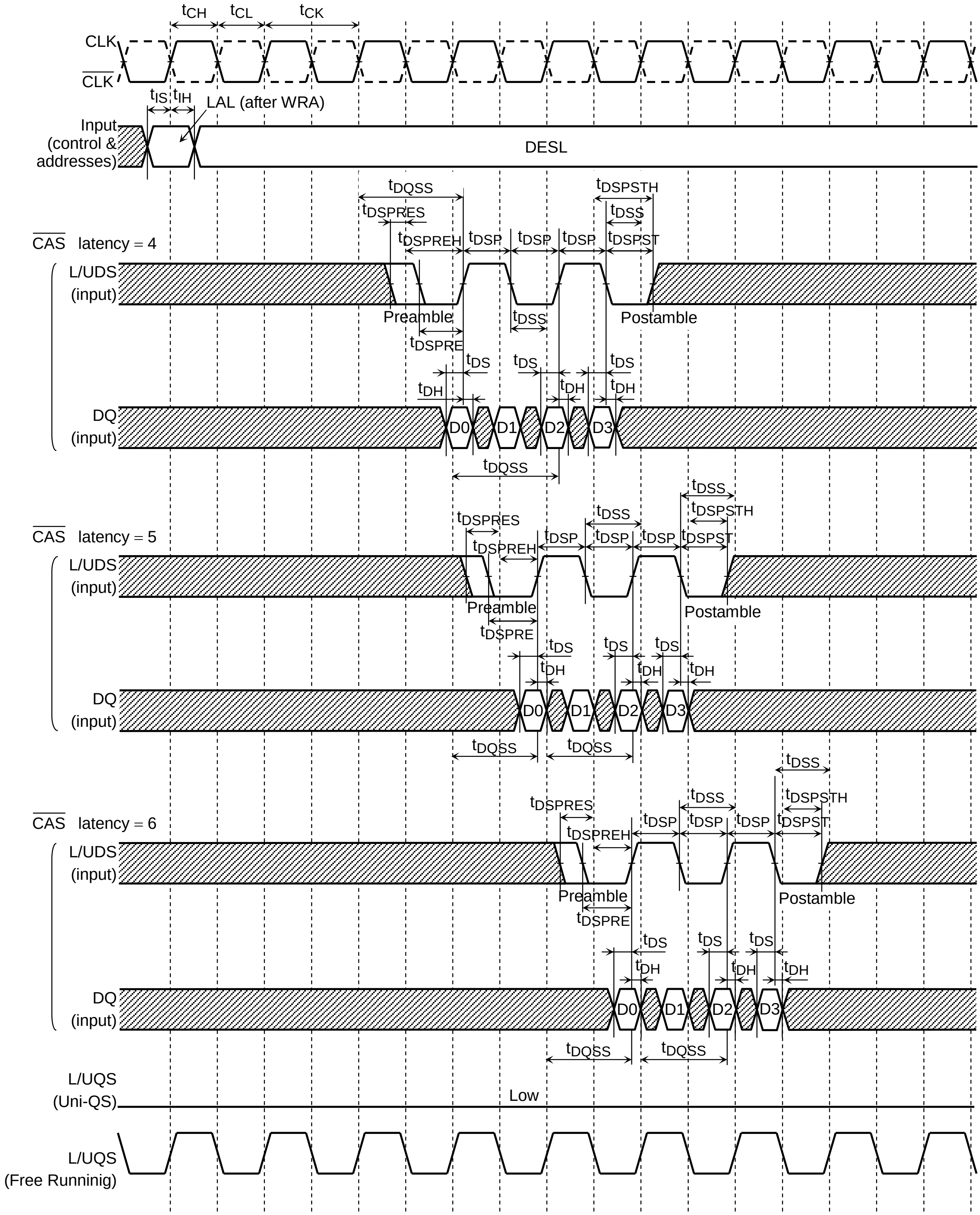


Note: DQ0 to DQ35 are aligned with QS.
The correspondence of LQS, UQS to DQ.

LQS	DQ0~DQ17
UQS	DQ18~DQ35

Write Timing (Burst Length = 4)

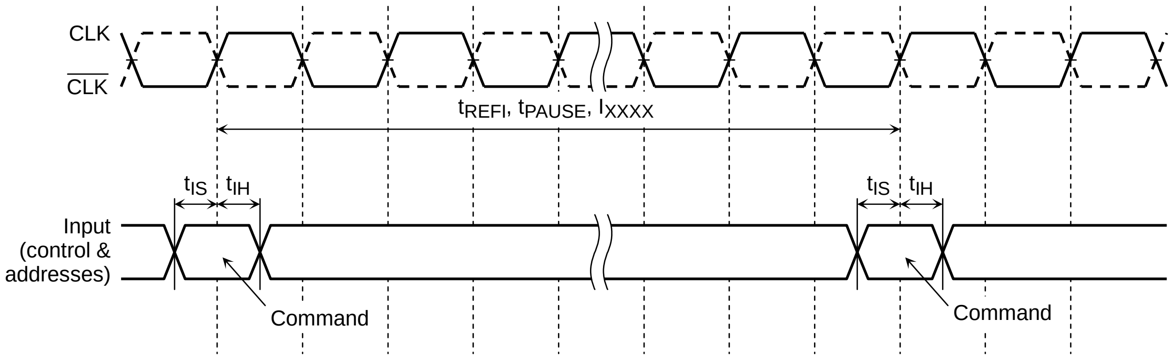
Unidirectional DS/QS mode, Unidirectional DS/Free Running QS mode



Note: DQ0 to DQ35 are sampled at both edges of DS.
The correspondence of LDS, UDS to DQ.

LDS	DQ0~DQ17
UDS	DQ18~DQ35

t_{REFI}, t_{PAUSE}, I_{XXXX} Timing



Note: “I_{XXXX}” means “I_{RC}”, “I_{RCD}”, “I_{RAS}”, etc.

FUNCTION TRUTH TABLE (Notes: 1, 2, 3)

Command Truth Table (Notes: 4)

• The First Command

SYMBOL	FUNCTION	$\overline{CS}$	FN	BA1~BA0	A13~A10	A9~A8	A7	A6~A0
DESL	Device Deselect	H	×	×	×	×	×	×
RDA	Read with Auto-close	L	H	BA	UA	UA	UA	UA
WRA	Write with Auto-close	L	L	BA	UA	UA	UA	UA

• The Second Command (The next clock of RDA or WRA command)

SYMBOL	FUNCTION	$\overline{CS}$	FN	BA1~ BA0	A13~ A12	A11~ A10	A9	A8	A7	A6~A0
LAL	Lower Address Latch	H	×	×	V	×	×	×	×	LA
REF	Auto-Refresh	L	×	×	×	×	×	×	×	×
MRS	Mode Register Set	L	×	V	L	L	L	L	V	V

Notes: 1. L = Logic Low, H = Logic High, × = either L or H, V = Valid (specified value), BA = Bank Address, UA = Upper Address, LA = Lower Address
2. All commands are assumed to issue at a valid state.
3. All inputs for command (excluding SELFX and PDEX) are latched on the crossing point of differential clock input where CLK goes to High.
4. Operation mode is decided by the combination of 1st command and 2nd command. Refer to "STATE DIAGRAM" and the command table below.

Read Command Table

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA1~BA0	A13~A10	A9~A8	A7	A6~A0	NOTES
RDA (1st)	L	H	BA	UA	UA	UA	UA	
LAL (2nd)	H	×	×	×	×	×	LA	

Write Command Table

COMMAND(SYMBOL)	$\overline{CS}$	FN	BA1~BA0	A13	A12	A11	A10	A9~A8	A7	A6~A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	×	×	VW0	VW1	×	×	×	×	LA

Notes: 5. A13~ A12 are used for Variable Write Length (VW) control at Write Operation.

VW Truth Table

Burst Length	Function	VW0	VW1
BL=2	Write All Words	L	×
	Write First One Word	H	×
BL=4	Reserved	L	L
	Write All Words	H	L
	Write First Two Words	L	H
	Write First One Word	H	H

FUNCTION TRUTH TABLE (continued)

Mode Register Set Command Table

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA1~BA0	A13~A9	A8	A7	A6~A0	NOTES
RDA (1st)	L	H	×	×	×	×	×	
MRS (2nd)	L	×	V	V	V	V	V	6

Notes: 6. Refer to "MODE REGISTER TABLE".

Auto-Refresh Command Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA1~BA0	A13~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Active	WRA (1st)	Standby	H	H	L	L	×	×	×	×	×	
Auto-Refresh	REF (2nd)	Active	H	H	L	×	×	×	×	×	×	

Self-Refresh Command Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA1~BA0	A13~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Active	WRA (1st)	Standby	H	H	L	L	×	×	×	×	×	
Self-Refresh Entry	REF (2nd)	Active	H	L	L	×	×	×	×	×	×	7, 8
Self-Refresh Continue	—	Self-Refresh	L	L	×	×	×	×	×	×	×	
Self-Refresh Exit	SELFX	Self-Refresh	L	H	H	×	×	×	×	×	×	9

Power Down Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA1~BA0	A13~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Power Down Entry	PDEN	Standby	H	L	H	×	×	×	×	×	×	8
Power Down Continue	—	Power Down	L	L	×	×	×	×	×	×	×	
Power Down Exit	PDEX	Power Down	L	H	H	×	×	×	×	×	×	9

Notes:
7. $\overline{PD}$ has to be brought to Low within t_{FPDL} from REF command.
8. $\overline{PD}$ should be brought to Low after DQ's state turned high impedance.
9. When $\overline{PD}$ is brought to High from Low, this function is executed asynchronously.

FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{PD}$ n − 1	$\overline{PD}$ n	$\overline{CS}$	FN	ADDRESS	COMMAND	ACTION	NOTES
Idle	H	H	H	×	×	DESL	NOP	
	H	H	L	H	BA, UA	RDA	Row activate for Read	
	H	H	L	L	BA, UA	WRA	Row activate for Write	
	H	L	H	×	×	PDEN	Power Down Entry	10
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Refer to Power Down State	
Row Active for Read	H	H	H	×	LA	LAL	Begin Read	
	H	H	L	×	Op-code	MRS/EMRS	Access to Mode Register	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	MRS/EMRS	Illegal	
	L	×	×	×	×	—	Invalid	
Row Active for Write	H	H	H	×	LA	LAL	Begin Write	
	H	H	L	×	×	REF	Auto-Refresh	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	REF (self)	Self-Refresh Entry	
	L	×	×	×	×	—	Invalid	
Read	H	H	H	×	×	DESL	Continue Burst Read to End	
	H	H	L	H	BA, UA	RDA	Illegal	11
	H	H	L	L	BA, UA	WRA	Illegal	11
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Write	H	H	H	×	×	DESL	Data Write&Continue Burst Write to End	
	H	H	L	H	BA, UA	RDA	Illegal	11
	H	H	L	L	BA, UA	WRA	Illegal	11
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Auto-Refreshing	H	H	H	×	×	DESL	NOP → Idle after I_{REFC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	×	×	PDEN	Self-Refresh Entry	12
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Refer to Self-Refreshing State	
Mode Register Accessing	H	H	H	×	×	DESL	NOP → Idle after I_{RSC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Power Down	H	×	×	×	×	—	Invalid	
	L	L	×	×	×	—	Maintain Power Down Mode	
	L	H	H	×	×	PDEX	Exit Power Down Mode → Idle after t_{PDEX}	
	L	H	L	×	×	—	Illegal	
Self-Refreshing	H	×	×	×	×	—	Invalid	
	L	L	×	×	×	—	Maintain Self-Refresh	
	L	H	H	×	×	SELFX	Exit Self-Refresh → Idle after I_{REFC}	
	L	H	L	×	×	—	Illegal	

Notes: 10. Illegal if any bank is not idle.
11. Illegal to bank in specified states; Function may be legal in the bank inidicated by Bank Address (BA).
12. Illegal if t_{FPDL} is not satisfied.

MODE REGISTER TABLE

Regular Mode Register (Notes: 1)

ADDRESS	BA1 *1	BA0 *1	A13~A8	A7 *3	A6~A4	A3	A2~A0
Register	0	0	0	TE	CL	BT	BL

A7	TEST MODE (TE)
0	Regular (default)
1	Test Mode Entry

A3	BURST TYPE (BT)
0	Sequential
1	Interleave

A6	A5	A4	$\overline{CAS}$ LATENCY (CL)
0	0	×	Reserved *2
0	1	0	Reserved *2
0	1	1	Reserved *2
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved *2

A2	A1	A0	BURST LENGTH (BL)
0	0	0	Reserved *2
0	0	1	2
0	1	0	4
0	1	1	Reserved *2
1	×	×	

Extended Mode Register (Notes: 4)

ADDRESS	BA1 *4	BA0 *4	A13~A7	A6~A5	A4~A3	A2~A1	A0 *5
Register	0	1	0	SS	DIC (QS)	DIC (DQ)	DS

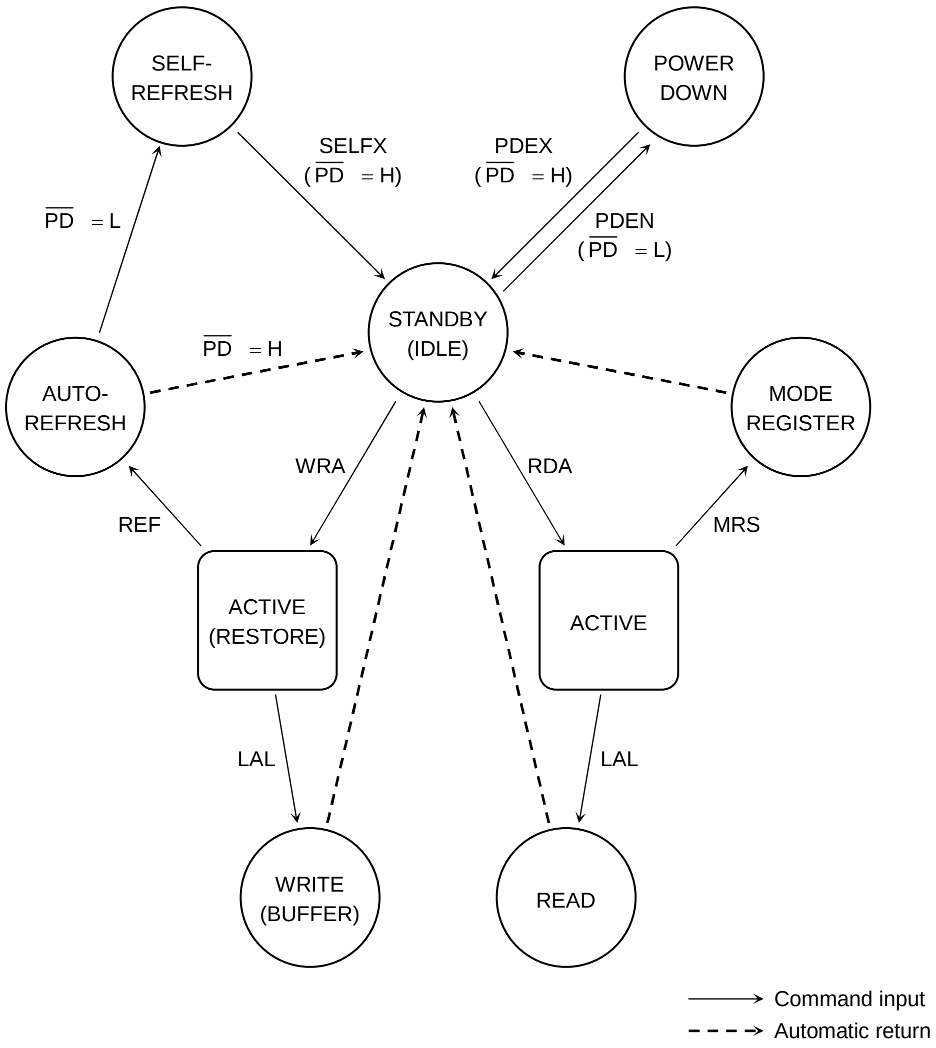
A6	A5	STROBE SELECT
0	0	Reserved *2
0	1	Reserved *2
1	0	Unidirectional DS/QS
1	1	Unidirectional DS/Free Running QS

QS		DQ		OUTPUT DRIVE IMPEDANCE CONTROL (DIC)
A4	A3	A2	A1	
0	0	0	0	Normal Output Driver
0	1	0	1	Strong Output Driver
1	0	1	0	Weak Output Driver
1	1	1	1	Reserved

A0	DLL SWITCH (DS)
0	DLL Enable
1	DLL Disable

Notes:
1. Regular Mode Register is chosen using the combination of BA0 = 0 and BA1 = 0.
2. "Reserved" places in Regular Mode Register should not be set.
3. A7 in Regular Mode Register must be set to "0" (low state). Because Test Mode is specific mode for supplier.
4. Extended Mode Register is chosen using the combination of BA0 = 1 and BA1 = 0.
5. A0 in Extended Mode Register must be set to "0" to enable DLL for normal operation.

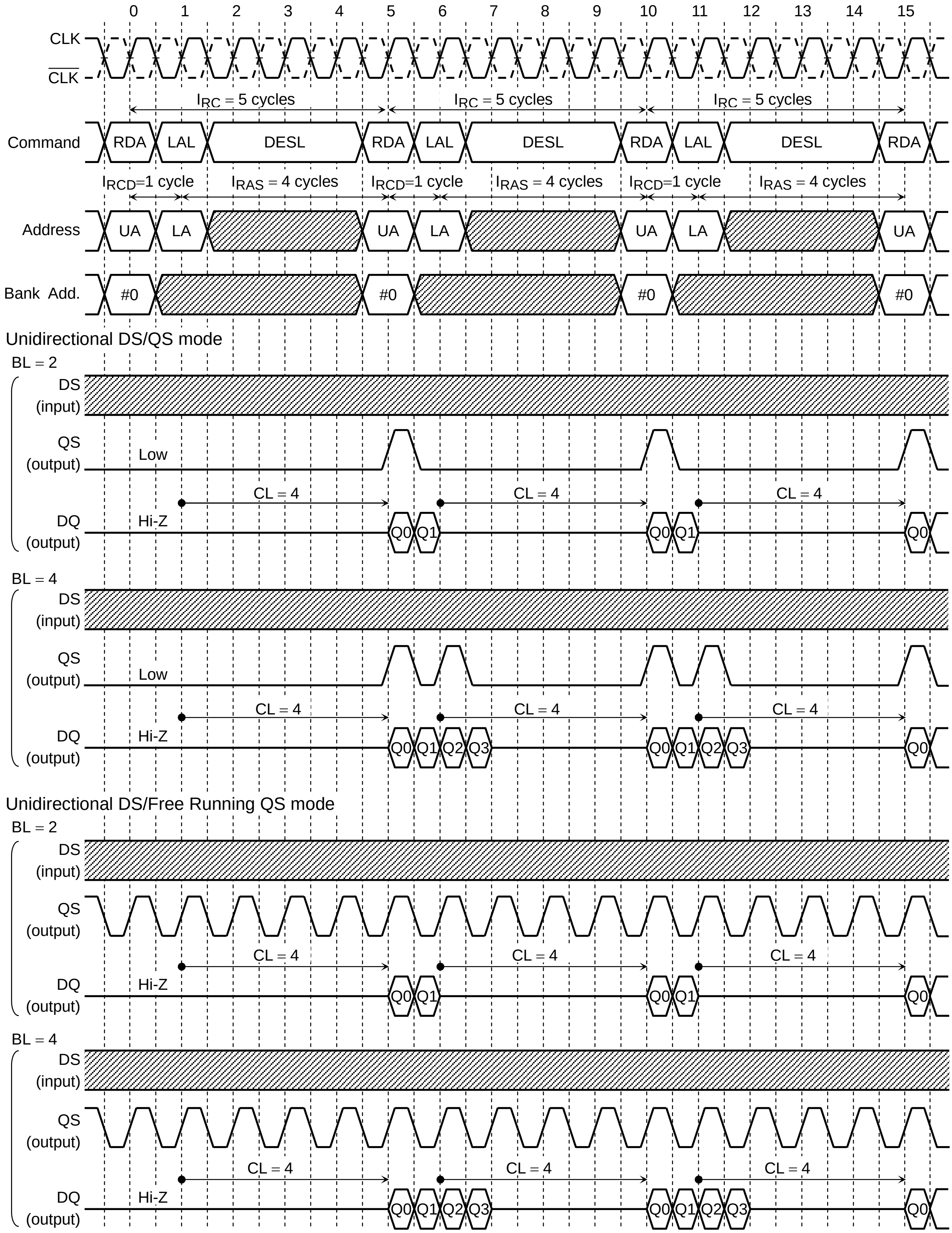
STATE DIAGRAM



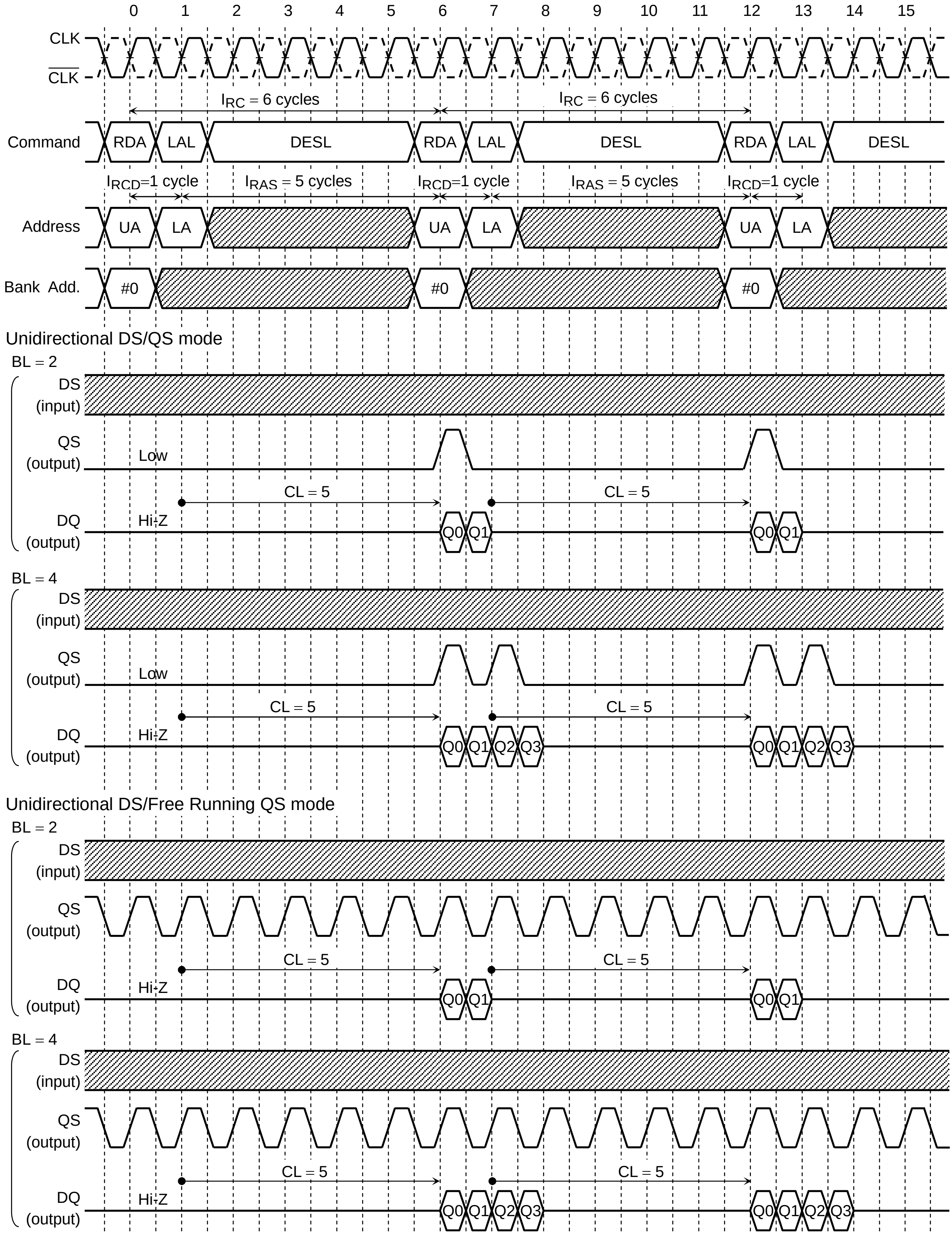
The second command at Active state must be issued 1 clock after RDA or WRA command input.

TIMING DIAGRAMS

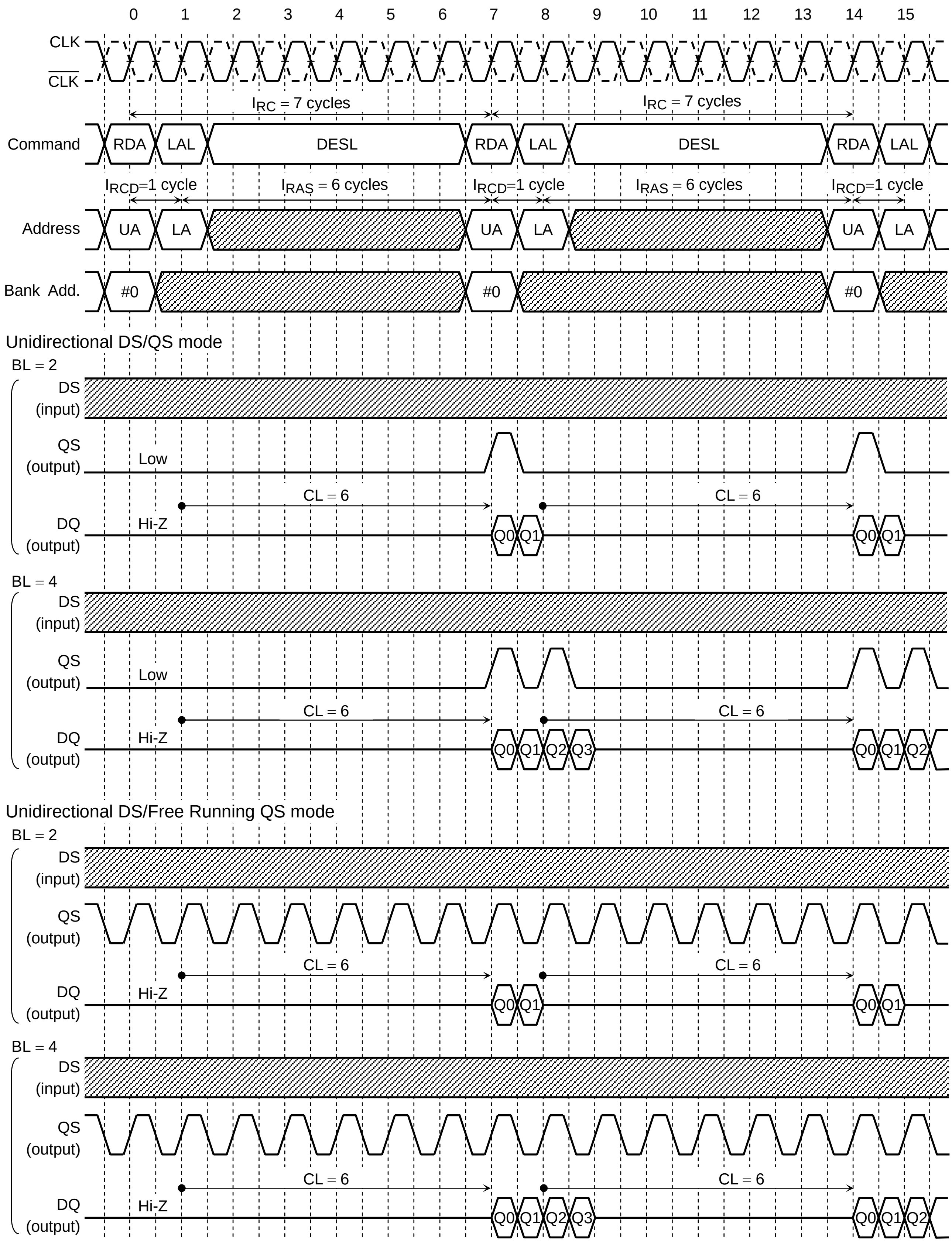
SINGLE BANK READ TIMING (CL = 4)



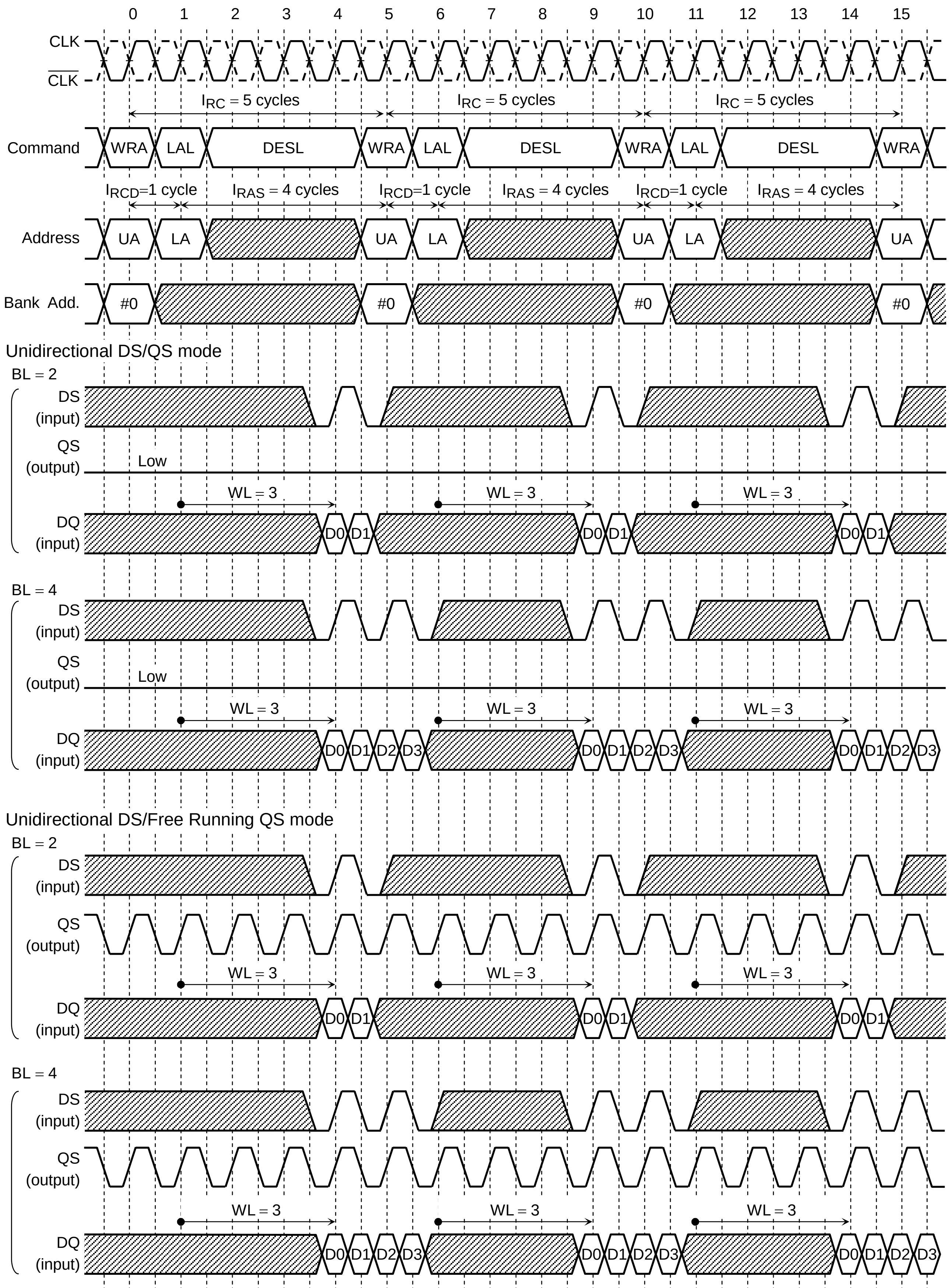
SINGLE BANK READ TIMING (CL = 5)



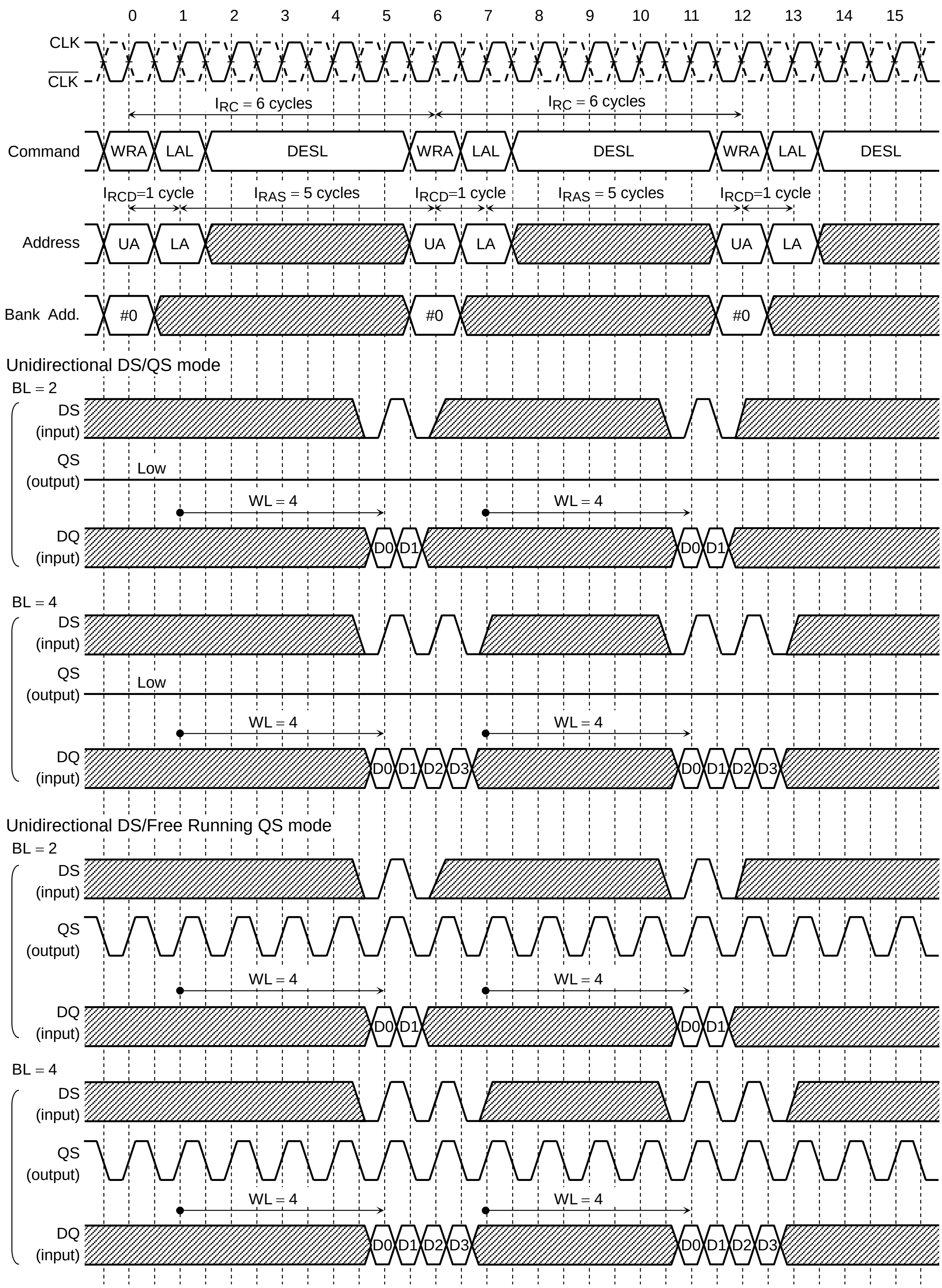
SINGLE BANK READ TIMING (CL = 6)



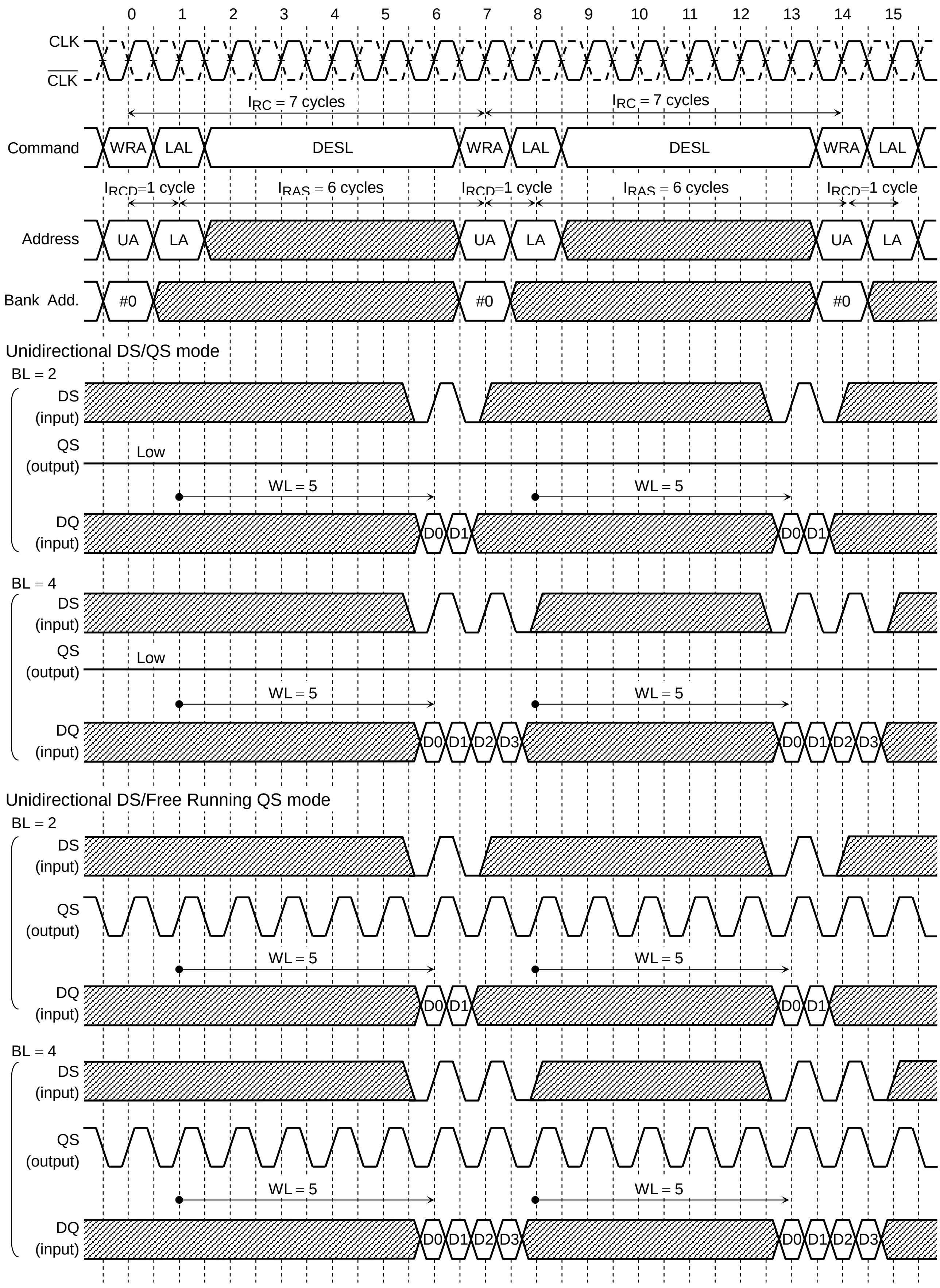
SINGLE BANK WRITE TIMING (CL = 4)



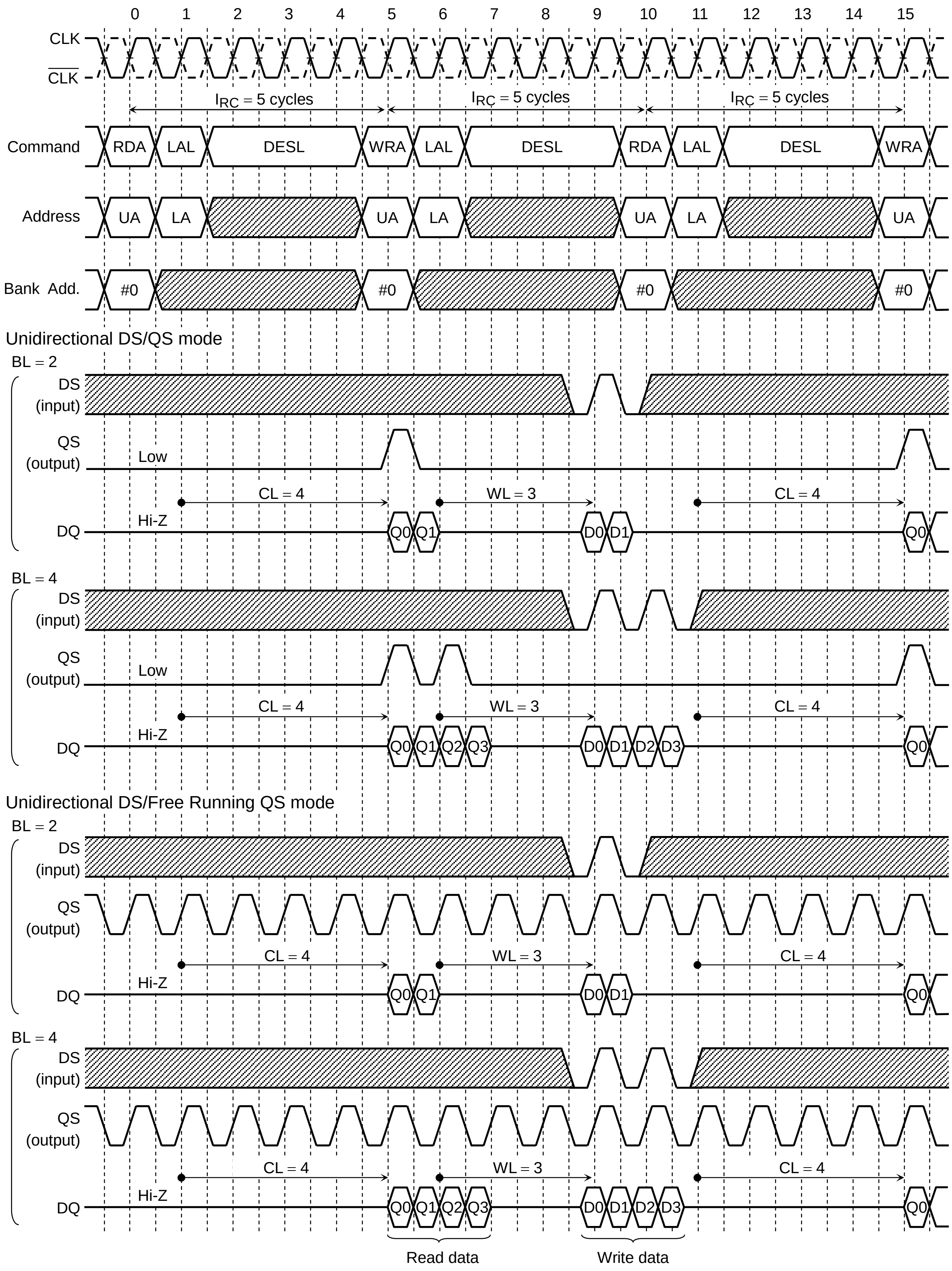
SINGLE BANK WRITE TIMING (CL = 5)



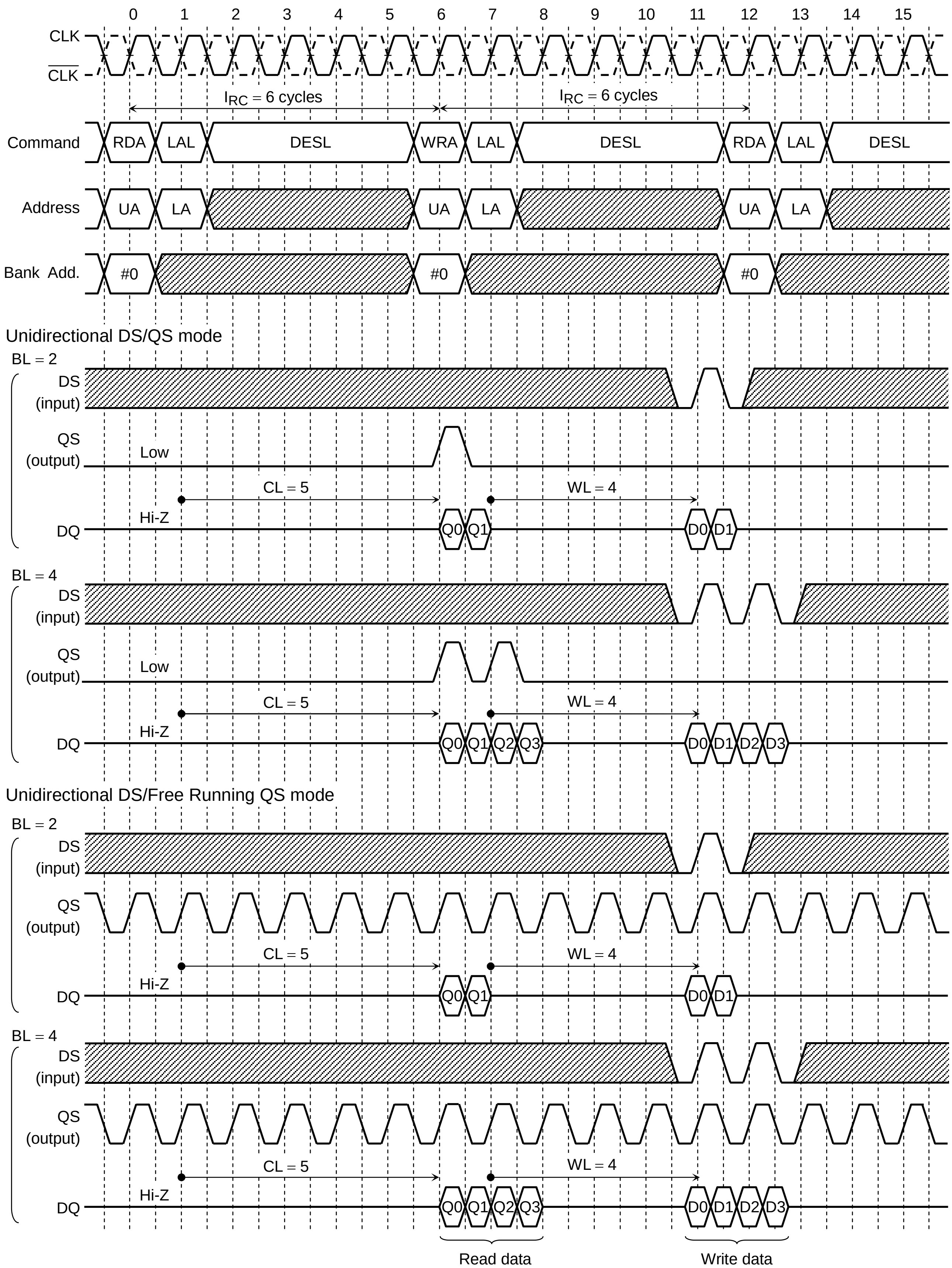
SINGLE BANK WRITE TIMING (CL = 6)



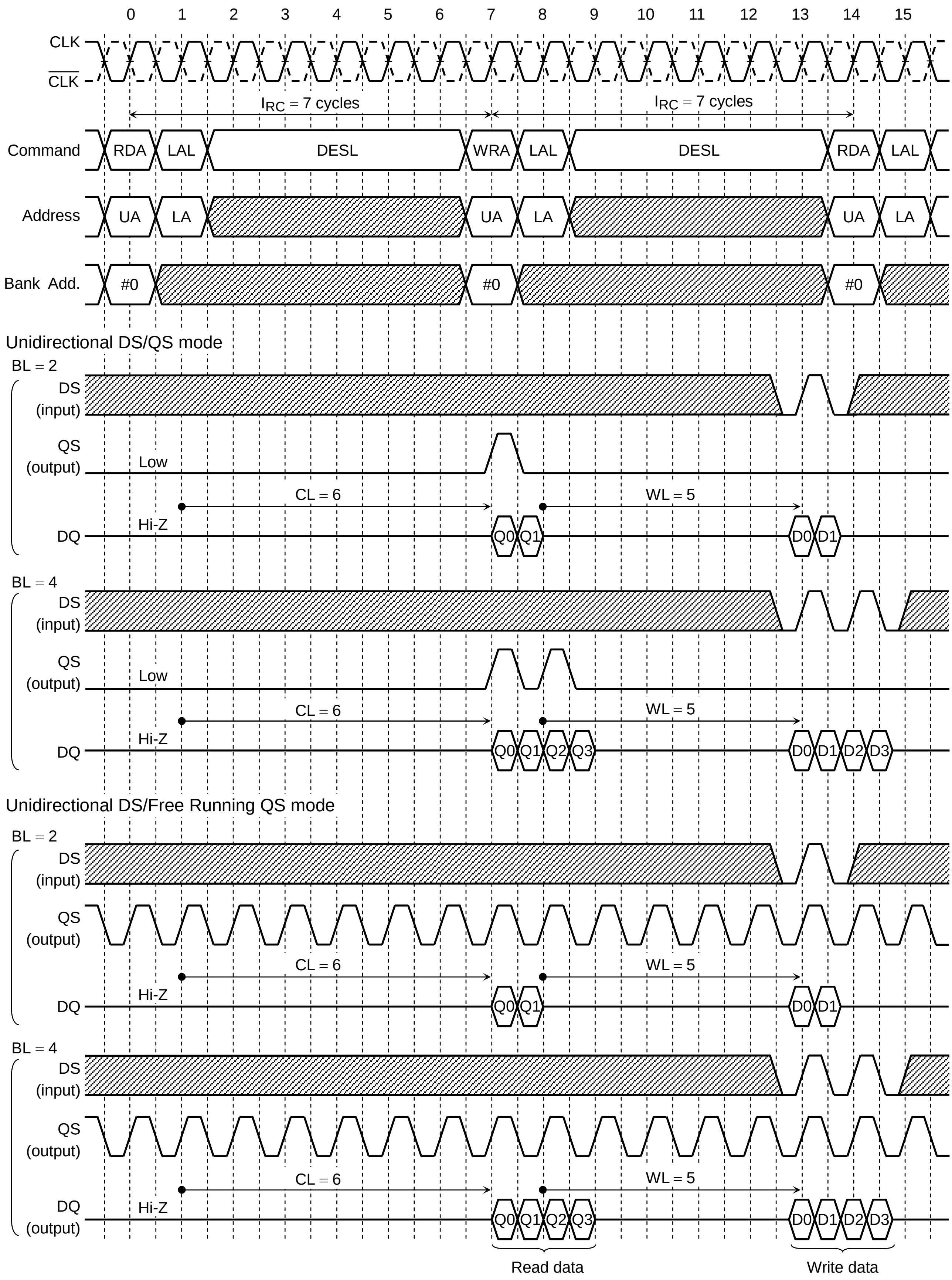
SINGLE BANK READ-WRITE TIMING (CL = 4)



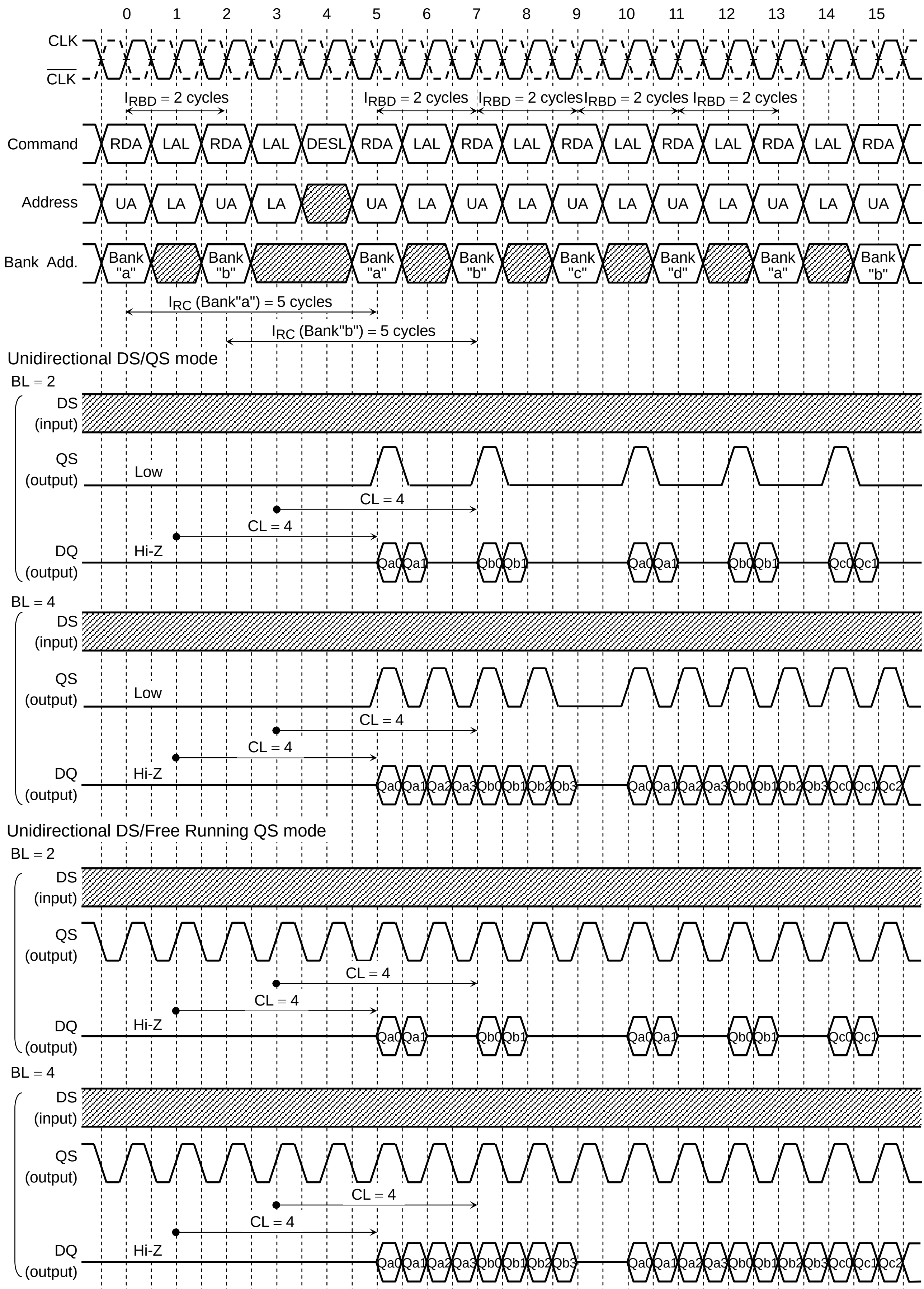
SINGLE BANK READ-WRITE TIMING (CL = 5)



SINGLE BANK READ-WRITE TIMING (CL = 6)

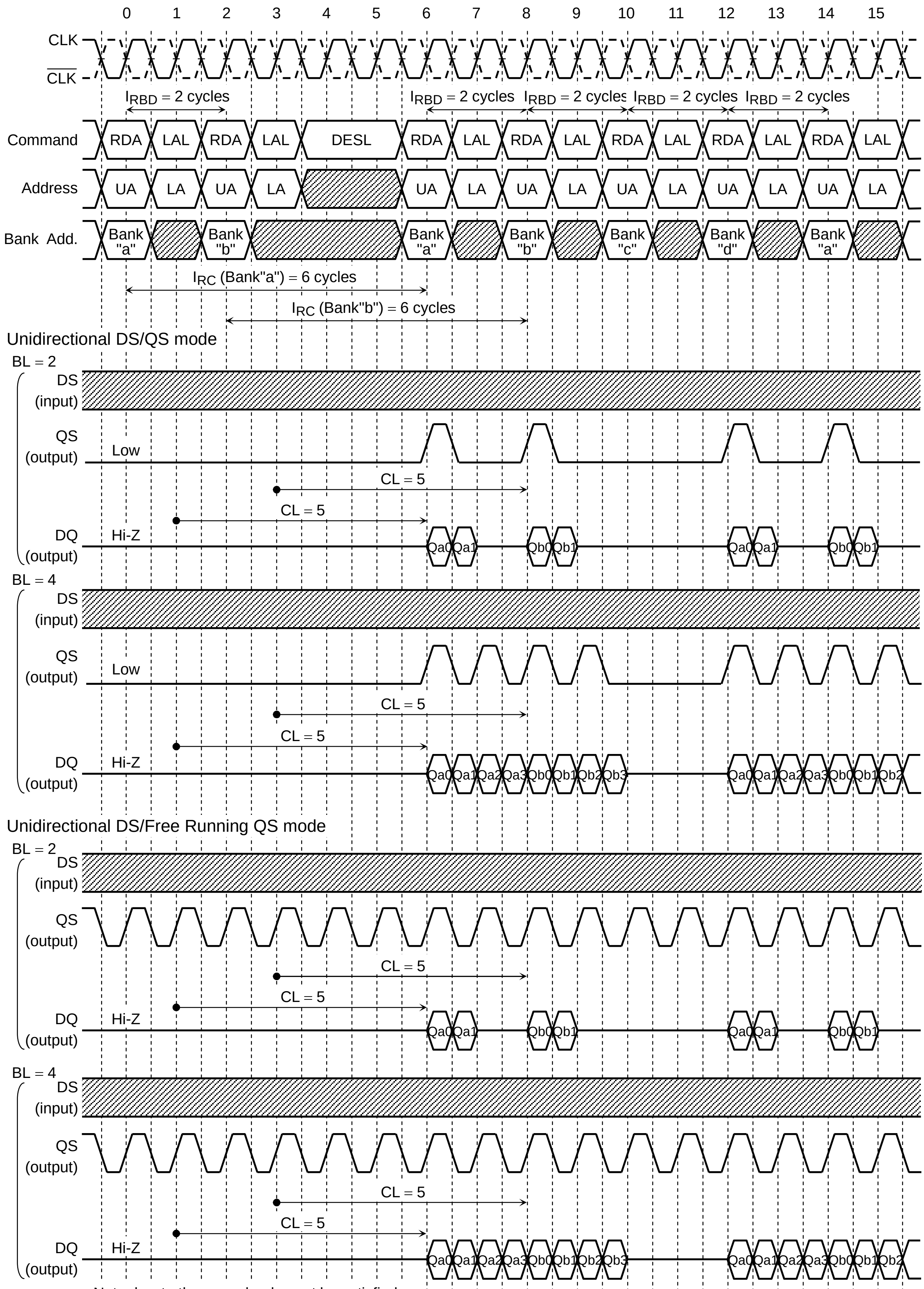


MULTIPLE BANK READ TIMING (CL = 4)



Note: l_{RC} to the same bank must be satisfied.

MULTIPLE BANK READ TIMING (CL = 5)



Note: I_{RC} to the same bank must be satisfied.

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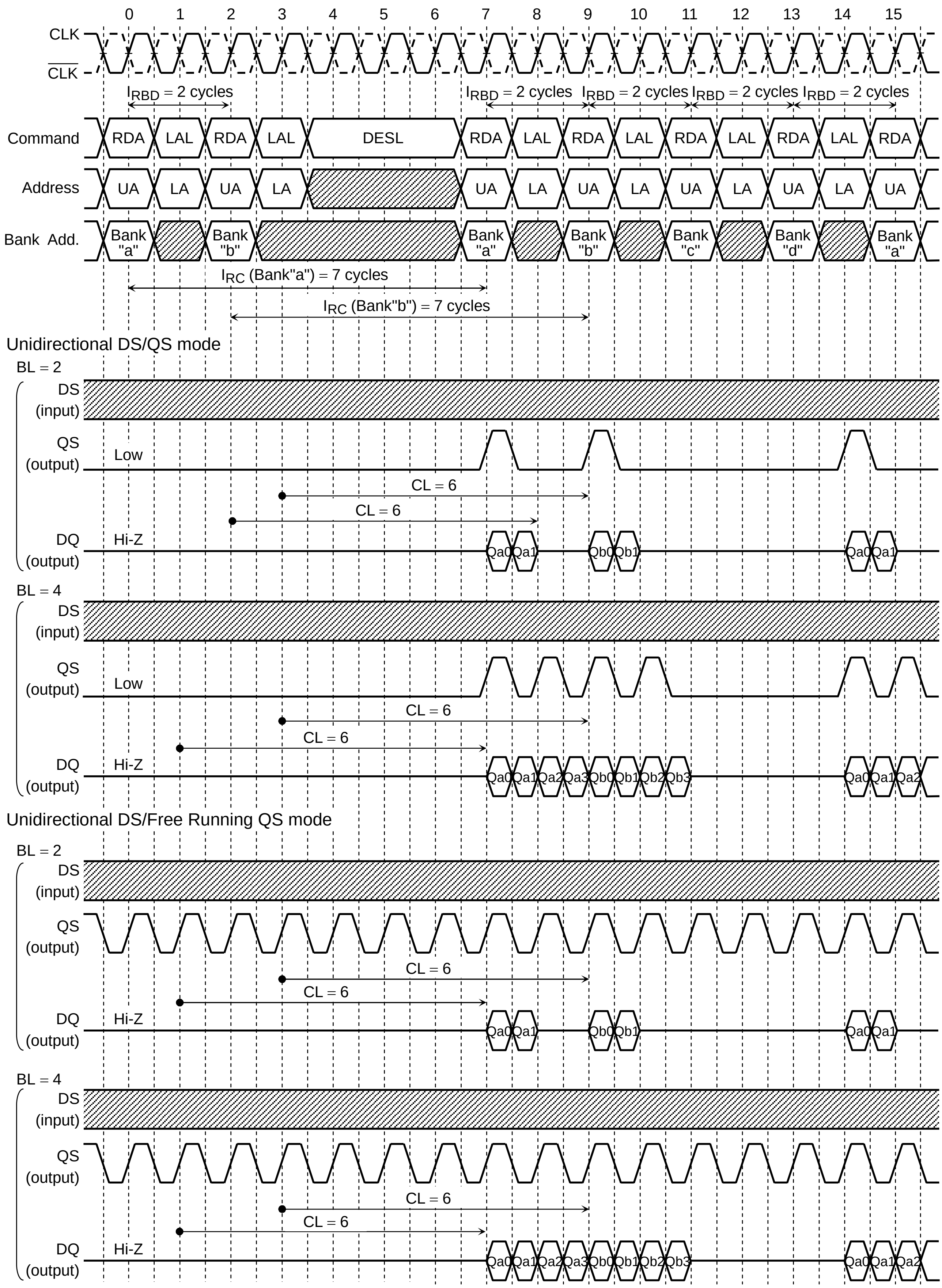
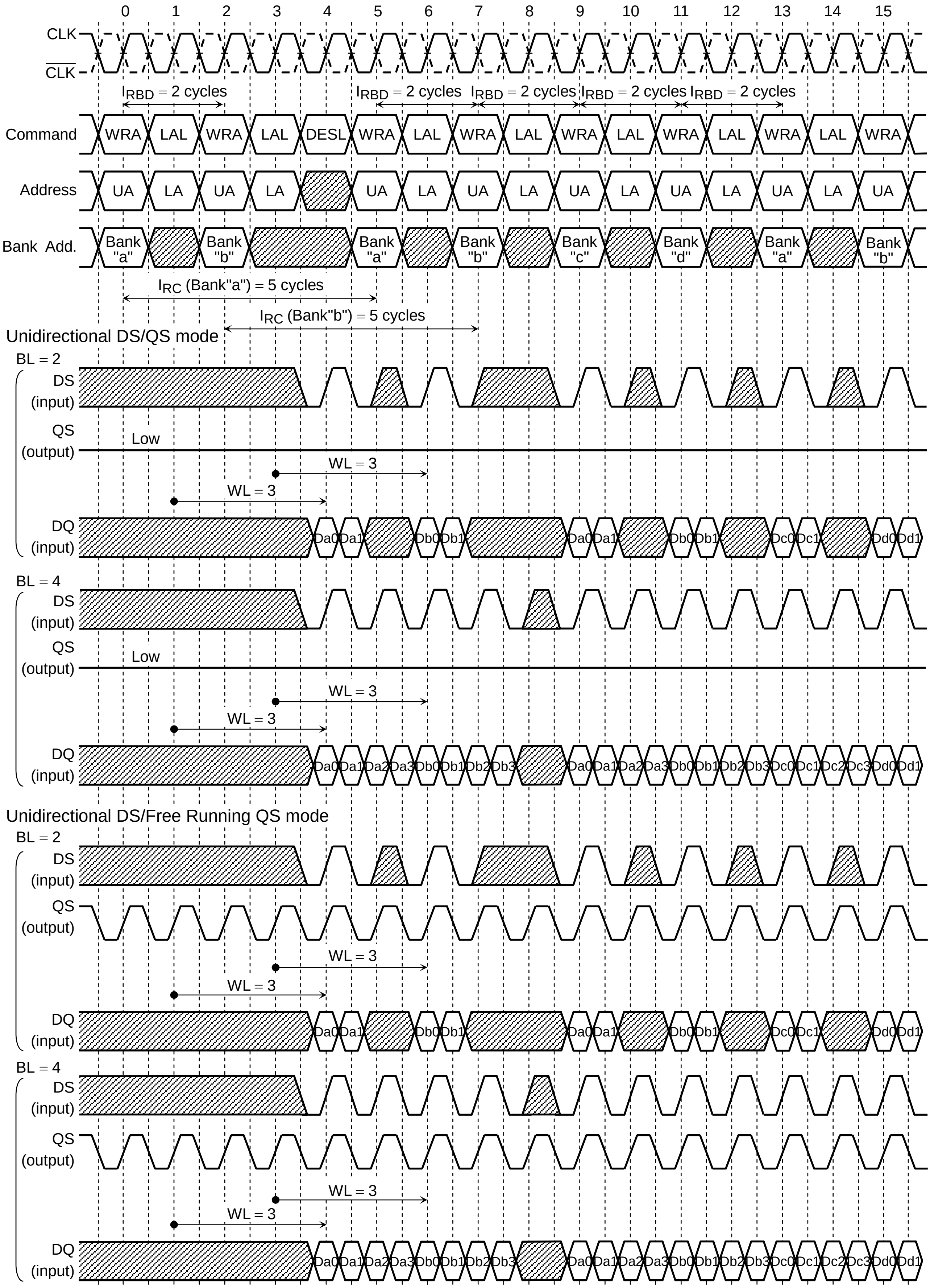
MULTIPLE BANK READ TIMING (CL = 6)



Note: l_{RC} to the same bank must be satisfied.

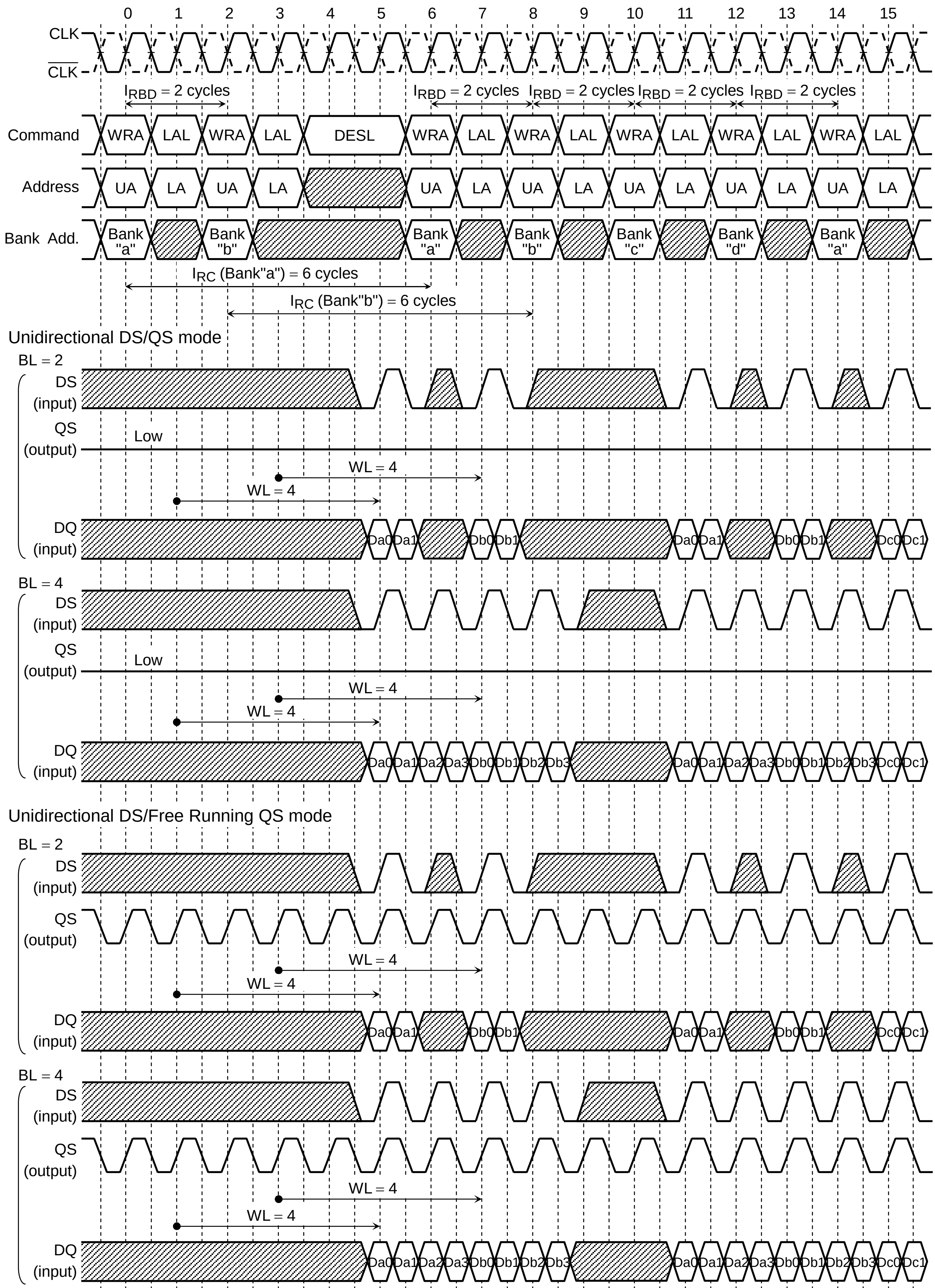
MULTIPLE BANK WRITE TIMING (CL = 4)



Note: I_{RC} to the same bank must be satisfied.

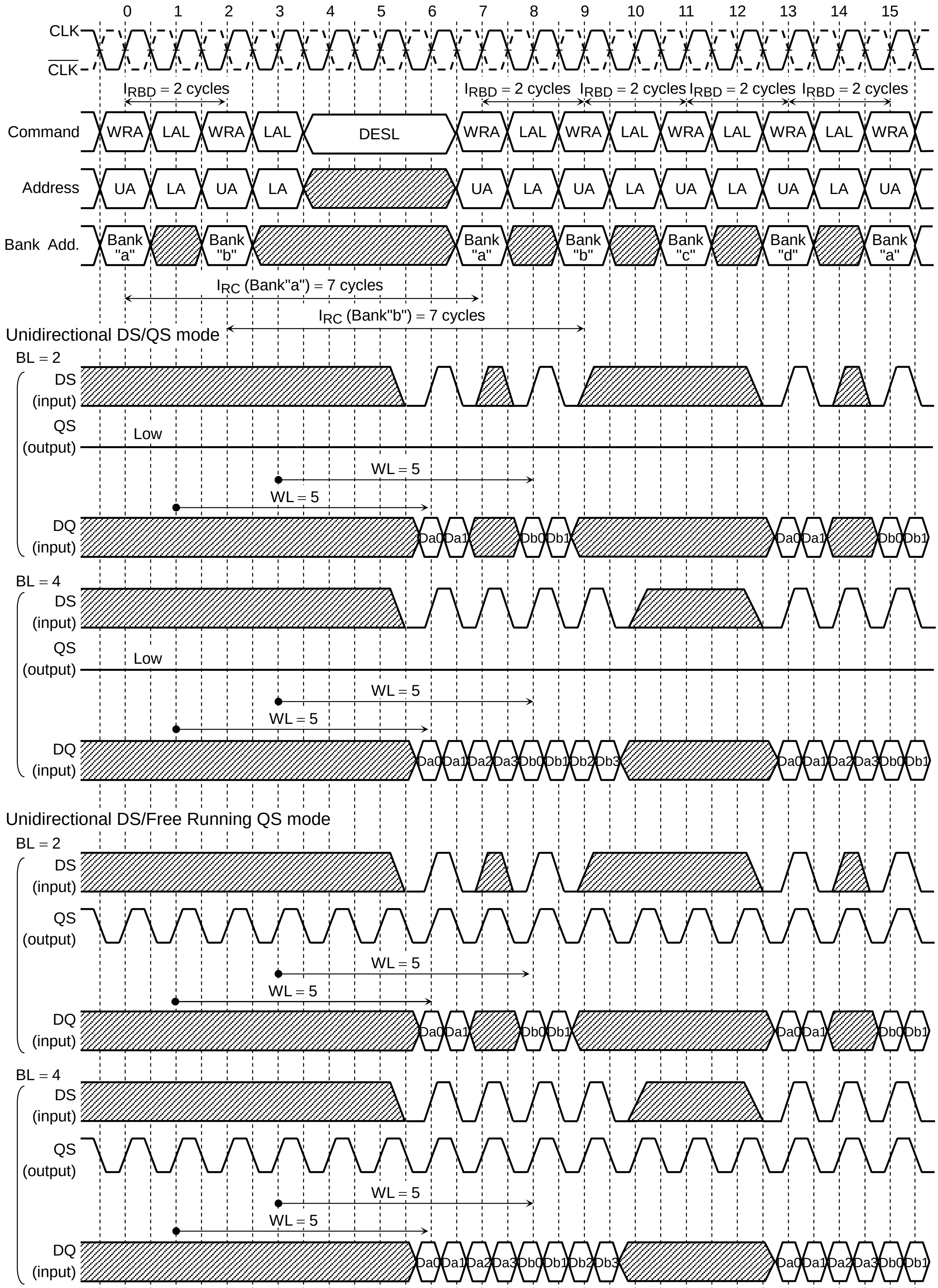
Rev 1.3

MULTIPLE BANK WRITE TIMING (CL = 5)



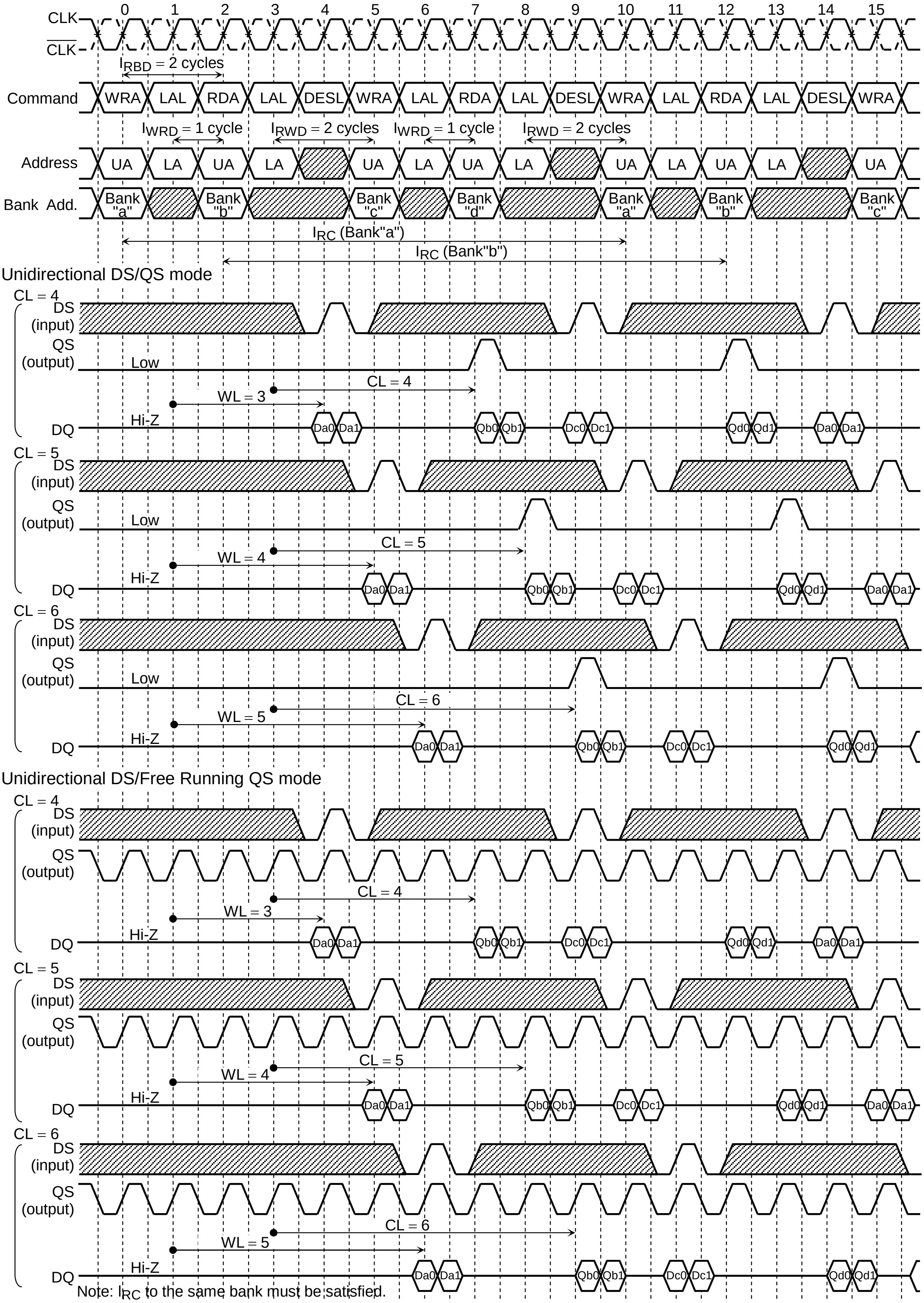
Note: I_{RC} to the same bank must be satisfied.

MULTIPLE BANK WRITE TIMING (CL = 6)



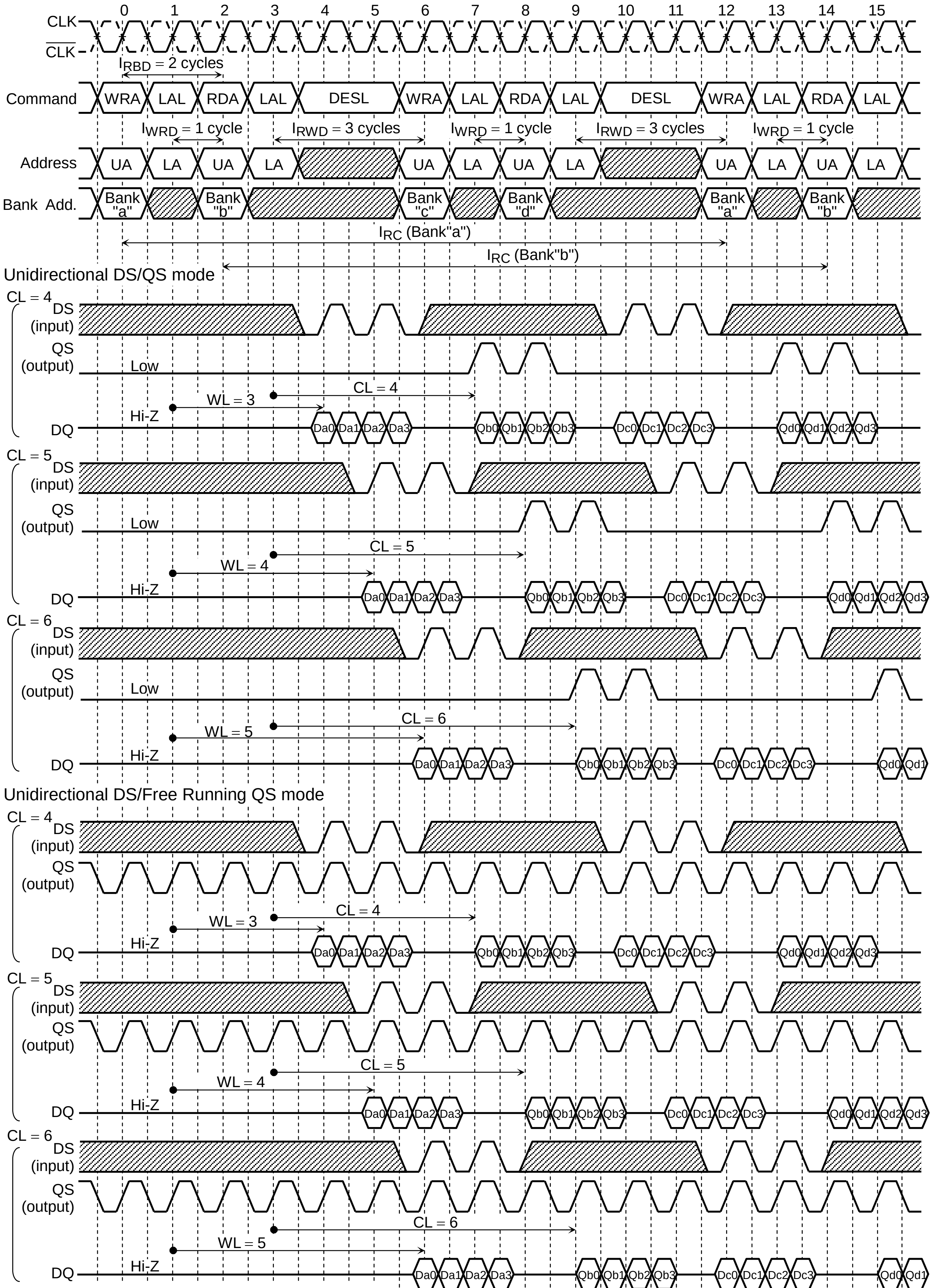
Note: l_{RC} to the same bank must be satisfied.

MULTIPLE BANK READ-WRITE TIMING (BL = 2)



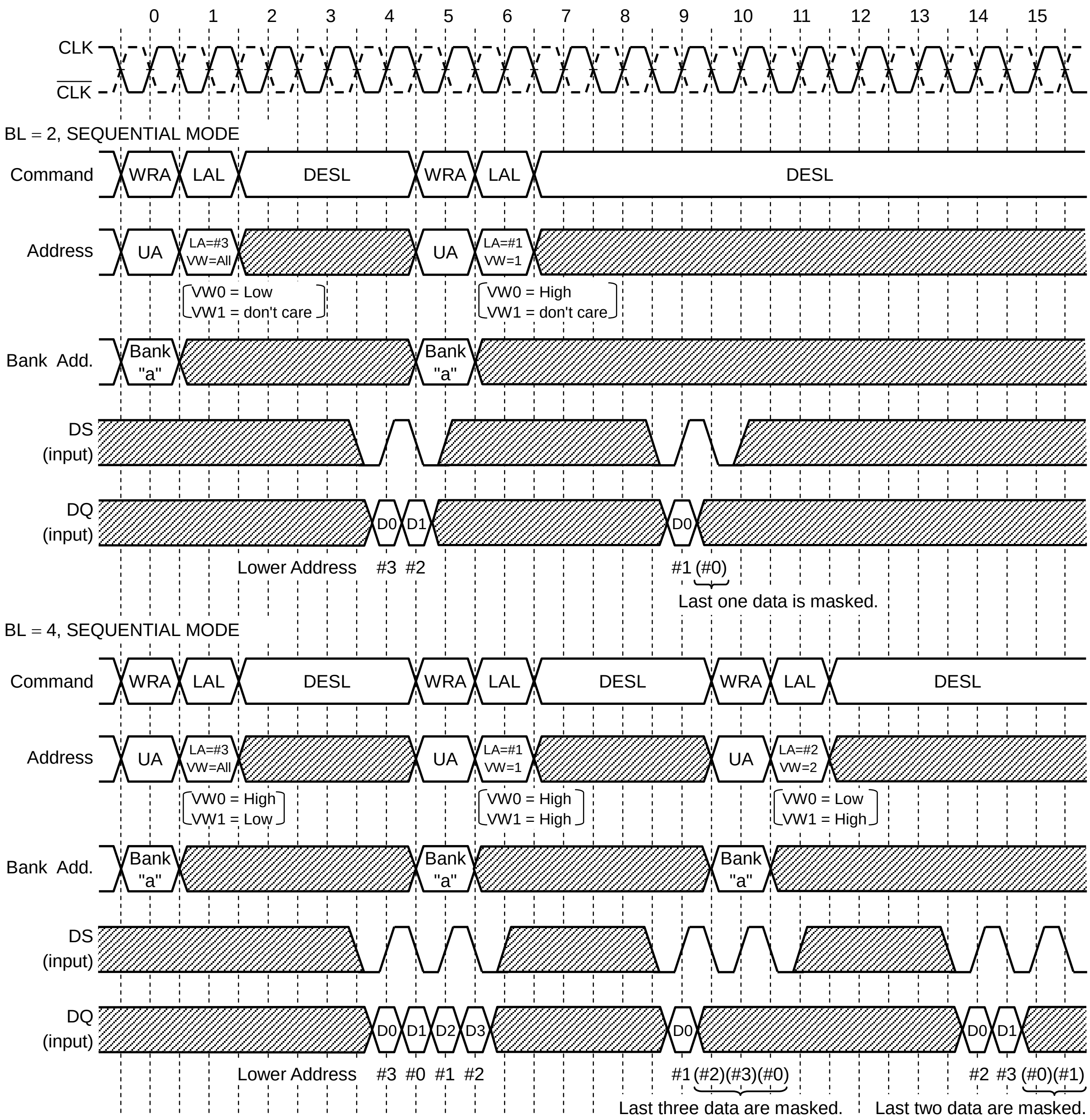
Note: l_{RC} to the same bank must be satisfied.

MULTIPLE BANK READ-WRITE TIMING (BL = 4)



Note: l_{RC} to the same bank must be satisfied.

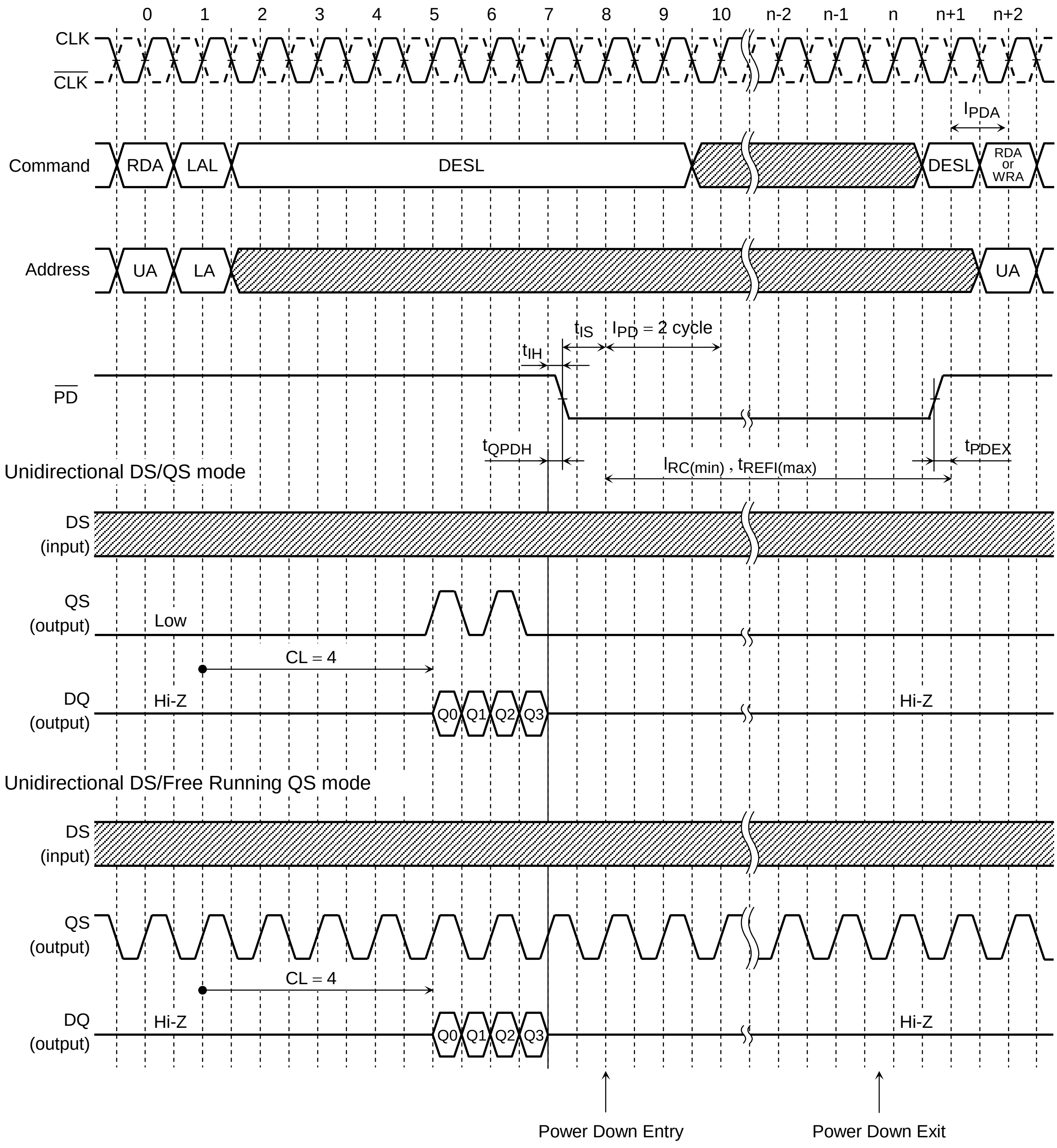
WRITE with VARIABLE WRITE LENGTH (VW) CONTROL (CL = 4)



Note: DS input must be continued till end of burst count even if some of laster data is masked.

POWER DOWN TIMING (CL = 4, BL = 4)

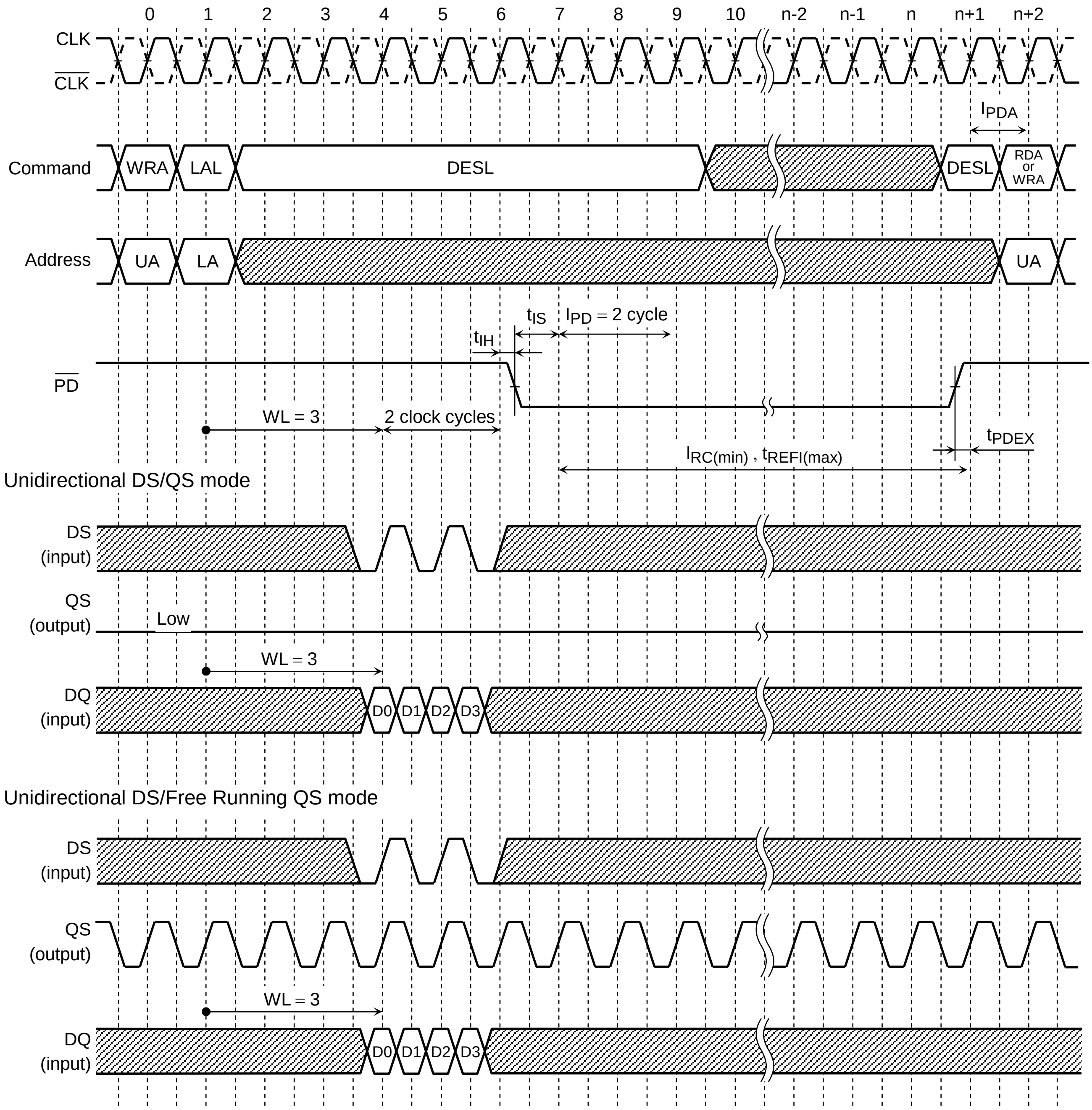
Read cycle to Power Down Mode



Note: $\overline{PD}$ must be kept "High" level until end of Burst data output.
$\overline{PD}$ should be brought to "High" within t_{REFI}(max.) to maintain the data written into cell.
In Power Down Mode, $\overline{PD}$ "Low" and a stable clock signal must be maintained.
When $\overline{PD}$ is brought to "High", a valid executable command may be applied l_{PDA} cycles later.

POWER DOWN TIMING (CL = 4, BL = 4)

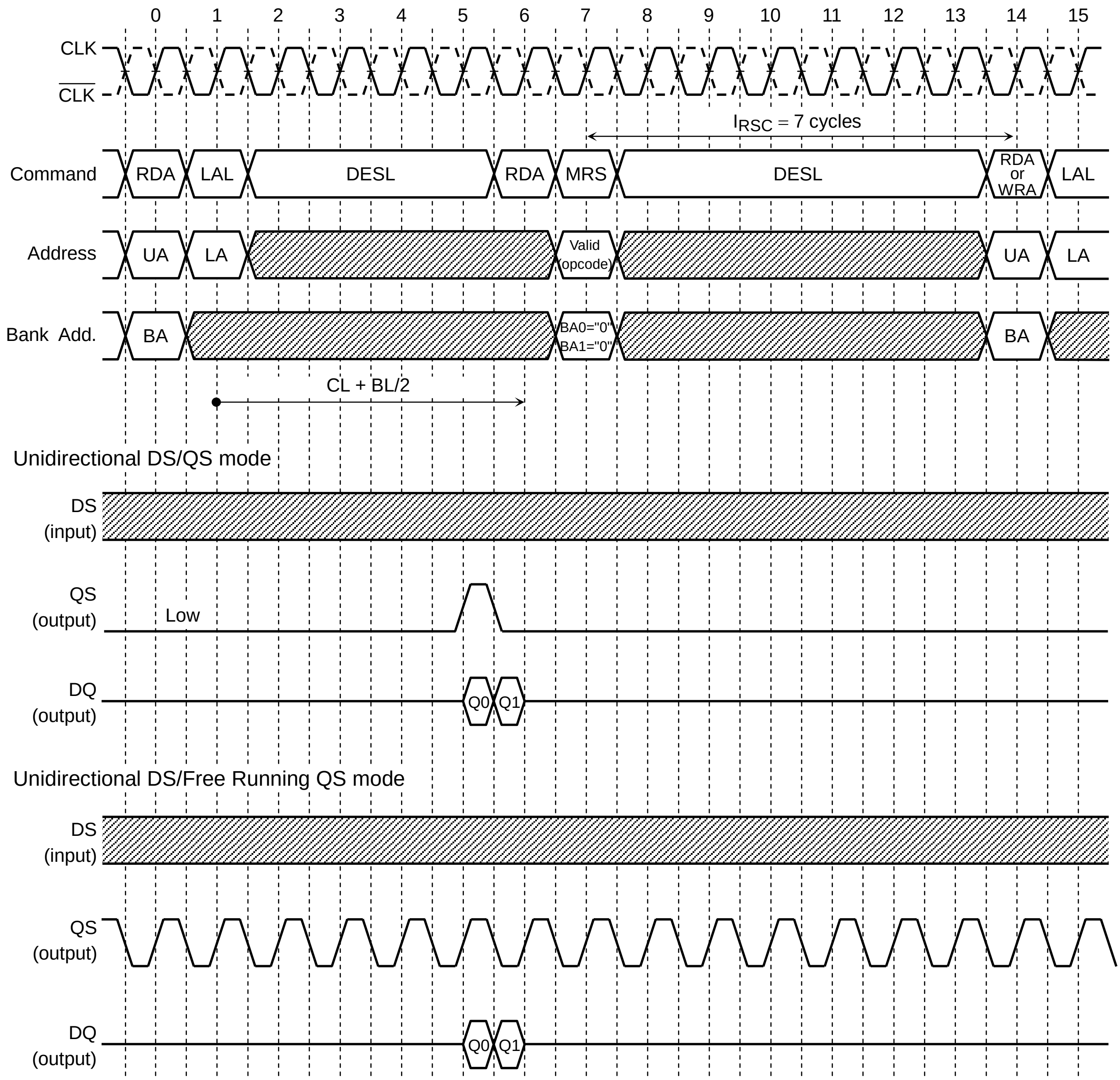
Write cycle to Power Down Mode



Note: $\overline{PD}$ must be kept "High" level until WL+2 clock cycles from LAL command.
$\overline{PD}$ should be brought to "High" within t_{REFI}(max.) to maintain the data written into cell.
In Power Down Mode, $\overline{PD}$ "Low" and a stable clock signal must be maintained.
When $\overline{PD}$ is brought to "High", a valid executable command may be applied l_{PDA} cycles later.

MODE REGISTER SET TIMING (CL = 4, BL = 2)

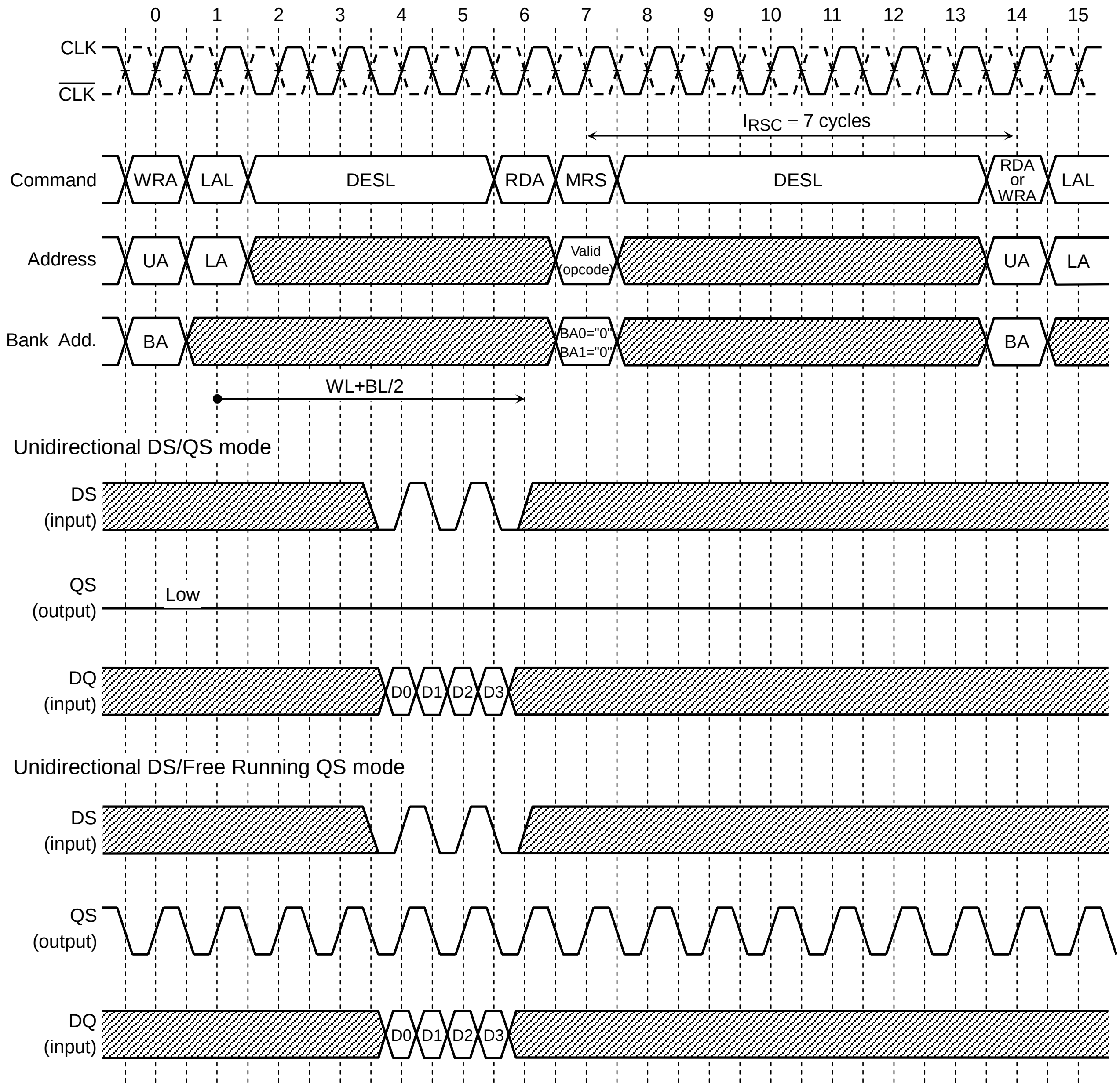
From Read operation to Mode Register Set operation.



Note: Minimum delay from LAL following RDA to RDA of MRS operation is CL+BL/2 clock cycles.

MODE REGISTER SET TIMING (CL = 4, BL = 4)

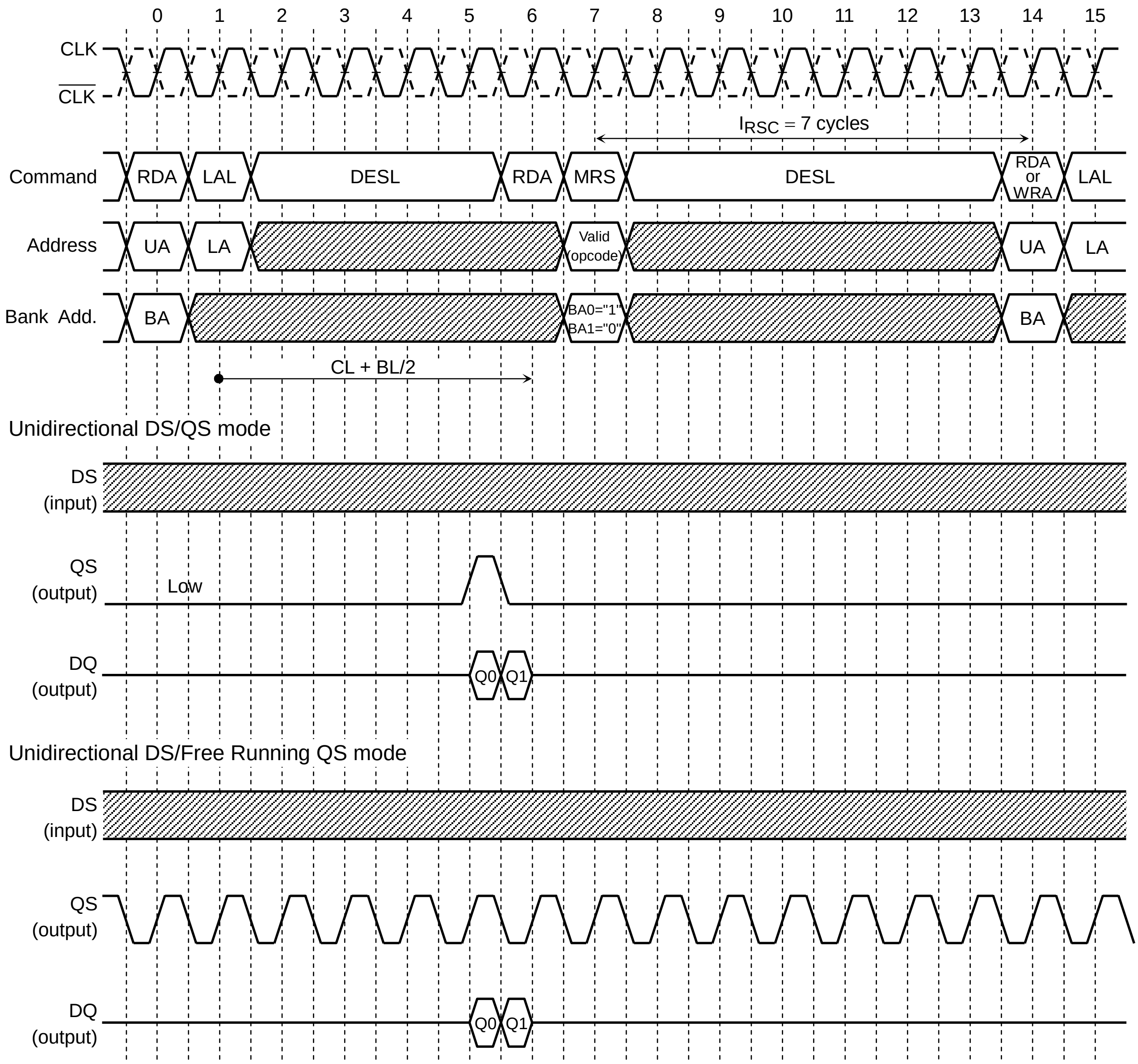
From Write operation to Mode Register Set operation.



Note: Minimum delay from LAL following WRA to RDA of MRS operation is WL+BL/2 clock cycles.

EXTENDED MODE REGISTER SET TIMING (CL = 4, BL = 2)

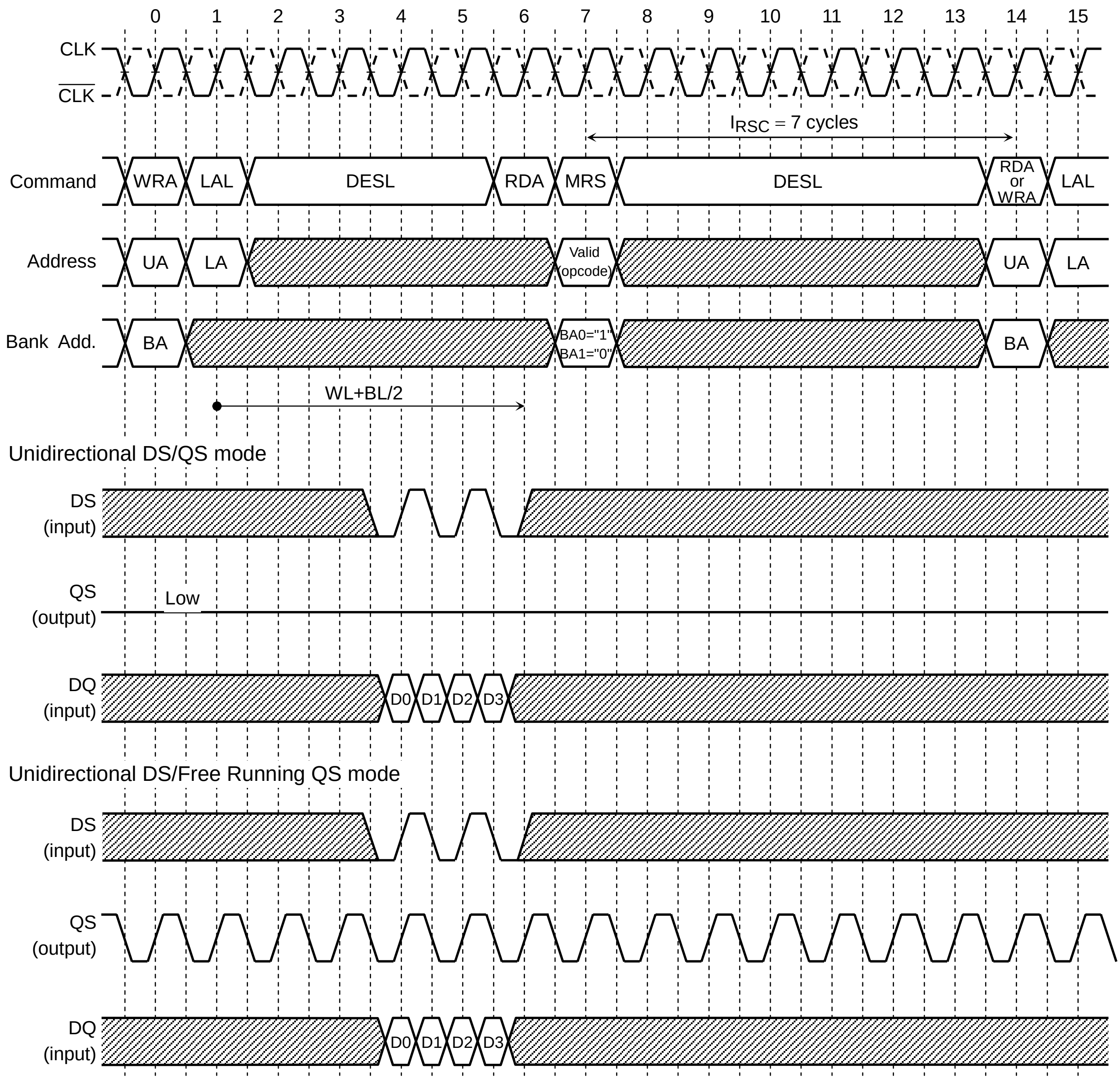
From Read operation to Extended Mode Register Set operation.



Note: Minimum delay from LAL following RDA to RDA of EMRS operation is CL+BL/2 clock cycles.
When DQ strobe mode is changed by EMRS, QS output is invalid for l_{RSC} period.
DLL switch in Extended Mode Register must be set to enable mode for normal operation.
DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.

EXTENDED MODE REGISTER SET TIMING (CL = 4, BL = 4)

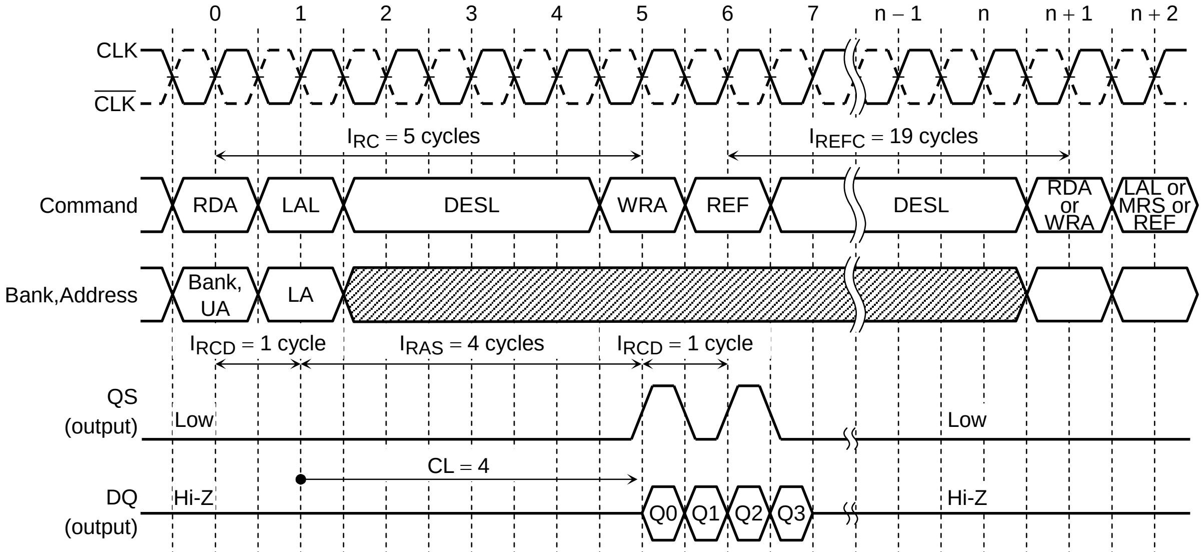
From Write operation to Extended Mode Register Set operation.



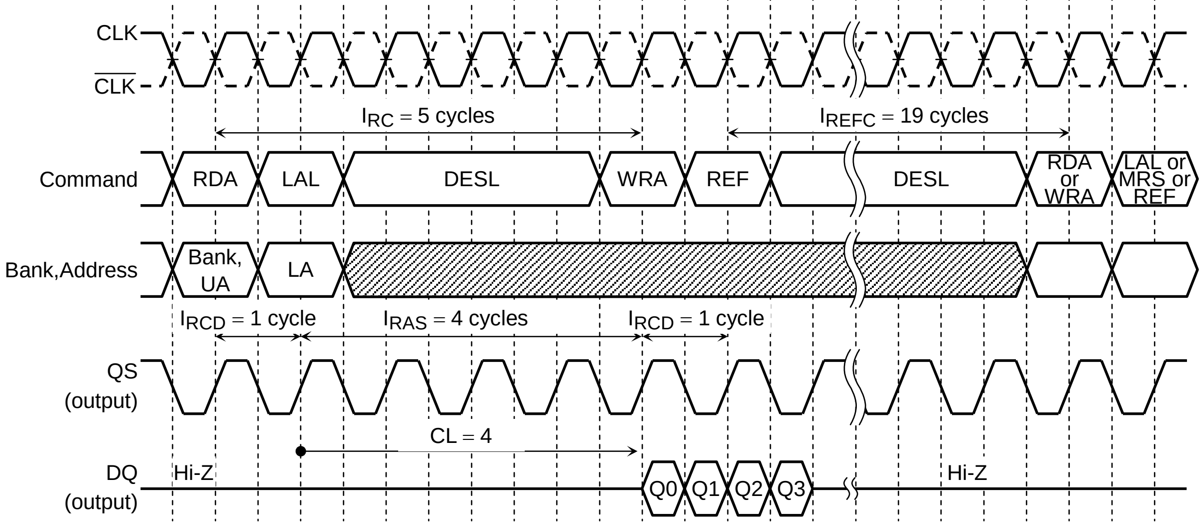
Note: When DQ strobe mode is changed by EMRS, QS output is invalid for I_{RSC} period.
DLL switch in Extended Mode Register must be set to enable mode for normal operation.
DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.
Minimum delay from LAL following WRA to RDA of EMRS operation is WL+BL/2 clock cycles.

AUTO-REFRESH TIMING (CL = 4, BL = 4)

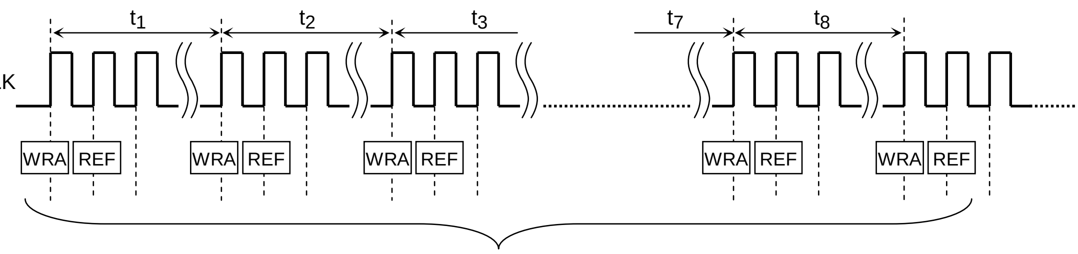
Unidirectional DS/QS mode



Unidirectional DS/Free Running QS mode



Note: In case of CL = 4, l_{REFC} must be meet 19 clock cycles.
When the Auto-Refresh operation is performed, the synthetic average interval of Auto-Refresh command specified by t_{REFI} must be satisfied.
t_{REFI} is average interval time in 8 Refresh cycles that is sampled randomly.

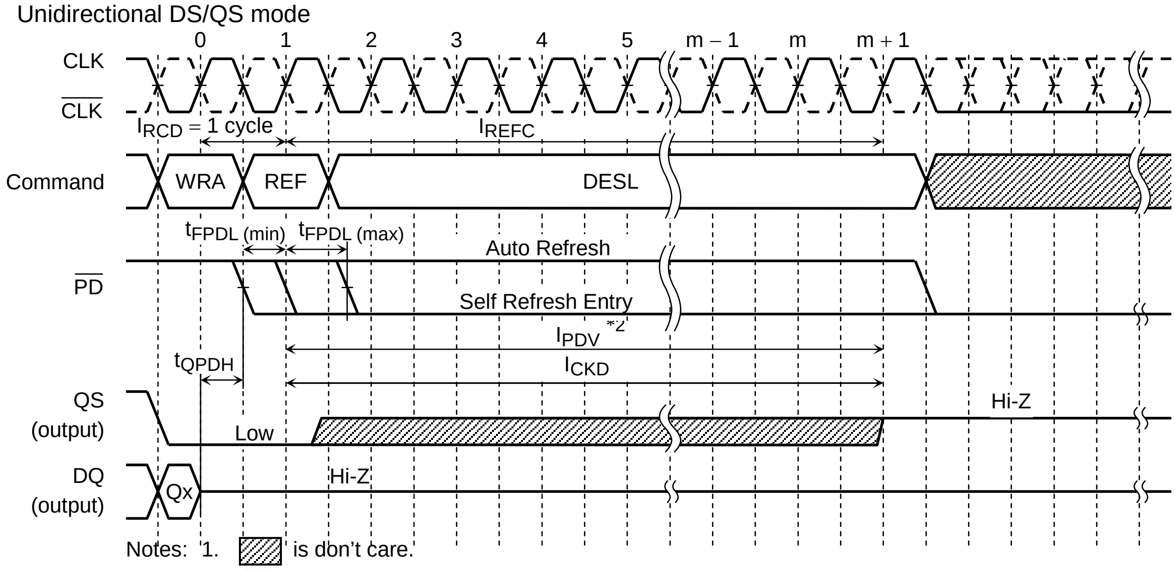


8 Refresh cycle

$$t_{REFI} = \frac{\text{Total time of 8 Refresh cycle}}{8} = \frac{t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8}{8}$$

t_{REFI} is specified to avoid partly concentrated current of Refresh operation that is activated larger area than Read / Write operation.

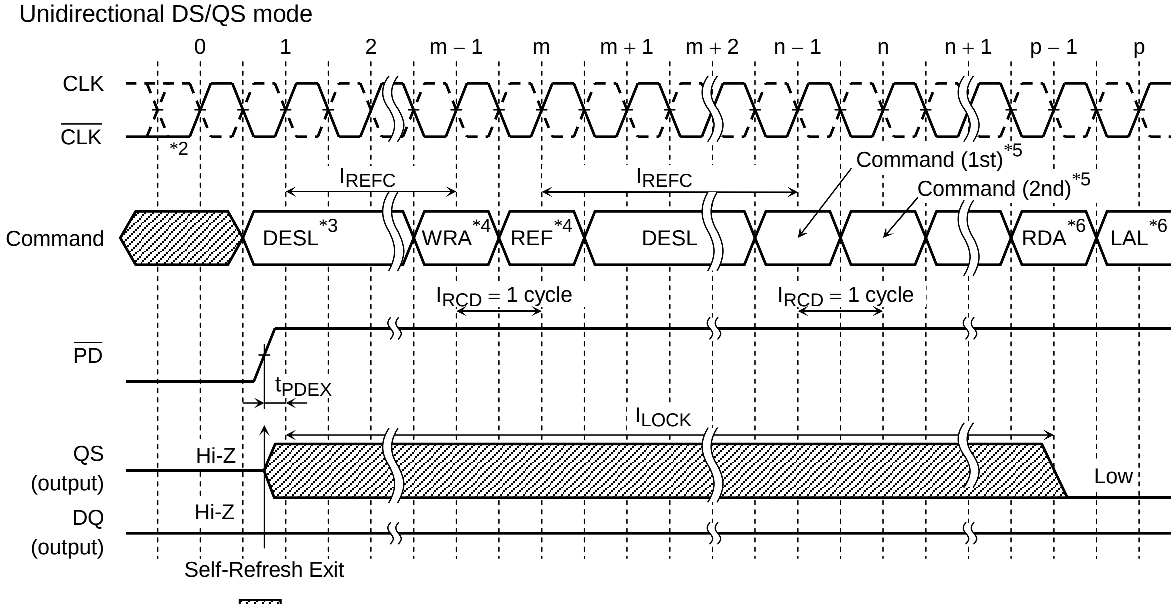
SELF-REFRESH ENTRY TIMING



Notes: 1. [hatched] is don't care.

2. $\overline{PD}$ must be brought to "Low" within the timing between t_{FPDL}(min) and t_{FPDL}(max) to Self Refresh mode. When $\overline{PD}$ is brought to "Low" after l_{PDV}, TC59LM836DKB perform Auto Refresh and enter Power down mode. In case of $\overline{PD}$ fall between t_{FPDL}(max) and l_{PDV}, TC59LM836DKB will either entry Self-Refresh mode or Power down mode after Auto-Refresh operation.
3. It is desirable that clock input is continued at least l_{CKD} from REF command even though $\overline{PD}$ is brought to "Low" for Self-Refresh Entry.
4. In case of Self-Refresh entry after Write Operation, the delay time from the LAL command following WRA to the REF command is Write latency (WL)+2 clock cycles minimum.

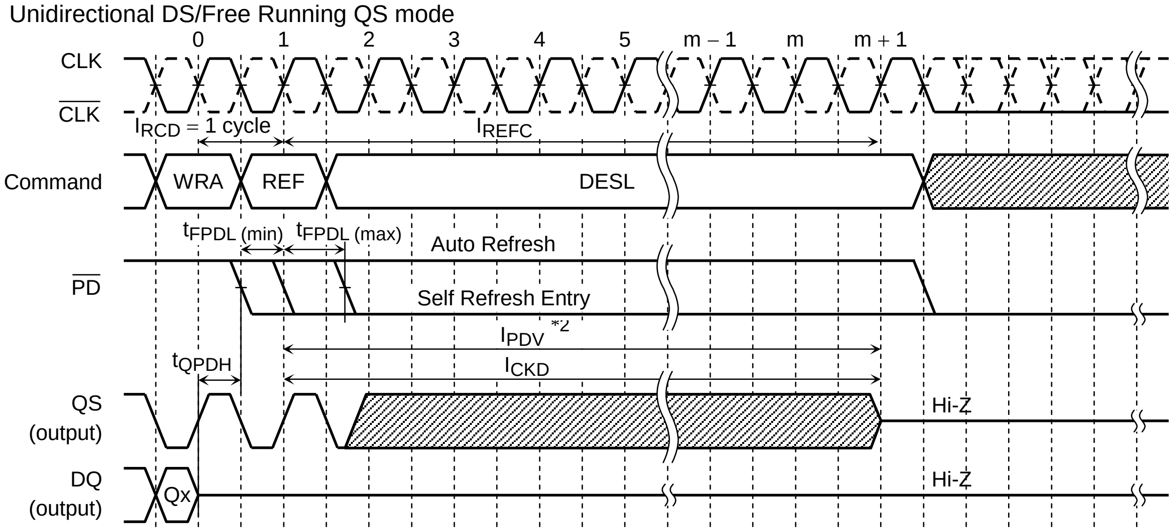
SELF-REFRESH EXIT TIMING



Notes: 1. [hatched] is don't care.

2. Clock should be stable prior to $\overline{PD}$ = "High" if clock input is suspended in Self-Refresh mode.
3. DESL command must be asserted during l_{REFC} after $\overline{PD}$ is brought to "High".
4. It is desirable that one Auto-Refresh command is issued just after Self-Refresh Exit before any other operation.
5. Any command (except Read command) can be issued after l_{REFC}.
6. Read command (RDA + LAL) can be issued after l_{LOCK}.

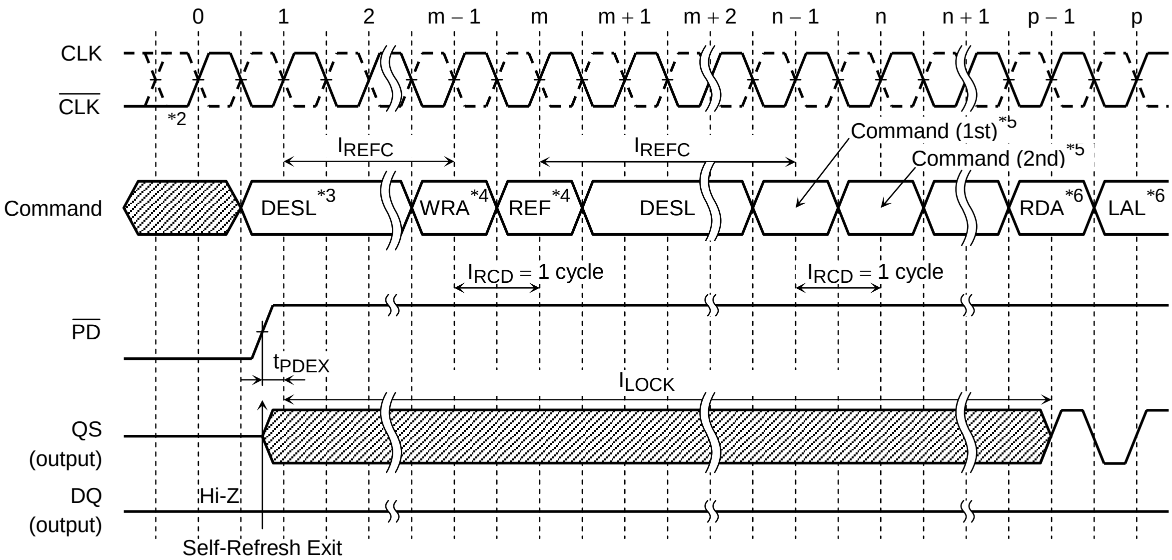
SELF-REFRESH ENTRY TIMING



Notes: 1. [hatched box] is don't care.

2. $\overline{PD}$ must be brought to "Low" within the timing between t_{FPDL}(min) and t_{FPDL}(max) to Self Refresh mode. When $\overline{PD}$ is brought to "Low" after I_{PDV}, TC59LM836DKB perform Auto Refresh and enter Power down mode. In case of $\overline{PD}$ fall between t_{FPDL}(max) and I_{PDV}, TC59LM836DKB will either entry Self-Refresh mode or Power down mode after Auto-Refresh operation.
3. It is desirable that clock input is continued at least I_{CKD} from REF command even though $\overline{PD}$ is brought to "Low" for Self-Refresh Entry.

SELF-REFRESH EXIT TIMING



Notes: 1. [hatched box] is don't care.

2. Clock should be stable prior to $\overline{PD}$ = "High" if clock input is suspended in Self-Refresh mode.
3. DESL command must be asserted during I_{REFC} after $\overline{PD}$ is brought to "High".
4. It is desirable that one Auto-Refresh command is issued just after Self-Refresh Exit before any other operation.
5. Any command (except Read command) can be issued after I_{REFC}.
6. Read command (RDA + LAL) can be issued after I_{LOCK}.
7. QS output is invalid until DLL lock from Self-Refresh exit.

FUNCTIONAL DESCRIPTION

Network FCRAM™

The FCRAM™ is an acronym of Fast Cycle Random Access Memory.
The Network FCRAM™ is competent to perform fast random core access, low latency and high-speed data transfer.

PIN FUNCTIONS

CLOCK INPUTS: CLK & $\overline{\text{CLK}}$

The CLK and $\overline{\text{CLK}}$ inputs are used as the reference for synchronous operation. CLK is master clock input. The $\overline{\text{CS}}$, FN and all address input signals are sampled on the crossing of the positive edge of CLK and the negative edge of $\overline{\text{CLK}}$. The QS and DQ output data are aligned to the crossing point of CLK and $\overline{\text{CLK}}$. The timing reference point for the differential clock is when the CLK and $\overline{\text{CLK}}$ signals cross during a transition.

POWER DOWN: $\overline{\text{PD}}$

The PD input controls the entry to the Power Down or Self-Refresh modes. The $\overline{\text{PD}}$ input does not have a Clock Suspend function like a CKE input of a standard SDRAMs, therefore it is illegal to bring $\overline{\text{PD}}$ pin into low state if any Read or Write operation is being performed.

CHIP SELECT & FUNCTION CONTROL: $\overline{\text{CS}}$ & FN

The $\overline{\text{CS}}$ and FN inputs are a control signal for forming the operation commands on FCRAM™. Each operation mode is decided by the combination of the two consecutive operation commands using the $\overline{\text{CS}}$ and FN inputs.

BANK ADDRESSES: BA0 & BA1

The BA0 and BA1 inputs are latched at the time of assertion of the RDA or WRA command and are selected the bank to be used for the operation. BA0 and BA1 also define which mode register is loaded during the Mode Register Set command (MRS or EMRS).

	BA0	BA1
Bank #0	0	0
Bank #1	1	0
Bank #2	0	1
Bank #3	1	1

ADDRESS INPUTS: A0~A13

Address inputs are used to access the arbitrary address of the memory cell array within each bank. The Upper Addresses with Bank addresses are latched at the RDA or WRA command and the Lower Addresses are latched at the LAL command. The A0 to A13 inputs are also used for setting the data in the Regular or Extended Mode Register set cycle.

I/O Organization	UPPER ADDRESS	LOWER ADDRESS
36 bits	A0~A13	A0~A6

DATA INPUT/OUTPUT: DQ0~DQ35

The input data of DQ0 to DQ35 are taken in synchronizing with the both edges of DS input signal. The output data of DQ0 to DQ35 are outputted synchronizing with the both edges of QS output signal.

DATA STROBE: LDS, UDS, LQS, UQS

Method of data strobe is chosen by Extended mode register. LDS and LQS are for DQ0 to DQ17. UDS and UQS are for DQ18 to DQ35.

(1) Unidirectional DS / QS mode

DS is input signal and QS is output signal. Both edges of DS are used to sample all DQs at Write operation. Both edges of QS are used for trigger signal of all DQs at Read operation. During Write, Auto-Refresh and NOP cycle, QS assert always “Low” level. QS is Hi-Z in Self-Refresh mode.

(2) Unidirectional DS / Free running QS mode

DS is input signal and QS is output signal. Both edge of DS are used to sample all DQs at Write operation. Both edges of QS are used for trigger signal of all DQs at Read operation. QS assert always toggle signal except Self-Refresh mode. This strobe type is easy to use for pin to pin connect application.

POWER SUPPLY: V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}

V_{DD} and V_{SS} are power supply pins for memory core and peripheral circuits.
V_{DDQ} and V_{SSQ} are power supply pins for the output buffer.

REFERENCE VOLTAGE: V_{REF}

V_{REF} is reference voltage for all input signals.

COMMAND FUNCTIONS and OPERATIONS

TC59LM836DKB are introduced the two consecutive command input method. Therefore, except for Power Down mode, each operation mode decided by the combination of the first command and the second command from stand-by states of the bank to be accessed.

Read Operation (1st command + 2nd command = RDA + LAL)

Issuing the RDA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a read mode. When the LAL command with Lower Addresses is issued at the next clock of the RDA command, the data is read out sequentially synchronizing with the both edges of QS output signal (Burst Read Operation). The initial valid read data appears after $\overline{CAS}$ latency from the issuing of the LAL command. The valid data is outputted for a burst length. The $\overline{CAS}$ latency, the burst length of read data and the burst type must be set in the Mode Register beforehand. The read operated bank goes back automatically to the idle state after l_{RC}.

Write Operation (1st command + 2nd command = WRA + LAL)

Issuing the WRA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a write mode. When the LAL command with Lower Addresses is issued at the next clock of the WRA command, the input data is latched sequentially synchronizing with the both edges of DS input signal (Burst Write Operation). The data and DS inputs have to be asserted in keeping with clock input after $\overline{CAS}$ latency-1 from the issuing of the LAL command. The DS has to be provided for a burst length. The $\overline{CAS}$ latency and the burst type must be set in the Mode Register beforehand. The write operated bank goes back automatically to the idle state after l_{RC}. Write Burst Length is controlled by VW0 and VW1 inputs with LAL command. See VW truth table.

Auto-Refresh Operation (1st command + 2nd command = WRA + REF)

TC59LM836DKB are required to refresh like a standard SDRAM. The Auto-Refresh operation is begun with the REF command following to the WRA command. The Auto-Refresh mode can be effective only when all banks are in the idle state. In a point to notice, the write mode started with the WRA command is canceled by the REF command having gone into the next clock of the WRA command instead of the LAL command. The minimum period between the Auto-Refresh command and the next command is specified by l_{REFC}. However, about a synthetic average interval of Auto-Refresh command, it must be careful. In case of equally distributed refresh, Auto-Refresh command has to be issued within once for every 3.9 μs by the maximum. In case of burst refresh or random distributed refresh, the average interval of eight consecutive Auto-Refresh commands has to be more than 400 ns always. In other words, the number of Auto-Refresh cycles that can be performed within 3.2 μs (8 × 400 ns) is to 8 times in the maximum.

Self-Refresh Operation (1st command + 2nd command = WRA + REF with $\overline{PD}$ = "L")

In case of Self-Refresh operation, refresh operation can be performed automatically by using an internal timer. When all banks are in the idle state and all outputs are in Hi-Z states, the TC59LM836DKB become Self-Refresh mode by issuing the Self-Refresh command. $\overline{PD}$ has to be brought to "Low" within t_{FPDL} from the REF command following to the WRA command for a Self-Refresh mode entry. In order to satisfy the refresh period, the Self-Refresh entry command should be asserted within 3.9 μs after the latest Auto-Refresh command. Once the device enters Self-Refresh mode, the DESL command must be continued for l_{REFC} period. In addition, it is desirable that clock input is kept in l_{CKD} period. The device is in Self-Refresh mode as long as $\overline{PD}$ held "Low". During Self-Refresh mode, all input and output buffers are disabled except for $\overline{PD}$, therefore the power dissipation lowers. Regarding a Self-Refresh mode exit, $\overline{PD}$ has to be changed over from "Low" to "High" along with the DESL command, and the DESL command has to be continuously issued in the number of clocks specified by l_{REFC}. The Self-Refresh exit function is asynchronous operation. It is required that one Auto-Refresh command is issued to avoid the violation of the refresh period just after l_{REFC} from Self-Refresh exit.

Power Down Mode ($\overline{PD}$ = "L")

When all banks are in the idle state and DQ outputs are in Hi-Z states, the TC59LM836DKB become Power Down Mode by asserting $\overline{PD}$ is "Low". When the device enters the Power Down Mode, all input and output buffers are disabled after specified time except for $\overline{PD}$, CLK, $\overline{CLK}$ and QS. Therefore, the power dissipation lowers. To exit the Power Down Mode, $\overline{PD}$ has to be brought to "High" and the DESL command has to be issued for l_{PDA} cycle after $\overline{PD}$ goes high. The Power Down exit function is asynchronous operation.

Mode Register Set (1st command + 2nd command = RDA + MRS)

When all banks are in the idle state, issuing the MRS command following to the RDA command can program the Mode Register. In a point to notice, the read mode started with the RDA command is canceled by the MRS command having gone into the next clock of the RDA command instead of the LAL command. The data to be set in the Mode Register is transferred using A0 to A13, BA0 and BA1 address inputs. The TC59LM836DKB have two mode registers. These are Regular and Extended Mode Register. The Regular or Extended Mode Register is chosen by BA0 and BA1 in the MRS command. The Regular Mode Register designates the operation mode for a read or write cycle. The Regular Mode Register has four function fields.

The four fields are as follows:
(R-1) Burst Length field to set the length of burst data
(R-2) Burst Type field to designate the lower address access sequence in a burst cycle
(R-3) $\overline{\text{CAS}}$ Latency field to set the access time in clock cycle
(R-4) Test Mode field to use for supplier only.

The Extended Mode Register has three function fields.
The three fields are as follows:
(E-1) DLL Switch field to choose either DLL enable or DLL disable
(E-2) Output Driver Impedance Control field.
(E-3) Data Strobe Select

Once those fields in the Mode Register are set up, the register contents are maintained until the Mode Register is set up again by another MRS command or power supply is lost. The initial value of the Regular or Extended Mode Register after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

- Regular Mode Register/Extended Mode Register change bits (BA0, BA1)
  These bits are used to choose either Regular MRS or Extended MRS

BA1	BA0	Mode Register Set
0	0	Regular MRS
0	1	Extended MRS
1	×	Reserved

Regular Mode Register Fields

(R-1) Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2 or 4 words.

A2	A1	A0	BURST LENGTH
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	Reserved
1	×	×	Reserved

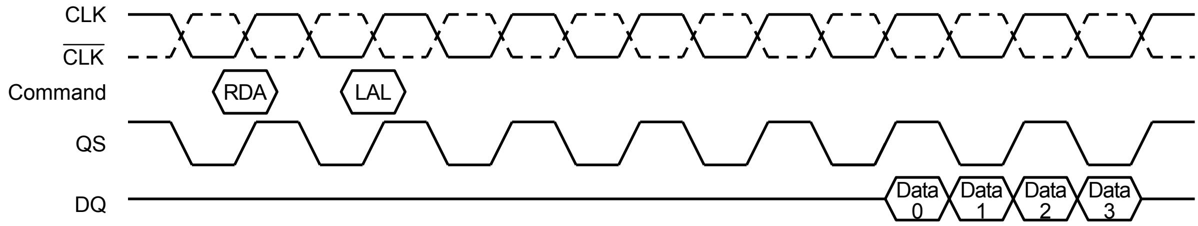
(R-2) Burst Type field (A3)

The Burst Type can be chosen Interleave mode or Sequential mode. When the A3 bit is “0”, Sequential mode is selected. When the A3 bit is “1”, Interleave mode is selected. Both burst types support burst length of 2 and 4 words.

A3	BURST TYPE
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode (A3)
  A column access is started from the inputted lower address and is performed by incrementing the lower address input to the device

$\overline{CAS}$ Latency = 4 (Free Running QS mode)



Addressing sequence for Sequential mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is LA0) not carried from LA0~LA1 (Data 0–Data 1)
Data 1	n + 1	
Data 2	n + 2	4 words (address bits is LA1, LA0) not carried from LA1~LA2 (Data 0–Data 3)
Data 3	n + 3	

- Addressing sequence of Interleave mode
  A column access is started from the inputted lower address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	···A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words (Data 0–Data 1)
Data 1	···A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words (Data 0–Data 3)
Data 3	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	

(R-3) $\overline{CAS}$ Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the LAL command following the RDA command to the first data read. The minimum value of $\overline{CAS}$ Latency depends on the frequency of CLK. In a write mode, the place of clock that should input write data is $\overline{CAS}$ Latency cycles − 1.

A6	A5	A4	$\overline{CAS}$ LATENCY
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

(R-4) Test Mode field (A7)

This bit is used to enter Test Mode for supplier only and must be set to “0” for normal operation.

(R-5) Reserved field in the Regular Mode Register

- Reserved bits (A8 to A13)
  These bits are reserved for future operations. They must be set to “0” for normal operation.

Extended Mode Register fields

(E-1) DLL Switch field (A0)

This bit is used to enable DLL. When the A0 bit is set “0”, DLL is enabled. This bit must be set to “0” for normal operation.

(E-2) Output Driver Impedance Control field (A1 to A4)

This field is used to choose Output Driver Strength. Three types of Driver Strength are supported. QS and DQ Driver Strength can be chosen separately. A2-A1 specified the DQ Driver Strength. A4-A3 specified the QS Driver Strength.

QS		DQ		OUTPUT DRIVER IMPEDANCE CONTROL
A4	A3	A2	A1	
0	0	0	0	Normal Output Driver
0	1	0	1	Strong Output Driver
1	0	1	0	Weak Output Driver
1	1	1	1	Reserved

(E-3) Strobe Select (A6 / A5)

Two types of data strobe are supported. This field is used to choose the type of data strobe.

(1) Unidirectional DS/QS mode

Data strobe is separated DS for write strobe and QS for read strobe.

DS is used to sample write data at write operation. QS is aligned with read data at Read operation.

(2) Unidirectional DS/Free running QS mode

Data strobe is separated DS for write strobe and QS for read strobe.

DS is used to sample write data at write operation. QS is aligned with read data and always clocking.

A6	A5	STROBE SELECT
0	0	Reserved
0	1	Reserved
1	0	Unidirectional DS/QS mode
1	1	Unidirectional DS/Free running QS mode

(E-4) Reserved field (A7 to A13)

These bits are reserved for future operations and must be set to “0” for normal operation.

BOUNDARY SCAN TEST ACCESS PORT OPERATIONS

The TC59LM836DKB has a serial boundary scan test access port (TAP) which is compatible with IEEE Standard 1149.1 – 1990, but which does not implement all the functions required for 1149.1 – 1990. TCK must be tied to V_{SS} or V_{DD} to disable the TAP when TAP operation is not required.

Test Access Port Signals

SYMBOL	DESCRIPTION	
TCK	Test Clock Input	All Test Access Port inputs are sampled on the rising edge of TCK. To disable the TAP, TCK must be tied to V_{SS} or V_{DD}.
TMS	Test Mode Select Input	The signal presented at TMS is sampled on the rising edge of TCK. This input is internally pulled up so as to recognize a floating input as a logical High (Test-Logic-Reset).
TDI	Test Data Input	Values presented at TDI are clocked into the selected register on the rising edge of TCK. This input is internally pulled up. This enables detection of when the TDI input to the board is open-circuit.
TDO	Test Data Output	TDO is the serial output for test instructions and data from the test logic. This output is controlled by the falling edge of TCK.

Test Access Port Registers

REGISTER		SYMBOL	LENGTH (bits)	DESCRIPTION
Instruction Register		IR [2 : 0]	3	The Instruction register controls five states (EXTEST, Sample-Z, Sample, Bypass, ID code).
Test Data Register				
	ID Register	IDR [31 : 0]	32	The register includes information on revision number, organization and TOSHIBA ID number.
	Bypass Register	BR	1	The register connects TDI and TDO.
	Boundary Scan Register	BSR [62 : 0]	63	The Boundary Scan register is comprised of boundary scan cells at each input and I/O pin. The BSCs are serially connected between TDI and TDO.

TAP Controller Instruction Set

IR2	IR1	IR0	INSTRUCTION	DESCRIPTION
0	0	0	EXTEST	Moves the Preloaded data on to the output pins. Samples the inputs connected to the BSCs.
0	0	1	ID CODE	Access ID code.
0	1	0	SAMPLE – Z	Tristates the RAM outputs and samples the inputs connected to the BSCs.
0	1	1	RESERVED	This instruction is reserved for future use.
1	0	0	SAMPLE	Samples the inputs connected to the BSCs. Load the sampled data at I/Os to the parallel output of the BSCs. Does not affect RAM operation.
1	0	1	RESERVED	This instruction is reserved for future use.
1	1	0	RESERVED	This instruction is reserved for future use.
1	1	1	BYPASS	Bypasses TDI and TDO using the Bypass register.

Note: The first bit to be scanned into TDI is taken to be the least significant bit (IR0).

ID Register

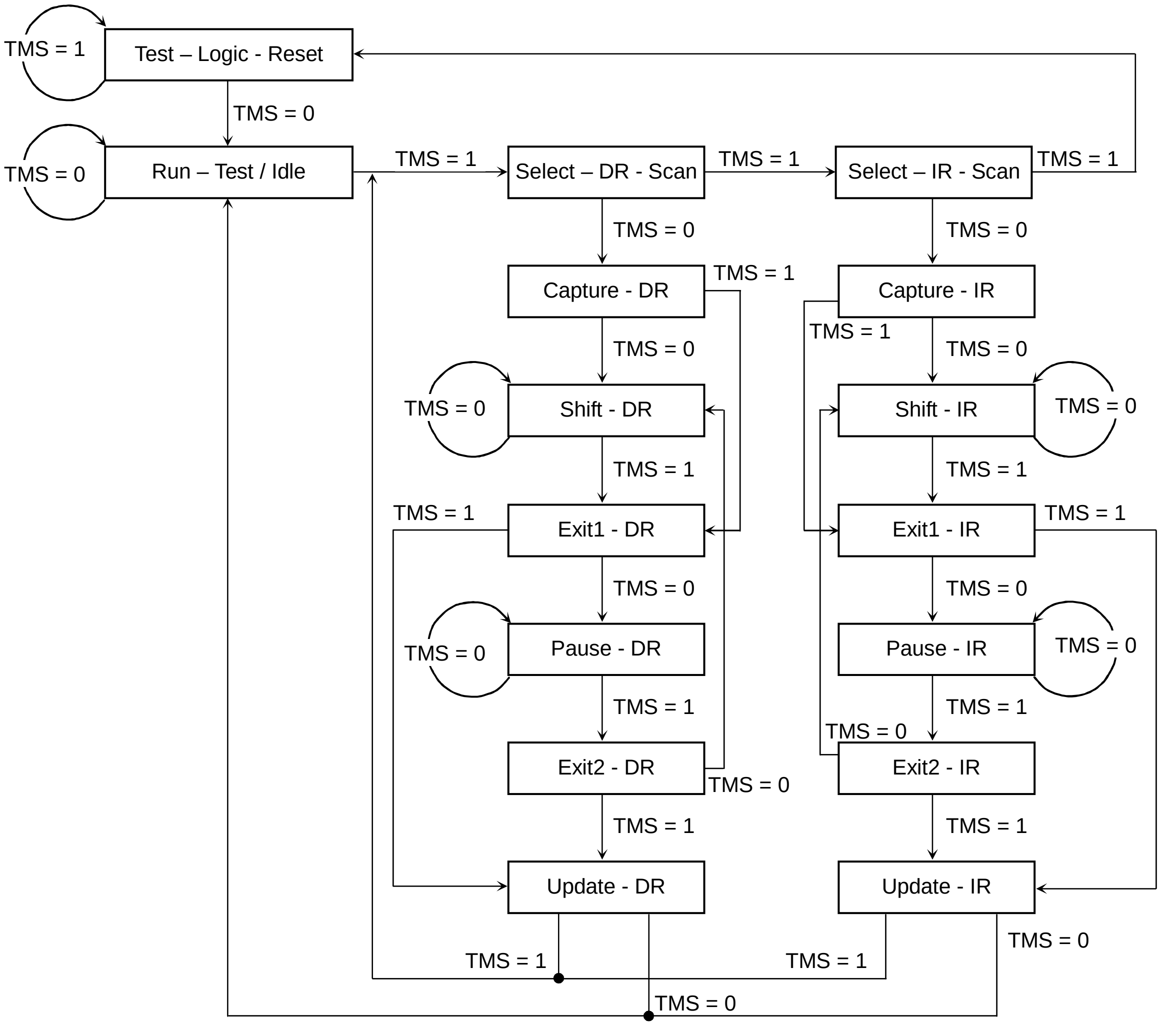
BIT #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	1
Content	Memory Type																				TOSHIBA ID number											Fixed

Boundary Scan Order

BIT	BALL LAYOUT	BALL NAME
0	U10	DQ35
1	U11	DQ34
2	T10	DQ33
3	T11	DQ32
4	R10	DQ31
5	R11	DQ30
6	P10	DQ29
7	P11	DQ28
8	N10	DQ27
9	N11	UQS
10	M3	A4
11	M11	A3
12	L10	A2
13	L11	A1
14	K10	A0
15	K11	A10
16	J10	BA1
17	J11	BA0
18	G10	A13
19	G11	FN
20	H10	/CS
21	F11	LQS
22	F10	DQ8
23	E11	DQ7
24	E10	DQ6
25	D11	DQ5
26	D10	DQ4
27	C11	DQ3
28	C10	DQ2
29	B11	DQ1

BIT	BALL LAYOUT	BALL NAME
30	B10	DQ0
31	B3	DQ17
32	B2	DQ16
33	C3	DQ15
34	C2	DQ14
35	D3	DQ13
36		
37	D2	DQ12
38	E3	DQ11
39	E2	DQ10
40	F3	DQ9
41	F2	LDS
42	G3	/CLK
43	H3	CLK
44	H2	/PD
45	J2	A12
46	J3	A11
47	K2	A9
48	K3	A8
49	L2	A7
50	L3	A6
51	M2	A5
52	N2	UDS
53	N3	DQ26
54	P2	DQ25
55	P3	DQ24
56	R2	DQ23
57		
58	R3	DQ22
59	T2	DQ21
60	T3	DQ20
61	U2	DQ19
62	U3	DQ18

TAP CONTROLLER STATE DIAGRAM



Notes:

1. To enter the Test-Logic-Reset state in order to initialize the device, keep TMS High for at least five rising edges of the TCK.
2. The TDO output buffer is active only during shift operations (the Shift-DR and Shift-IR states) and is inactive (High-Z) during other states.

TAP DC OPERATING CHARACTERISTICS

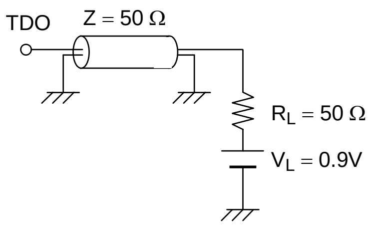
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LO}	Output Leakage Current (TDO pin)	Output Deselected V_{OUT}=0 to V_{DD}	−10	—	10	μA
I_I	Input Leakage Current (TCK, TMS, TDI pins)	V_{IN} = 1.7V to V_{DD}	−20	—	10	μA
		V_{IN} = 0 to 0.7V	−100	—	10	μA
V_{IH}	Input High Voltage (TCK, TMS, TDI pins)	—	V_{REF}+0.4	—	V_{DD}+0.2	V
V_{IL}	Input Low Voltage (TCK, TMS, TDI pins)	—	−0.1	—	V_{REF}−0.4	V
V_{OH}	Output High Voltage (TDO pin)	I_{OH} = −2 mA	1.5	—	V_{DD}	V
V_{OL}	Output Low Voltage (TDO pin)	I_{OL} = 2 mA	—	—	0.45	V

AC CHARACTERISTICS (V_{DD} = 2.5V ± 0.125V, V_{DDQ} = 1.4V ~ 1.9V, T_{CASE} = 0 ~ 85°C)

SYMBOL	PARAMETER	TC59LM836DKB		UNIT
		MIN	MAX	
t_{THTH}	TCK Cycle Time	50	—	ns
t_{THTL}	TCK High Pulse Width	20	—	
t_{TLTH}	TCK Low Pulse Width	20	—	
t_{MVTH}	TMS Setup Time to TCK	10	—	
t_{THMX}	TMS Hold Time to TCK	10	—	
t_{CS}	Capture Setup time to TCK	10	—	
t_{CH}	Capture Hold time to TCK	10	—	
t_{DVTH}	TDI Setup Time to TCK	10	—	
t_{THDX}	TDI Hold Time to TCK	10	—	
t_{TLQV}	Output Valid Time from TCK Low	—	20	
t_{TLQX}	Output Hold Time from TCK Low	0	—	
t_{TLQLZ}	Output Low-Z Time from TCK Low	5	—	
t_{TLQHZ}	Output High-Z Time from TCK Low	—	5	

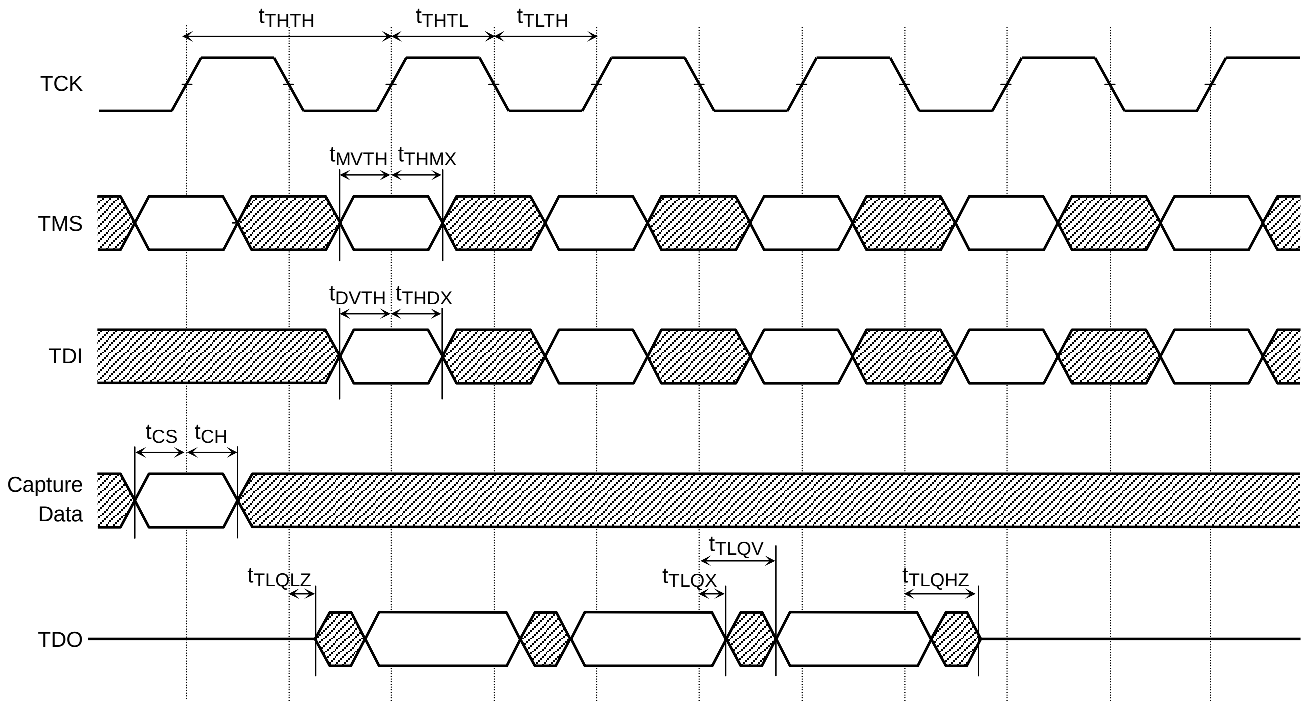
TAP AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	1.8V / 0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	0.9V
Output Timing Measurement Reference Level	0.9V



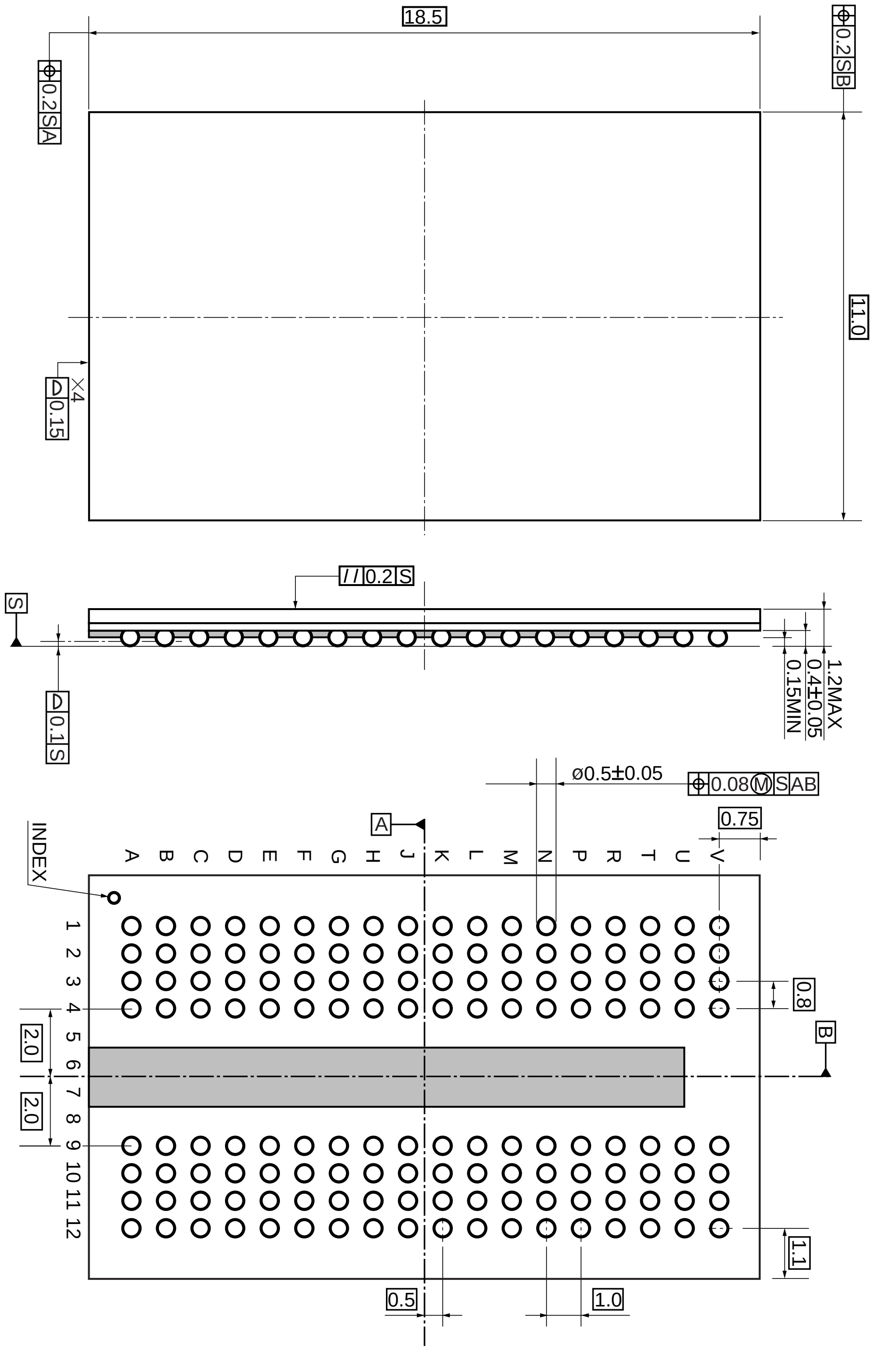
Output Load

TAP TIMING DIAGRAMS



PACKAGE DIMENSIONS

P-TFBGA144-1119-0.80BZ



Weight: 0.30g (typ.)

REVISION HISTORY

– Rev.1.0 (Feb. 26 '2004)

– Rev.1.1 (May. 25 '2004)

- I_{DD6} spec changed from 10mA to 15mA (page 1, 7)
- V_{SWING} in AC Test conditions changed from 0.7 V to 0.8 V (page 11)
- Corrected typo (page 54)

– Rev.1.2 (Aug. 27 '2004)

- Some notes in the page 8 moved to page 7 (page 7, 8).
- Note 2 changed as below (page 7).

  Before: These parameters depend on the output loading. The specified values are obtained with the output open

  After: These parameters define the current between V_{DD} and V_{SS}.

- Corrected TYPO (page 9, 14~18, 61, 62).
- $t_{CK,MAX}$ for "-30" changed from 7.5 ns to 5.0 ns (page 9)
- Package drawing minor change (page 63).
- Package weight (0.30g) added (page 63)

– Rev.1.3 (Mar.7 '2005)

- Corrected figure of l_{PDA} based AC timing spec table (page 12, 43, 44, 50, 51).

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