19-0656; Rev 1; 3/07

EVALUATION KIT AVAILABLE

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

General Description

The MAX16809/MAX16810 are integrated, high-efficiency white or RGB LED drivers. They are designed for LCD backlighting and other LED lighting applications with multiple strings of LEDs. The MAX16809/MAX16810's current-mode PWM controller regulates the necessary voltage to the LED array. Depending on the input voltage and LED voltage range, it can be used with boost or buck-boost (SEPIC) topologies.

The MAX16809/MAX16810 LED drivers include 16 open-drain, constant-current-sinking LED driver outputs rated for 36V continuous operation. The LED current-control circuitry achieves ±3% current matching among strings and enables paralleling of outputs for LED string currents higher than 55mA. The output-enable pin is used for simultaneous PWM dimming of all output channels. Dimming frequency range is 50Hz to 30kHz and dimming ratio is up to 5000:1. The constant-current outputs are single resistor programmable and the LED current can be adjusted up to 55mA per output channel.

The MAX16809/MAX16810 operate either in stand-alone mode or with a microcontroller (µC) using an industry-standard, 4-wire serial interface. The MAX16810 includes a watchdog and circuitry that automatically detects open-circuit LEDs.

The MAX16809/MAX16810 include overtemperature protection, operate over the full -40°C to +125°C temperature range, and are available in a 5mm x 7mm thermally enhanced, 38-pin TQFN exposed paddle package.

Pin Configuration appears at end of data sheet.

Features

- **16 Constant-Current Output Channels (Up to 55mA Each)**
- **±3% Current Matching Among Outputs**
- **Paralleling Channels Allows Higher Current per LED String**
- **Outputs Rated for 36V Continuous Voltage**
- **Output-Enable Pin for PWM Dimming (Up to 30kHz)**
- **One Resistor Sets LED Current for All Channels**
- **Wide Dimming Ratio Up to 5000:1**
- **Low Current-Sense Reference (300mV) for High Efficiency**
- **8V to 26.5V Input Voltage or Higher with External Biasing Devices**
- **Open LED Detection and Watchdog Timer (MAX16810)**
- **4-Wire Serial Interface to Control Individual Output Channels**

Applications

LCD White or RGB LED Backlighting:
LCD TVs, Desktop, and Notebook Panels
Automotive Navigation, Heads-Up, and Infotainment Displays
Industrial and Medical Displays

Ambient, Mood, and Accent Lighting

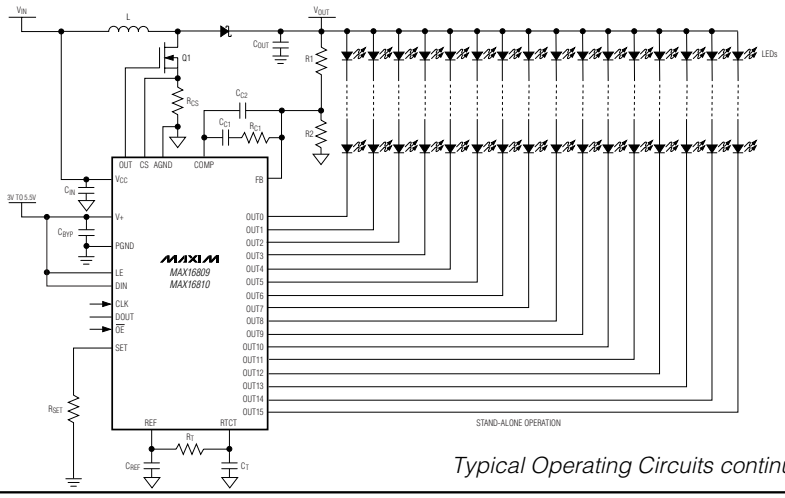
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX16809ATU+	-40°C to +125°C	38 TQFN-EP*	T3857-1
MAX16810ATU+	-40°C to +125°C	38 TQFN-EP*	T3857-1

+Denotes a lead-free package.

**EP = Exposed paddle.*

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND .....-0.3V to +30V
Current into V_{CC} (V_{CC} > 24V) 30mA
V+ to PGND .....-0.3V to +6V
OUT to AGND .....-0.3V to (V_{CC} + 0.3V)
OUT Current (10µs duration) .....±1A
FB, COMP, CS, RTCT, REF to AGND .....-0.3V to +6V
COMP Sink Current 10mA
OUT0–OUT15 to PGND .....-0.3V to +40V
DIN, CLK, LE, $\overline{OE}$, SET to PGND .....-0.3V to (V+ + 0.3V)
DOUT Current .....±10mA
OUT0–OUT15 Sink Current 60mA
Total PGND Current (1s pulse time) 960mA
Continuous Power Dissipation (T_A = +70°C)
38-Pin TQFN (derate 35.7mW/°C* above +70°C) 2857mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**Per JEDEC51 Standard (Multilayer Board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (PWM CONTROLLER)

(V_{CC} = +15V, V+ = +3V to +5.5V referenced to PGND, R_T = 10kΩ, C_T = 3.3nF, REF = open, COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND, AGND = PGND = 0V; all voltages are measured with respect to AGND, unless otherwise noted. T_J = T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Output Voltage	V_{REF}	I_{REF} = 1mA, T_J = +25°C	4.95	5	5.05	V
Line Regulation	ΔV_{LINE}	12V< V_{CC} < 25V, I_{REF} = 1mA		0.4	4	mV
Load Regulation	ΔV_{LOAD}	1mA < I_{REF} < 20mA		6	50	mV
Total Output-Voltage Variation	V_{REFT}	(Note 2)	4.875		5.125	V
Output Noise Voltage	V_{NOISE}	10Hz < f < 10kHz		50		µV
Output Short-Circuit Current	I_{SHORT}	V_{REF} = 0V	30		180	mA
OSCILLATOR						
Initial Accuracy		T_J = +25°C	51	54	57	kHz
Voltage Stability		12V < V_{CC} < 25V		0.2	0.5	%
Temperature Stability				1		%
RTCT Ramp Peak-to-Peak				1.7		V
RTCT Ramp Valley				1.1		V
Discharge Current	I_{DIS}	V_{RTCT} = 2V, T_J = +25°C	7.9	8.3	8.7	mA
		V_{RTCT} = 2V, -40°C ≤ T_J ≤ +125°C	7.5	8.3	9.0	
Frequency Range	f_{OSC}		20		1000	kHz
ERROR AMPLIFIER						
FB Input Voltage	V_{FB}	FB shorted to COMP	2.45	2.5	2.55	V
Input Bias Current	$I_{B(FB)}$			-0.01	-0.1	µA
Open-Loop Gain	A_{VOL}	2V ≤ V_{COMP} ≤ 4V		100		dB
Unity-Gain Bandwidth	f_{GBW}			1		MHz
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V	60	80		dB
COMP Sink Current	I_{SINK}	V_{FB} = 2.7V, V_{COMP} = 1.1V	2	6		mA
COMP Source Current	I_{SOURCE}	V_{FB} = 2.3V, V_{COMP} = 5V	0.5	1.2	1.8	mA
COMP Output-Voltage High	V_{OH}	V_{FB} = 2.3V, R_{COMP} = 15kΩ to AGND	5	5.8		V
COMP Output-Voltage Low	V_{OL}	V_{FB} = 2.7V, R_{COMP} = 15kΩ to V_{REF}		0.1	1.1	V

ELECTRICAL CHARACTERISTICS (PWM CONTROLLER) (continued)

(V_{CC} = +15V, V+ = +3V to +5.5V referenced to PGND, R_T = 10kΩ, C_T = 3.3nF, REF = open, COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND, AGND = PGND = 0V; all voltages are measured with respect to AGND, unless otherwise noted. T_J = T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIER							
Current-Sense Gain	A_{CS}	(Notes 3, 4)		2.85	3	3.40	V/V
Maximum Current-Sense Signal	V_{CS_MAX}	(Note 3)		0.275	0.300	0.325	V
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V			70		dB
Current-Sense Input Bias Current	I_{CS}	V_{COMP} = 0V			-1	-2.5	µA
Current Sense to OUT Delay	t_{PWM}	50mV overdrive			60		ns
MOSFET DRIVER							
OUT Low-Side On-Resistance	V_{RDS_ONL}	I_{SINK} = 200mA	T_J = -40°C to +85°C (Note 2)		4.5	10	Ω
			T_J = -40°C to +125°C		4.5	12	
OUT High-Side On-Resistance	V_{RDS_ONH}	I_{SOURCE} = 100mA	T_J = -40°C to +85°C (Note 2)		3.5	7.5	Ω
			T_J = -40°C to +125°C		3.5	10	
Source Current (Peak)	I_{SOURCE}	C_{LOAD} = 10nF			2		A
Sink Current (Peak)	I_{SINK}	C_{LOAD} = 10nF			1		A
Rise Time	t_R	C_{LOAD} = 1nF			15		ns
Fall Time	t_F	C_{LOAD} = 1nF			22		ns
UNDERVOLTAGE LOCKOUT/STARTUP							
Startup Voltage Threshold	V_{CC_START}			7.98	8.4	8.82	V
Minimum Operating Voltage After Turn-On	V_{CC_MIN}			7.1	7.6	8.0	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYST}$				0.8		V
PULSE-WIDTH MODULATION (PWM)							
Maximum Duty Cycle	D_{MAX}			94.5	96	97.5	%
Minimum Duty Cycle	D_{MIN}					0	%
SUPPLY CURRENT							
Startup Supply Current	I_{START}	V_{CC} = 7.5V			32	65	µA
Operating Supply Current	I_{CC}	V_{FB} = V_{CS} = 0V			3	5	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25mA		24	26.5		V

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ELECTRICAL CHARACTERISTICS (LED DRIVER)

(V+ = +3V to +5.5V, AGND = PGND = 0V; all voltages are measured with respect to PGND, unless otherwise noted. $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		3.0		5.5	V
Output Voltage	$V_{OUT\_\_}$				36	V
Standby Current (Interface Idle, All Output Ports High Impedance)		R_{SET} = 360Ω, DIN, LE, CLK = PGND or V+, $\overline{OE}$ = V+, DOUT unconnected		3.6	4.5	mA
Standby Current (Interface Active, All Output Ports High Impedance)		R_{SET} = 360Ω, f_{CLK} = 5MHz, $\overline{OE}$ = V+, DIN, LE = PGND or V+, DOUT unconnected		3.8	4.8	mA
Supply Current (Interface Idle, All Output Ports Active Low)	I+	R_{SET} = 360Ω, $\overline{OE}$ = PGND, DIN, LE = V+, DOUT unconnected		30	52.5	mA
INTERFACE (DIN, CLK, DOUT, LE, $\overline{OE}$)						
Input-Voltage High (DIN, CLK, LE, $\overline{OE}$)	V_{IH}		0.7 x V+			V
Input-Voltage Low (DIN, CLK, LE, $\overline{OE}$)	V_{IL}				0.3 x V+	V
Hysteresis Voltage (DIN, CLK, LE, $\overline{OE}$)	V_{HYST}			0.8		V
Input Leakage Current (DIN, CLK)	I_{LEAK}		-1		+1	µA
$\overline{OE}$ Pullup Current to V+	$I_{\overline{OE}}$	V+ = 5.5V, $\overline{OE}$ = PGND	0.25	1.5	25	µA
LE Pulldown Current to PGND	I_{LE}	V+ = 5.5V, LE = V+	0.25	1.5	25	µA
Output-Voltage High (DOUT)	V_{OH}	I_{SOURCE} = 4mA	V+ - 0.5V			V
Output-Voltage Low (DOUT)	V_{OL}	I_{SINK} = 4mA			0.5	V
OUT_ _ Output Current	$I_{OUT\_\_}$	0°C ≤ T_A ≤ +125°C, V_{OUT} = 1V to 2.5V, R_{SET} = 360Ω	43.25	47.5	51.75	mA
		T_A = -40°C, V_{OUT} = 1V to 2.5V, R_{SET} = 360Ω	40		55	
OUT_ _ Leakage Current		$\overline{OE}$ = V+			1	µA
OUT_ _ Fault Detection Threshold (MAX16810)	V_{OUTTH}	V+ = 5.5V, $\overline{OE}$ = V+		0.8		V
Watchdog Timeout Period (MAX16810)	t_{WD}	V+ = 5.5V	0.1	1	2.5	s

5V TIMING CHARACTERISTICS

(V+ = +4.5V to +5.5V, AGND = PGND = 0V; all voltages are measured with respect to PGND, unless otherwise noted. $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 5)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INTERFACE TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		40			ns
CLK Pulse-Width High	t_{CH}		19			ns
CLK Pulse-Width Low	t_{CL}		19			ns
DIN Setup Time	t_{DS}		4			ns
DIN Hold Time	t_{DH}		8			ns
DOUT Propagation Delay	t_{DO}		10		50	ns
DOUT Rise Time	t_{DR}	C_{DOUT} = 10pF, 20% to 80%			10	ns
DOUT Fall Time	t_{DF}	C_{DOUT} = 10pF, 80% to 20%			10	ns
LE Pulse-Width High	t_{LW}		20			ns
LE Setup Time	t_{LS}		15			ns
LE Rising to OUT_ _ Rising Delay	t_{LRR}	(Note 6)			110	ns
LE Rising to OUT_ _ Falling Delay	t_{LRF}	(Note 6)			340	ns
CLK Rising to OUT_ _ Rising Delay	t_{CRR}	(Note 6)			110	ns
CLK Rising to OUT_ _ Falling Delay	t_{CRF}	(Note 6)			340	ns
$\overline{OE}$ Rising to OUT_ _ Rising Delay	$t_{\overline{OE}R}$	(Note 6)			110	ns
$\overline{OE}$ Falling to OUT_ _ Falling Delay	$t_{\overline{OE}F}$	(Note 6)			340	ns
OUT_ _ Turn-On Fall Time	t_F	80% to 20% (Note 6)			210	ns
OUT_ _ Turn-Off Rise Time	t_R	20% to 80% (Note 6)			130	ns

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3.3V TIMING CHARACTERISTICS

(V+ = +3V to < +4.5V, AGND = PGND = 0V; all voltages are measured with respect to PGND, unless otherwise noted. $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 5)

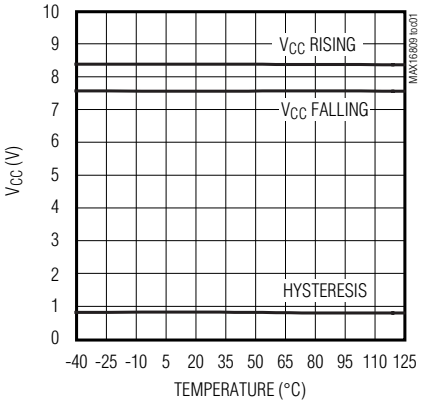
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERFACE TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		52			ns
CLK Pulse-Width High	t_{CH}		24			ns
CLK Pulse-Width Low	t_{CL}		24			ns
DIN Setup Time	t_{DS}		4			ns
DIN Hold Time	t_{DH}		8			ns
DOUT Propagation Delay	t_{DO}		12		70	ns
DOUT Rise Time	t_{DR}	C_{DOUT} = 10pF, 20% to 80%			12	ns
DOUT Fall Time	t_{DF}	C_{DOUT} = 10pF, 80% to 20%			12	ns
LE Pulse-Width High	t_{LW}		20			ns
LE Setup Time	t_{LS}		15			ns
LE Rising to OUT_ _ Rising Delay	t_{LRR}	(Note 6)			140	ns
LE Rising to OUT_ _ Falling Delay	t_{LRF}	(Note 6)			400	ns
CLK Rising to OUT_ _ Rising Delay	t_{CRR}	(Note 6)			140	ns
CLK Rising to OUT_ _ Falling Delay	t_{CRF}	(Note 6)			400	ns
$\overline{OE}$ Rising to OUT_ _ Rising Delay	$t_{\overline{OE}R}$	(Note 6)			140	ns
$\overline{OE}$ Falling to OUT_ _ Falling Delay	$t_{\overline{OE}F}$	(Note 6)			400	ns
OUT_ _ Turn-On Fall Time	t_F	80% to 20% (Note 6)			275	ns
OUT_ _ Turn-Off Rise Time	t_R	20% to 80% (Note 6)			150	ns

Note 1: All devices are 100% production tested at T_J = +25°C and +125°C. Limits to -40°C are guaranteed by design.
Note 2: Guaranteed by design, not production tested.
Note 3: Parameter is measured at trip point of latch with V_{FB} = 0V.
Note 4: Gain is defined as $A = \Delta V_{COMP} / \Delta V_{CS}$, $0.05V \le V_{CS} \le 0.25V$.
Note 5: See Figures 3 and 4.
Note 6: A 65Ω pullup resistor is connected from OUT_ _ to 5.5V. Rising refers to $V_{OUT\_\_}$ when current through OUT_ _ is turned off and falling refers to $V_{OUT\_\_}$ when current through OUT_ _ is turned on.

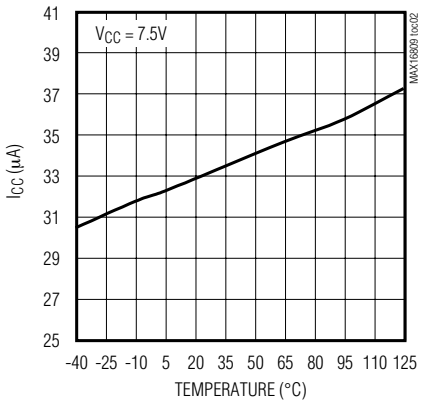
Typical Operating Characteristics

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND = PGND = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

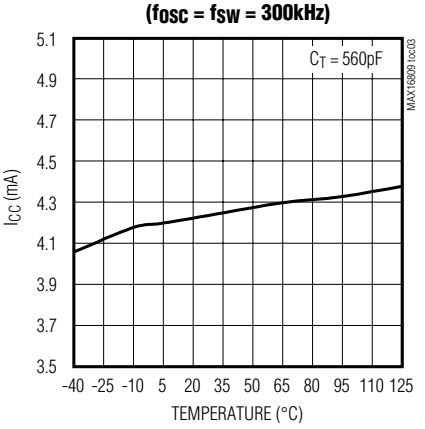
BOOTSTRAP UVLO vs. TEMPERATURE



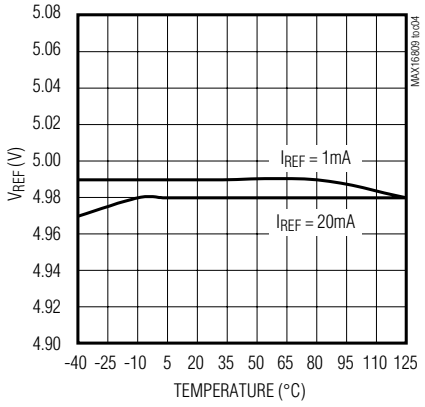
STARTUP CURRENT vs. TEMPERATURE



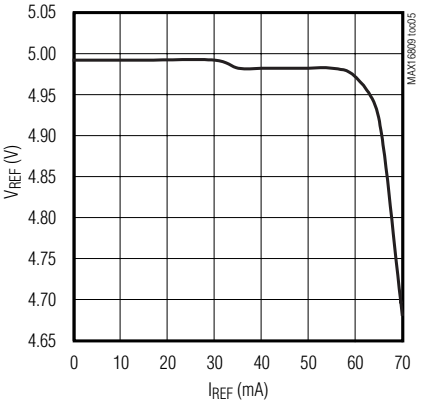
OPERATING SUPPLY CURRENT vs. TEMPERATURE AFTER STARTUP (f_{OSC} = f_{SW} = 300kHz)



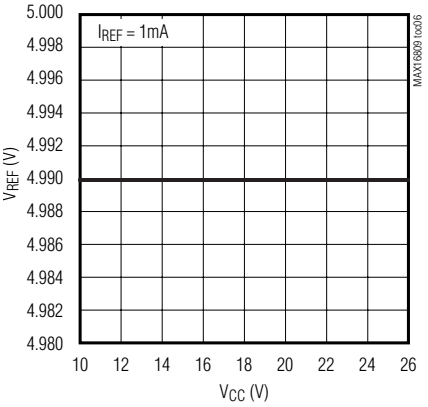
REFERENCE VOLTAGE vs. TEMPERATURE



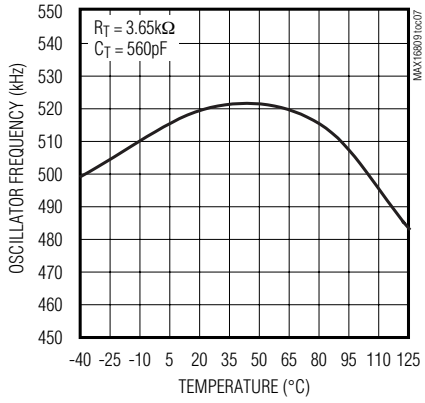
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



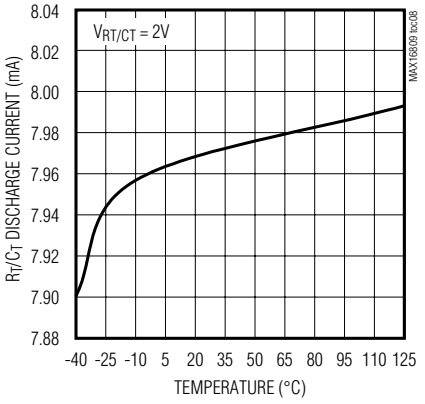
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



OSCILLATOR FREQUENCY (f_{OSC}) vs. TEMPERATURE



OSCILLATOR R_T/C_T DISCHARGE CURRENT vs. TEMPERATURE

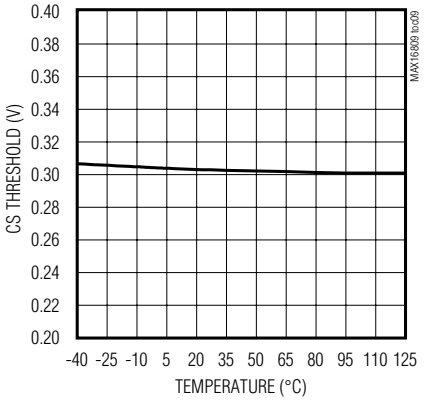


Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

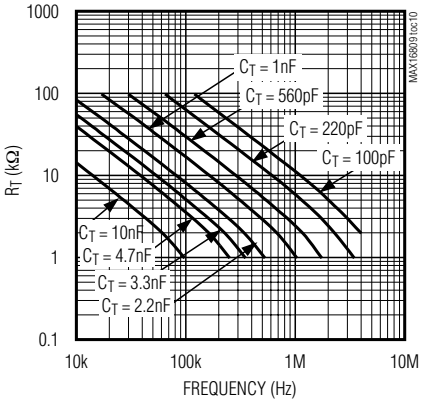
Typical Operating Characteristics (continued)

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND = PGND = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

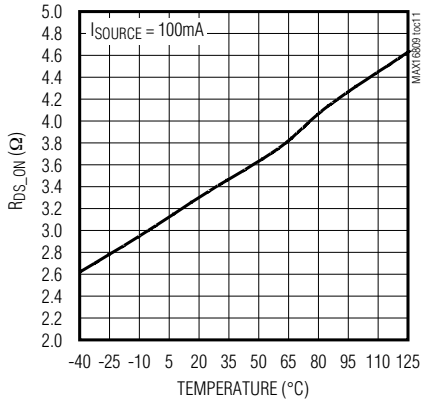
CURRENT-SENSE TRIP THRESHOLD vs. TEMPERATURE



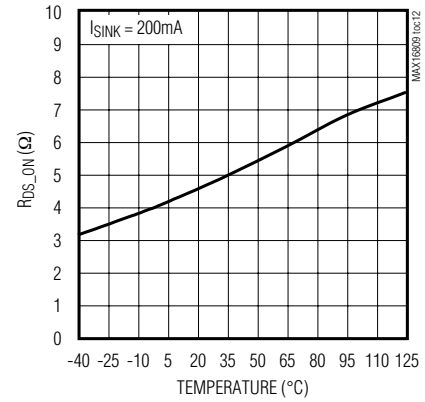
TIMING RESISTANCE vs. OSCILLATOR FREQUENCY



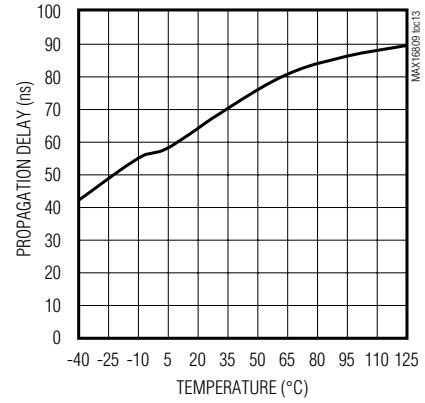
OUT IMPEDANCE vs. TEMPERATURE (R_{DS_ON} PMOS DRIVER)



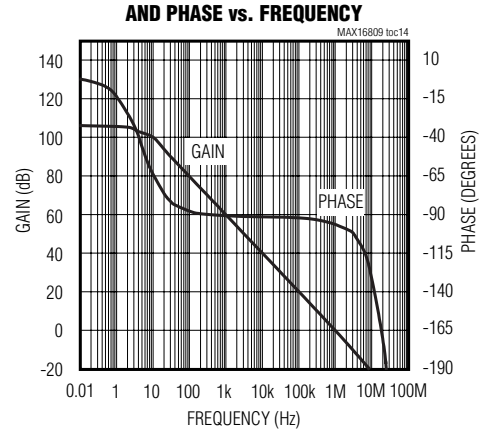
OUT IMPEDANCE vs. TEMPERATURE (R_{DS_ON} NMOS DRIVER)



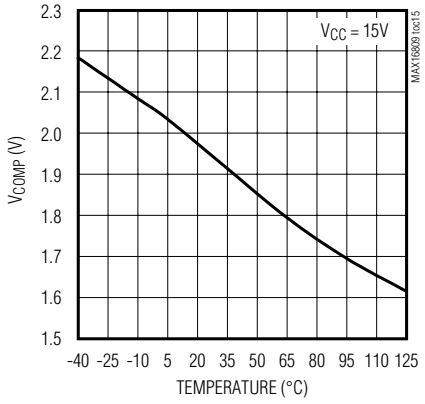
PROPAGATION DELAY FROM CURRENT-LIMIT COMPARATOR TO OUT vs. TEMPERATURE



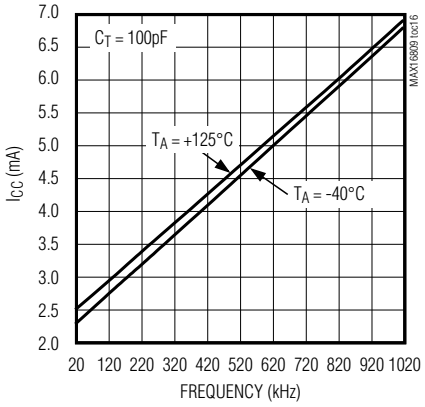
ERROR-AMPLIFIER OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



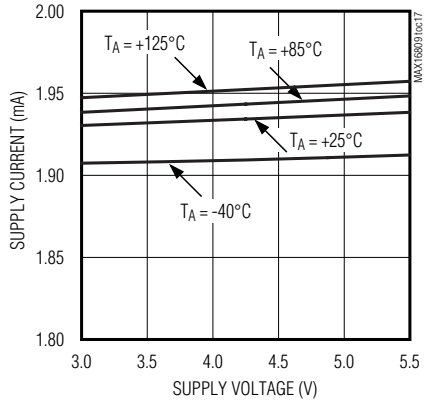
COMP VOLTAGE LEVEL TO TURN OFF DEVICE vs. TEMPERATURE



SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



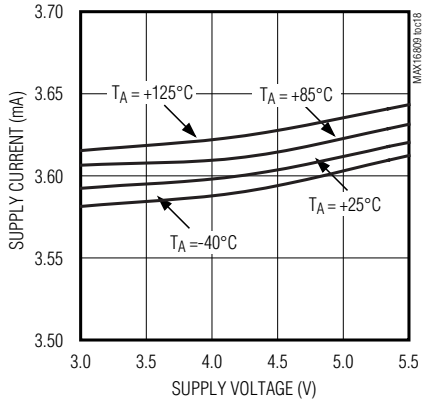
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS OFF, R_{SET} = 720Ω)



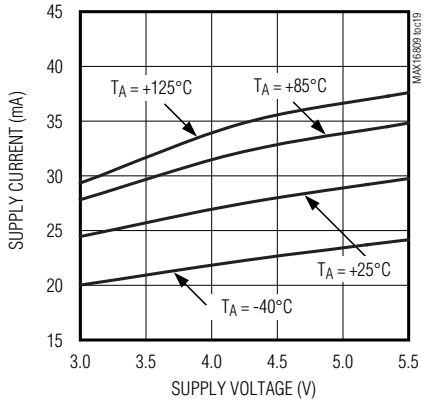
Typical Operating Characteristics (continued)

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND = PGND = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

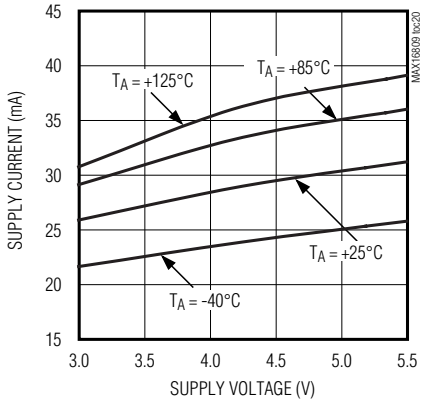
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS OFF, R_{SET} = 360Ω)



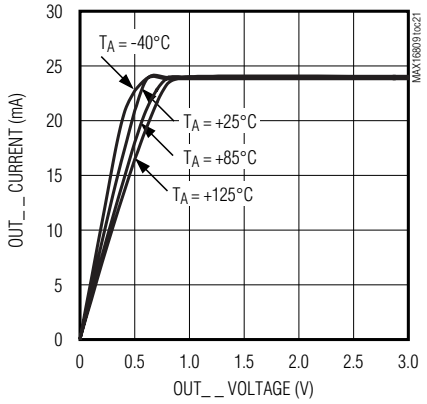
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS ON, R_{SET} = 720Ω)



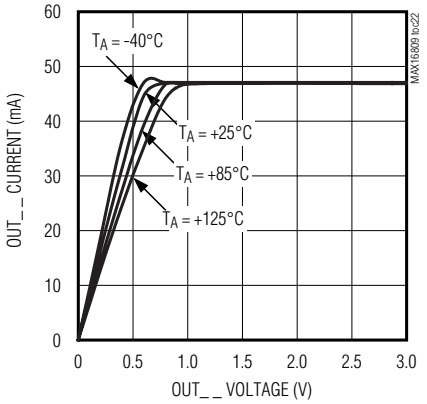
SUPPLY CURRENT vs. SUPPLY VOLTAGE (INTERFACE IDLE, ALL OUTPUTS ON, R_{SET} = 360Ω)



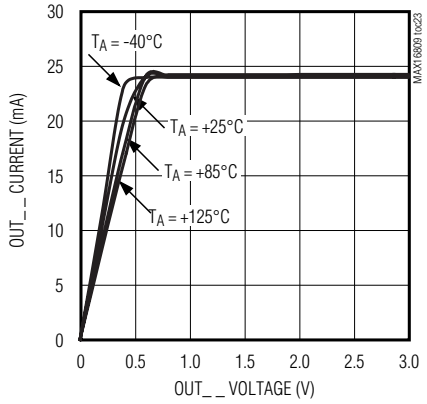
OUT_ _ CURRENT vs. OUT_ _ VOLTAGE (R_{SET} = 720Ω, V+ = 3.3V)



OUT_ _ CURRENT vs. OUT_ _ VOLTAGE (R_{SET} = 360Ω, V+ = 3.3V)



OUT_ _ CURRENT vs. OUT_ _ VOLTAGE (R_{SET} = 720Ω, V+ = 5.0V)

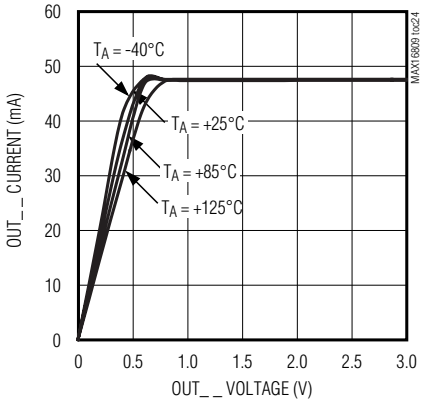


Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

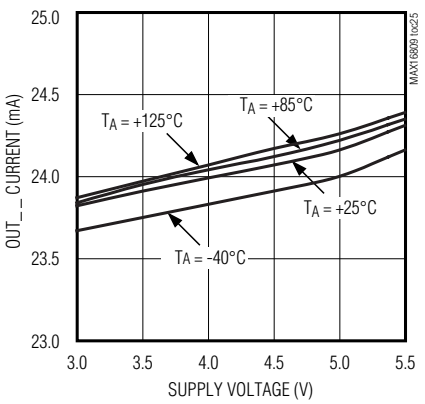
Typical Operating Characteristics (continued)

(V_{CC} = +15V, V+ = 3V to 5.5V, R_T = 10kΩ, C_T = 3.3nF, V_{REF} = COMP = open, C_{REF} = 0.1µF, V_{FB} = 2V, CS = AGND = PGND = 0V. Typical values are at T_A = +25°C, unless otherwise noted.)

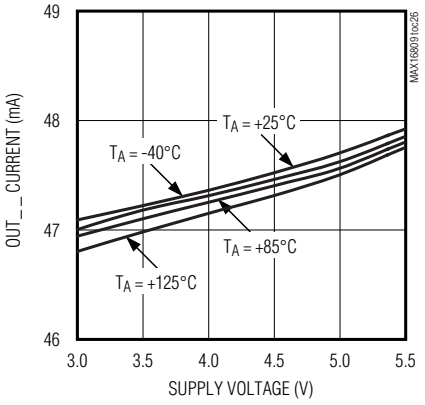
OUT_ _ CURRENT vs. OUT_ _ VOLTAGE (R_{SET} = 360Ω V+ = 5.0V)



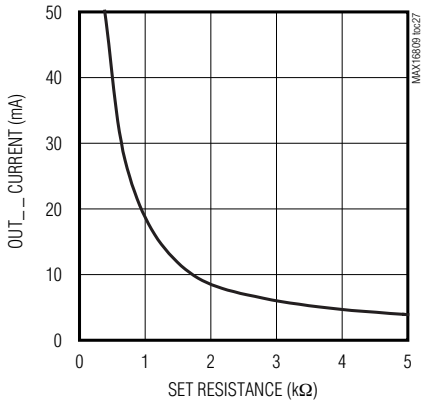
OUT_ _ CURRENT vs. V+ (R_{SET} = 720Ω, V_{OUT} = 2V)



OUT_ _ CURRENT vs. V+ (R_{SET} = 360Ω, V_{OUT} = 2V)



OUT_ _ CURRENT vs. SET RESISTANCE (V+ = 5.0V)



Pin Description

PIN	NAME	FUNCTION
1, 31, 32, 36, 38	N.C.	No Connection. Not internally connected. Leave unconnected.
2	FB	Error-Amplifier Inverting Input
3	COMP	Error-Amplifier Output
4–11	OUT8–OUT15	LED Driver Outputs. OUT8–OUT15 are open-drain, constant-current-sinking outputs rated for 36V.
12	$\overline{OE}$	Active-Low, Output Enable Input. Drive $\overline{OE}$ low to PGND to enable the OUT0–OUT15. Drive $\overline{OE}$ high to disable OUT0–OUT15.
13	DOUT	Serial-Data Output. Data is clocked out of the 16-bit internal shift register to DOUT on CLK's rising edge.
14	SET	LED Current Setting. Connect R_{SET} from SET to PGND to set the LED current.
15	V+	LED Driver Positive Supply Voltage. Bypass V+ to PGND with a 0.1µF ceramic capacitor.
16, 17	PGND	Power Ground
18	DIN	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
19	CLK	Serial-Clock Input
20	LE	Latch-Enable Input. Data is loaded transparently from the internal shift register(s) to the output latch(es) while LE is high. Data is latched into the output latch(es) on LE's falling edge, and retained while LE is low.
21–28	OUT0–OUT7	LED Driver Outputs. OUT0–OUT7 are open-drain, constant-current-sinking outputs rated for 36V.
29	RTCT	PWM Controller Timing Resistor/Capacitor Connection. A resistor R_T from RTCT to REF and a capacitor C_T from RTCT to AGND set the oscillator frequency.
30	CS	PWM Controller Current-Sense Input
33	AGND	Analog Ground
34	OUT	MOSFET Driver Output OUT. Connects to the gate of the external n-channel MOSFET.
35	V_{CC}	Power-Supply Input. Bypass V_{CC} to AGND with a 0.1µF ceramic capacitor or a parallel combination of a 0.1µF and a higher value ceramic capacitor.
37	REF	5V Reference Output. Bypass REF to AGND with a 0.1µF ceramic capacitor.
—	EP	Exposed Paddle. Connect to the ground plane for improved power dissipation. Do not use as the only ground connection.

Detailed Description

The MAX16809/MAX16810 LED drivers include an internal switch-mode controller that can be used as boost or buck-boost (SEPIC) converters to generate the voltage necessary to drive the multiple strings of LEDs. These devices incorporate an integrated low-side driver, a programmable oscillator (20kHz to 1MHz), an error amplifier, a low-voltage (300mV) current sense for higher efficiency, and a 5V reference to power up external circuitry (see Figures 1a, 1b, and 1c).

The MAX16809/MAX16810 LED drivers include a 4-wire serial interface and a current-mode PWM controller to generate the necessary voltage for driving 16 open-drain, constant-current-sinking output ports. The drivers use current-sensing feedback circuitry (not simple current mirrors) to ensure very small current variations over the full allowed range of output voltage (see the *Typical Operating Characteristics*). The 4-wire serial interface comprises a 16-bit shift register and a 16-bit transparent latch. The shift register is written through a clock input, CLK, and a data input, DIN, and the data propagates to a data output, DOUT. The data output allows multiple drivers to be cascaded and operated together. The contents of the 16-bit shift register are loaded into the transparent latch through a latch-enable input, LE. The latch is transparent to the shift register outputs when high and latches the current state on the falling edge of LE. Each driver output is an open-drain, constant-current sink that should be connected to the

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

cathode of a string of LEDs connected in series. The constant-current capability is up to 55mA per output, set for all 16 outputs by an external resistor, R_{SET}. The devices can operate in a stand-alone mode (see the *Typical Operating Circuits*).

The MAX16810 includes circuitry that automatically detects open-circuit LEDs. Fault status is loaded into the serial-interface shift register when LE goes high and is automatically shifted out on DOUT when the next data transmission is shifted in. The MAX16810 also features a watchdog that monitors activity on the CLK, DIN, and LE inputs (see the *Watchdog (MAX16810)* section). The number of channels can be expanded by using the MAX6970 and MAX6971 family in conjunction with the MAX16809 and MAX16810.

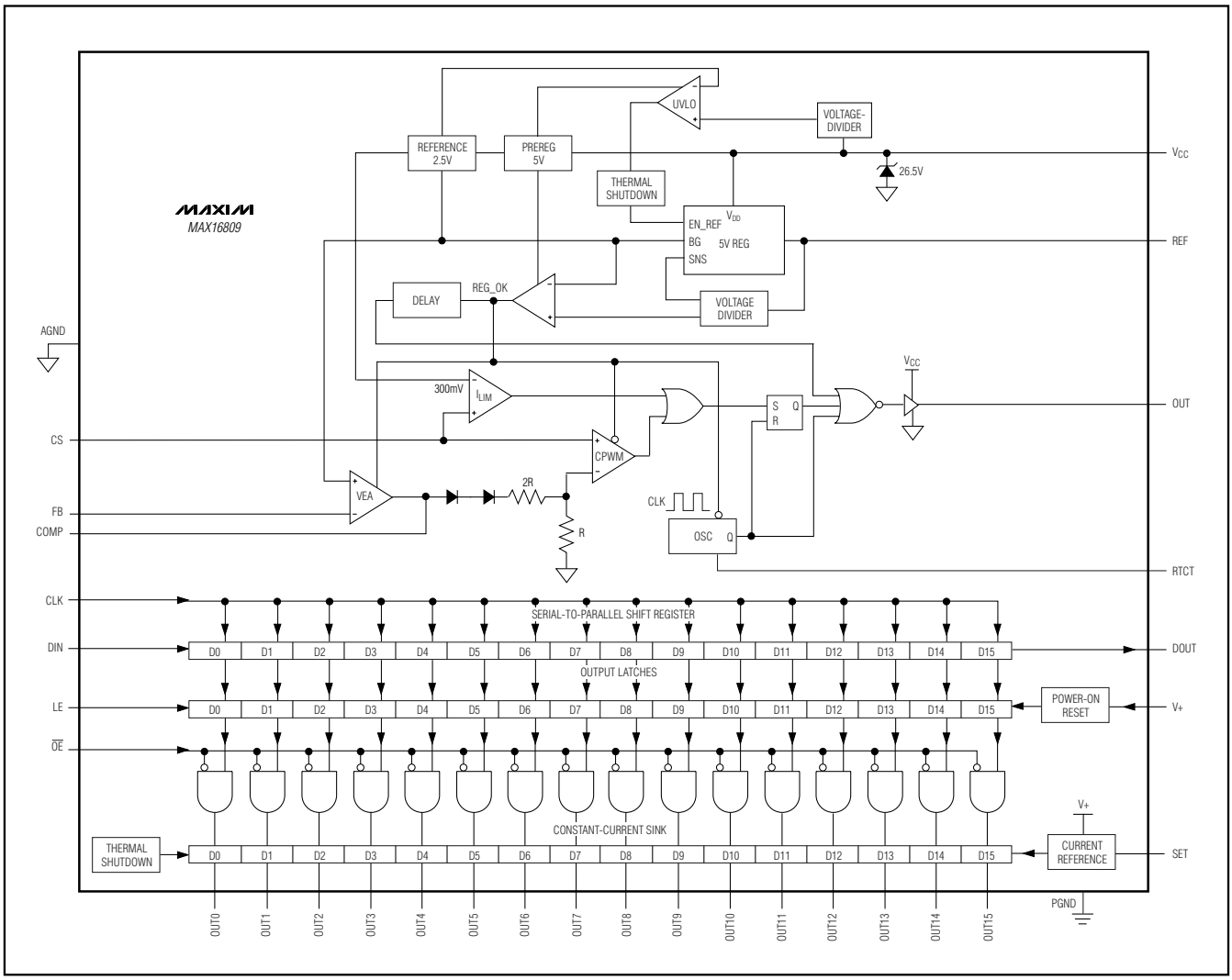


Figure 1a. Internal Block Diagram (MAX16809)

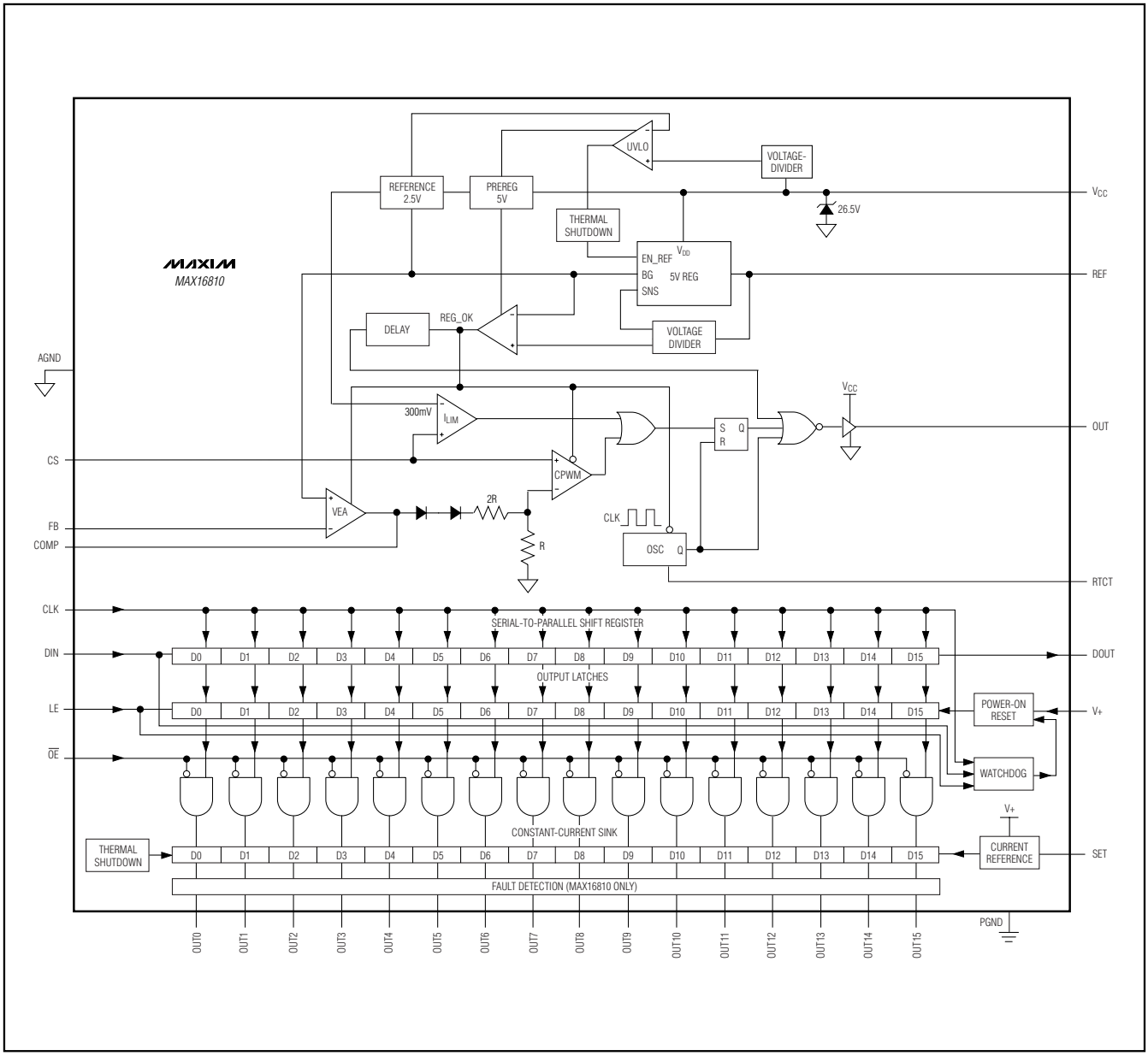


Figure 1b. Internal Block Diagram (MAX16810)

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

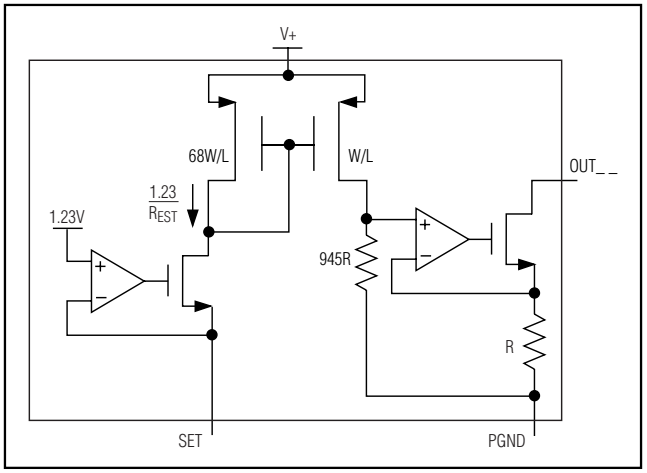


Figure 1c. OUT_ _ Driver Internal Diagram

Switch-Mode Controller

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single-pole system unlike the double pole in the voltage-mode control scheme. The MAX16809/MAX16810 use a current-mode control loop where the output of the error amplifier is compared to the current-sense voltage (V_{CS}). When the current-sense signal is lower than the inverting input of the CPWM comparator, the output of the comparator is low and the switch is turned on at each clock pulse. When the current-sense signal is higher than the inverting input of the CPWM comparator, the output is high and the switch is turned off.

Undervoltage Lockout (UVLO)

The turn-on supply voltage for the MAX16809/MAX16810 is 8.4V (typ). Once V_{CC} reaches 8.4V, the reference powers up. There is a 0.8V of hysteresis from the turn-on voltage to the UVLO threshold. Once V_{CC} reaches 8.4V, the MAX16809/MAX16810 operate with V_{CC} down to 7.6V. Once V_{CC} goes below 7.6V (typ), the device is in UVLO. When in UVLO, the quiescent supply current into V_{CC} falls back to 32µA (typ), and OUT and REF are pulled low.

MOSFET Driver

OUT drives an external n-channel MOSFET and swings from AGND to V_{CC}. Ensure that V_{CC} remains below the absolute maximum V_{GS} rating of the external MOSFET. OUT is a push-pull output with the on-resistance of the pMOS typically 3.5Ω and the on-resistance of the nMOS typically 4.5Ω. The driver can source 2A and sink 1A typically. This allows for the MAX16809/MAX16810 to quickly turn on and off high gate-charge MOSFETs. Bypass V_{CC} with one or more 0.1µF ceramic capacitors to AGND, placed close to V_{CC}. The average current sourced to drive the external MOSFET depends on the total gate charge (Q_G) and operating frequency of the converter. The power dissipation in the MAX16809/MAX16810 is a function of the average output drive current (I_{DRIVE}). Use the following equation to calculate the power dissipation in the device due to I_{DRIVE}:

$$I_{DRIVE} = (Q_G \times f_{SW})$$
$$PD = (I_{DRIVE} + I_{CC}) \times V_{CC}$$

where I_{CC} is the operating supply current. See the *Typical Operating Characteristics* for the operating supply current at a given frequency.

Error Amplifier

The MAX16809/MAX16810 include an internal error amplifier. The inverting input is at FB and the noninverting input is internally connected to a 2.5V reference. Set the output voltage using a resistive divider between output of the converter V_{OUT}, FB, and AGND. Use the following formula to set the output voltage:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{FB}$$

where V_{FB} = 2.5V.

Oscillator

The oscillator frequency is programmable using an external capacitor and a resistor at RTCT (see R_T and C_T in the *Typical Operating Circuits*). R_T is connected from RTCT to the 5V reference (REF), and C_T is connected from RTCT to AGND. REF charges C_T through R_T until its voltage reaches 2.8V. C_T then discharges through an 8.3mA internal current sink until C_T's voltage reaches 1.1V, at which time C_T is allowed to charge through R_T again. The oscillator's period is the sum of the charge and discharge times of C_T. Calculate the charge time as follows:

$$t_C = 0.57 \times R_T \times C_T$$

where t_C is in seconds, R_T in ohms (Ω), and C_T in Farads (F).

The discharge time is then:

$$t_D = (R_T \times C_T \times 1000) / [(4.88 \times R_T) - (1.8 \times 1000)]$$

where t_D is in seconds, R_T in ohms (Ω), and C_T in Farads (F).

The oscillator frequency is then:

$$f_{OSC} = \frac{1}{(t_C + t_D)}$$

Reference Output

REF is a 5V reference output that can source 20mA. Bypass REF to AGND with a 0.1µF capacitor.

Current Limit

The MAX16809/MAX16810 include a fast current-limit comparator to terminate the ON cycle during an overload or a fault condition. The current-sense resistor, R_{CS}, connected between the source of the external MOSFET and AGND, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 0.3V. Use the following equation to calculate R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{P-P}}$$

I_{P-P} is the peak current that flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (OUT) turns the switch off within 60ns. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the time constant of the RC filter at 50ns.

Buck-Boost (SEPIC) Operation

Figure 2 shows a buck-boost application circuit using the MAX16809/MAX16810 in a stand-alone mode of operation. SEPIC topology is necessary when the total forward voltage of the LEDs in a string is such that V_{OUT} can be below or above V_{IN}.

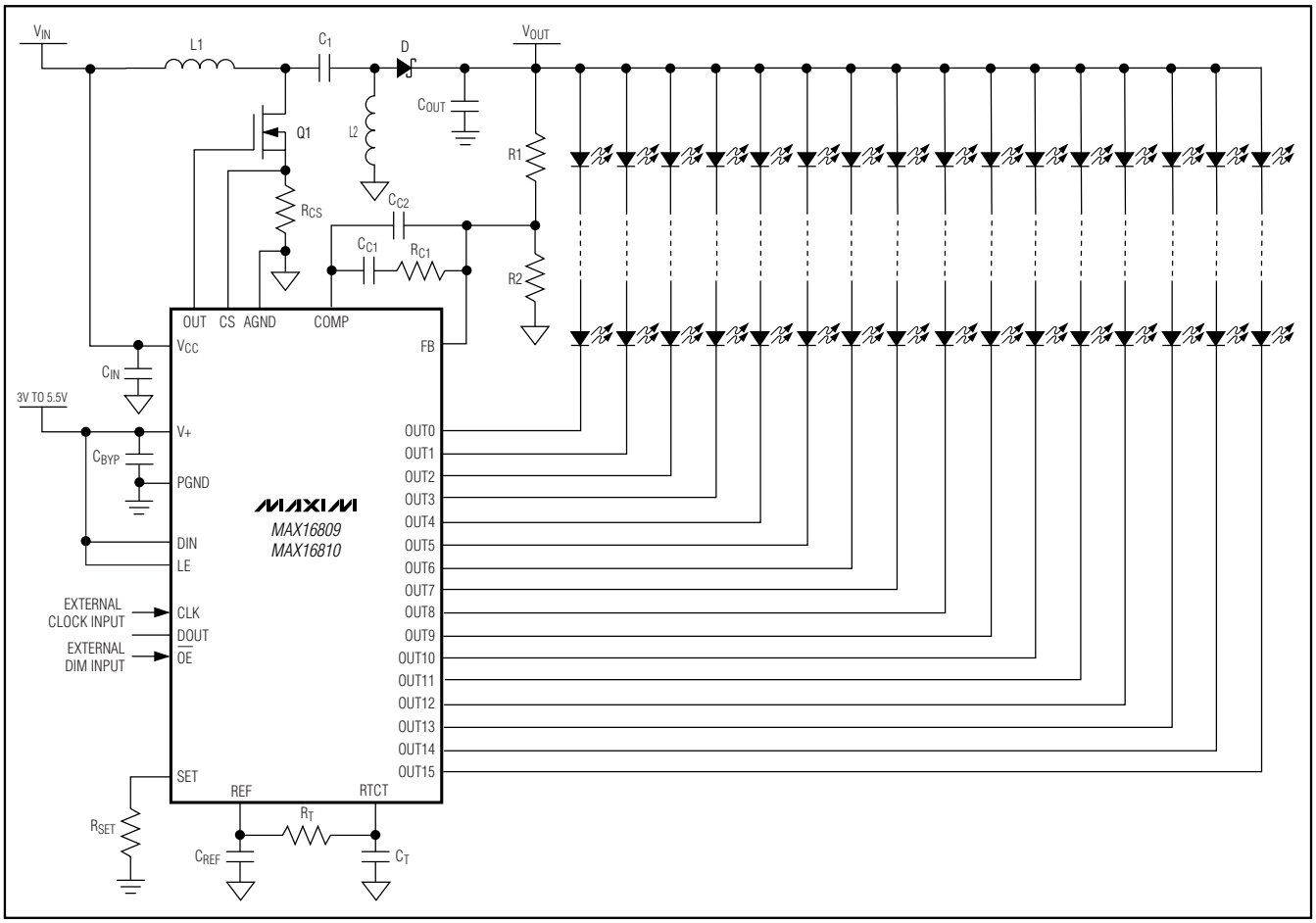


Figure 2. Buck-Boost (SEPIC) Operation

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

LED Driver

4-Wire Interface

The MAX16809/MAX16810 also operate in a stand-alone mode (see the *Typical Operating Circuits*). For use with a microcontroller, the MAX16809/MAX16810 feature a 4-wire serial interface using DIN, CLK, LE, $\overline{OE}$ inputs and DOUT as a data output. This interface is used to write the LED channels' data to the MAX16809/MAX16810. The serial-interface data word length is 16 bits, D0–D15. See Figure 3.

The functions of the five interface pins are as follows:

DIN is the serial-data input, and must be stable when it is sampled on the rising edge of CLK. Data is shifted in MSB first. This means that data bit D15 is clocked in first, followed by 15 more data bits, finishing with the LSB, D0.

CLK is the serial-clock input that shifts data at DIN into the MAX16809/MAX16810's 16-bit shift register on its rising edge.

LE is the latch-enable input of the MAX16809/MAX16810 that transfers data from the 16-bit shift register to its 16-bit output latches (transparent latch). The data latches on the falling edge of LE (Figure 4). The fourth input ($\overline{OE}$) provides output-enable control of the output drivers. When $\overline{OE}$ is driven high, the outputs (OUT0–OUT15) are forced to high impedance without altering the contents of the output latches. Driving $\overline{OE}$ low enables the outputs to follow the state of the output latches. $\overline{OE}$ is independent of the serial interface operation. Data can be shifted into the serial-interface shift register and latched, regardless of the state of $\overline{OE}$. DOUT is the serial-data output that shifts data out from the MAX16809/MAX16810's 16-bit shift register on the rising edge of CLK. Data at DIN propagates through the shift register and appears at DOUT 16 clock cycles later. Table 1 shows the 4-wire serial-interface truth table.

Table 1. 4-Wire Serial-Interface Truth Table

SERIAL DATA INPUT DIN	CLOCK INPUT	SHIFT REGISTER CONTENTS						LOAD INPUT	LATCH CONTENTS						BLANKING INPUT	OUTPUT CONTENTS CURRENT AT OUT_ _					
	CLK	D0	D1	D2	…	Dn-1	Dn	LE	D0	D1	D2	…	Dn-1	Dn	$\overline{OE}$	D0	D1	D2	…	Dn-1	Dn
H	↑	H	R0	R1	…	Rn-2	Rn-1														
L	↑	L	R0	R1	…	Rn-2	Rn-1														
X	↓	R0	R1	R2	…	Rn-1	Rn														
		X	X	X	…	X	X	L	R0	R1	R2	…	Rn-1	Rn							
		P0	P1	P2	…	Pn-1	Pn	H	P0	P1	P2	…	Pn-1	Pn	L	P0	P1	P2	…	Pn-1	Pn
									X	X	X	…	X	X	H	L	L	L	…	L	L

L = Low Logic Level
H = High Logic Level
X = Don't Care
P = Present State (Shift Register)
R = Previous State (Latched)

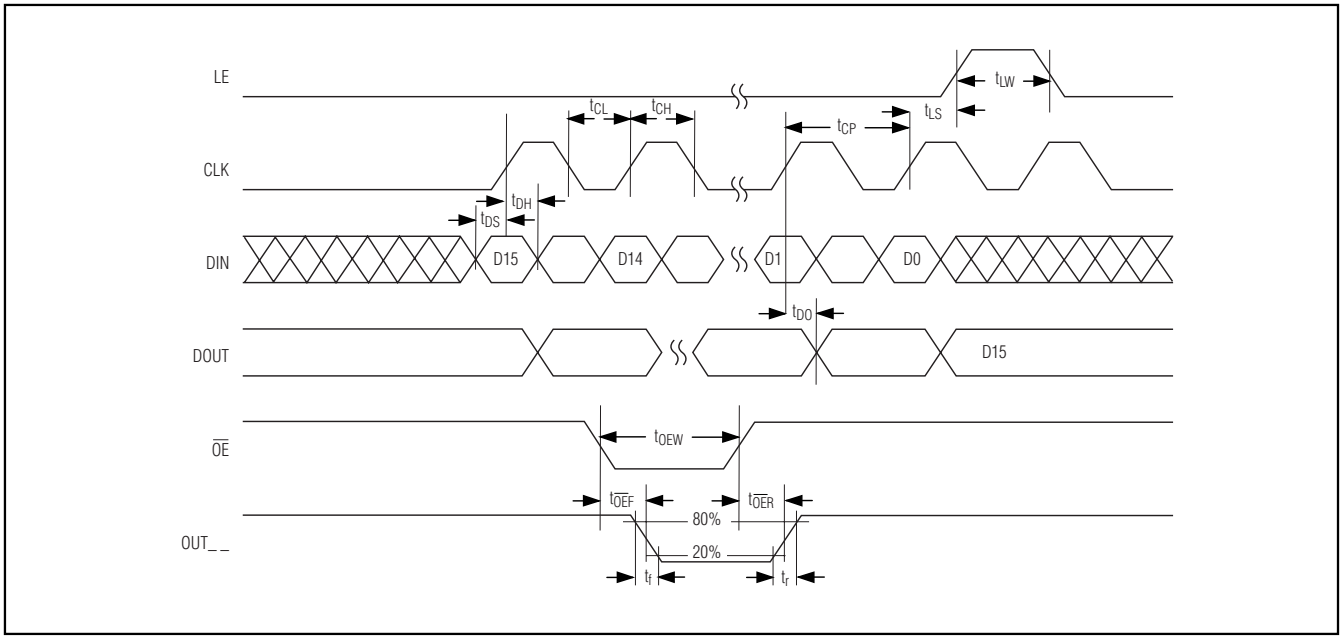


Figure 3. 4-Wire Serial-Interface Timing Diagram

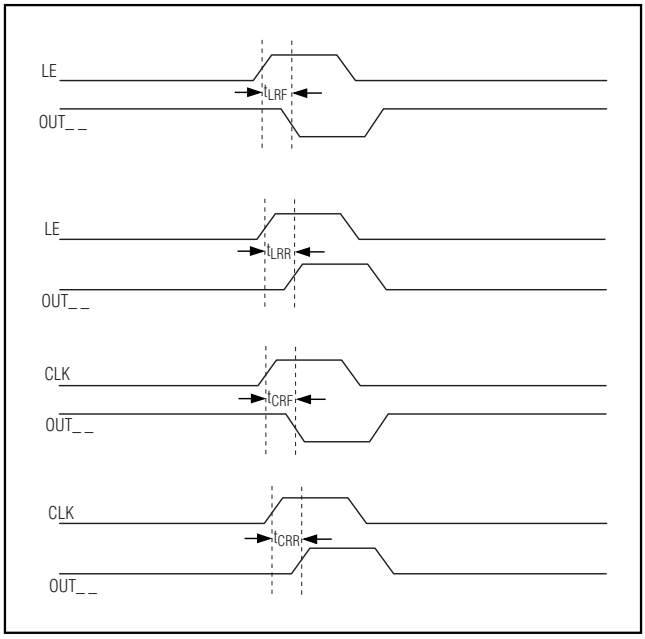


Figure 4. LE and CLK to OUT_ _ Timing

Watchdog (MAX16810)

The MAX16810 includes a watchdog circuit that monitors the CLK, DIN, and LE inputs. If there is no transition on any one of these inputs for nominally 1s, the output latches are cleared and outputs OUT0–OUT15 go high impedance like the initial power-up condition. This turns off all LEDs connected to the outputs. The shift-register data does not change, just the output-latch data. When the watchdog triggers, the outputs remain off until the driver output latches are updated with data turning them on. Recovery is therefore automatic if the transmission failure is temporary because the MAX16810 does not lock up in the watchdog timeout state. The MAX16810 operates correctly when the serial interface is next activated, and the watchdog circuit is reset and starts monitoring the serial interface again. The watchdog function requires no software change to the application driving the MAX16810. The rise time for CLK, DIN, and LE should be less than 10µs.

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LED Fault Detection (MAX16810)

The MAX16810 includes circuitry that detects open-circuit LEDs automatically. An open-circuit fault occurs when an output is sinking current less than approximately 50% of the programmed current flows. Open circuits are checked just after the falling edge of $\overline{OE}$. The fault data is latched on the rising edge of LE and is shifted out when new LED data is loaded into the output latches from the shift register. If one or more output ports are detected with an open-circuit fault, the D14 and D13 bits of DOUT go high. If no open-circuit faults are detected, D14 and D13 are set to low. The data in the other 14 bit positions in DOUT are not altered. Fault status is shifted out on DOUT for the first two rising edges of the clock after the falling edge of LE (see Figure 5). LE is normally taken high after all 16 bits of new LED data have been clocked into the shift register(s), and then DOUT outputs data bit D15. A typical fault-detecting application tests all the shifted out data. Bits D0–D12 and D15 are checked against the originally transmitted data to check data-link integrity. Bits D13 and D14 are checked first to see that they contain the same data (validating the status), and second, whether faults are reported or not by the actual logic level.

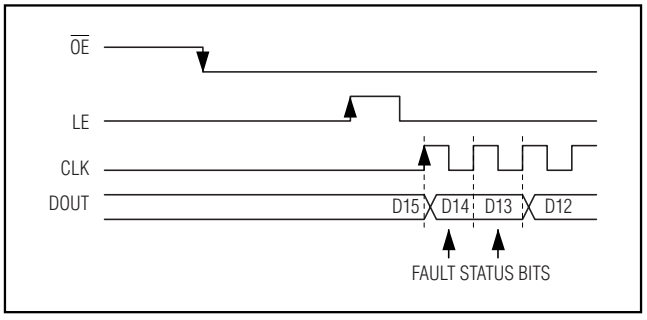


Figure 5. Fault Timing

Selecting External Component R_{SET} to Set LED Output Current

The MAX16809/MAX16810 use an external resistor, R_{SET}, to set the LED current for outputs OUT0–OUT15. The minimum allowed value of R_{SET} is 311Ω, which sets the output currents to 55mA. The maximum allowed value of R_{SET} is 5kΩ ($I_{OUT\_\_}$ = 3.6mA) and maximum allowed capacitance at SET is 100pF.

Use the following formula to set the output current:

$$R_{SET} = \frac{17{,}100V}{I_{OUT\_\_}}$$

where $I_{OUT\_\_}$ is the desired output current in milliamps and the value for R_{SET} is in ohms.

Overtemperature Cutoff

The MAX16809/MAX16810 contain an internal temperature sensor that turns off all outputs when the die temperature exceeds +165°C. The outputs are enabled again when the die temperature drops below +140°C. Register contents are not affected, so when a driver is overdissipating, the external symptom is the load LEDs cycling on and off as the driver repeatedly overheats and cools, alternately turning itself off and then back on again.

Stand-Alone Operation

In stand-alone operation, the MAX16809/MAX16810 does not use the 4-wire interface (see the *Typical Operating Circuits*). Connect DIN and LE to V+ and provide at least 16 external clock pulses to CLK to enable 16 output ports. This startup pulse sequence can be provided either using an external clock or the PWM signal. The external clock can also be generated using the signal at RTCT and an external comparator.

LED Dimming

PWM Dimming

All the output channels can be dimmed simultaneously by applying a PWM signal (50Hz to 30kHz) to $\overline{OE}$. This allows for a wide range of dimming up to a 5000:1 ratio. Each channel can be independently turned on and off using a 4-wire serial interface. The dimming is proportional to the PWM duty cycle.

LED Current Amplitude Adjustment

Using an analog or digital potentiometer as R_{SET} allows for LED current amplitude adjustment and linear dimming.

Computing Power Dissipation

Use the following equation to estimate the upper limit power dissipation (PD) for the MAX16809/MAX16810:

$$PD = DUTY \times \left[(V+ \times I+) + \sum_{i=0}^{i=15} V_{OUTi} \times I_{OUTi} \right] + (V_{CC} \times I_{CC})$$

where:

V+ = supply voltage

I+ = V+ operating supply current

DUTY = PWM duty cycle applied to $\overline{OE}$

V_{OUTi} = MAX16809/MAX16810 port output voltage when driving load LED(s)

I_{OUTi} = LED drive current programmed by R_{SET}

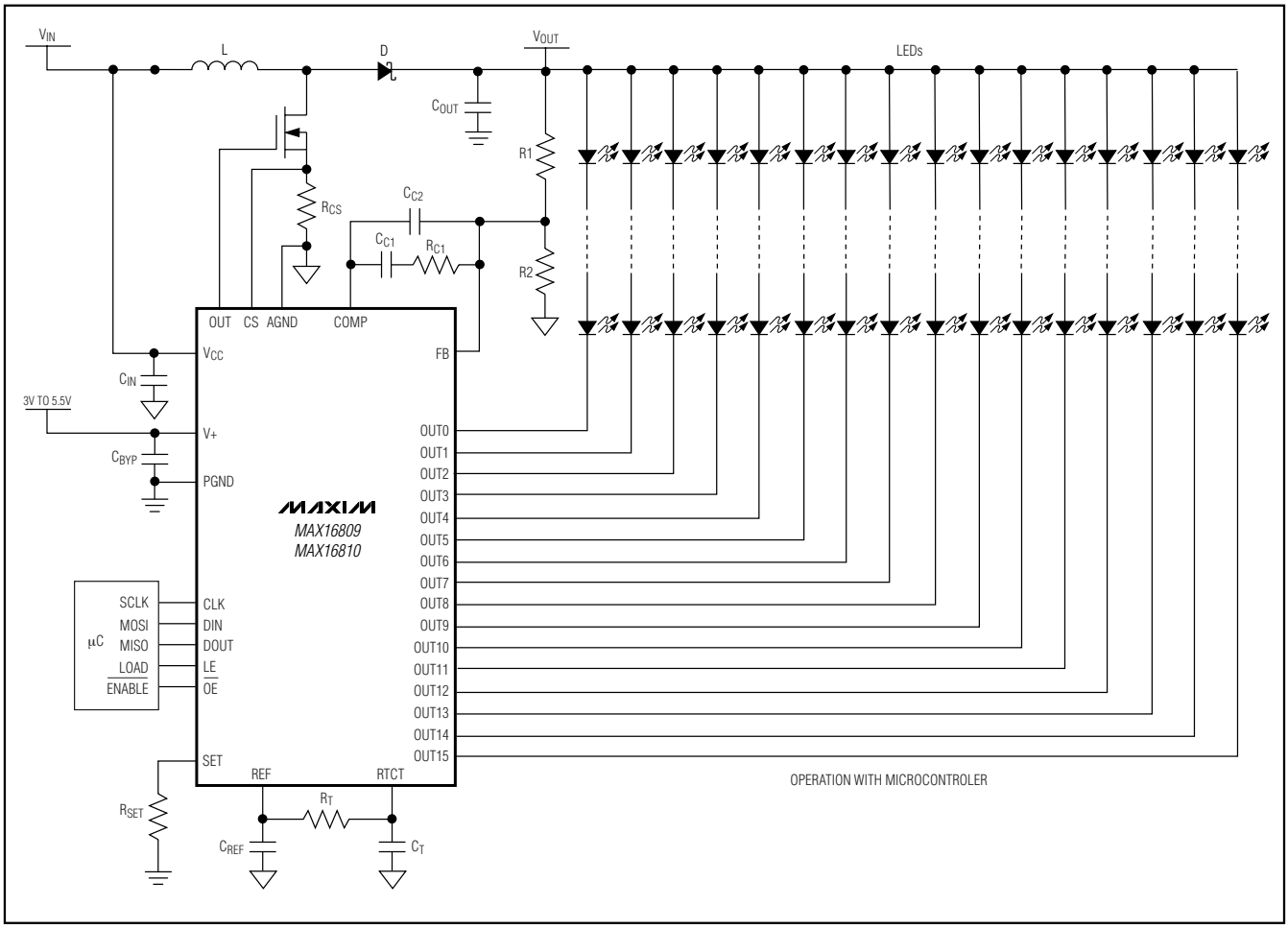
PD = power dissipation

PCB Layout Guidelines

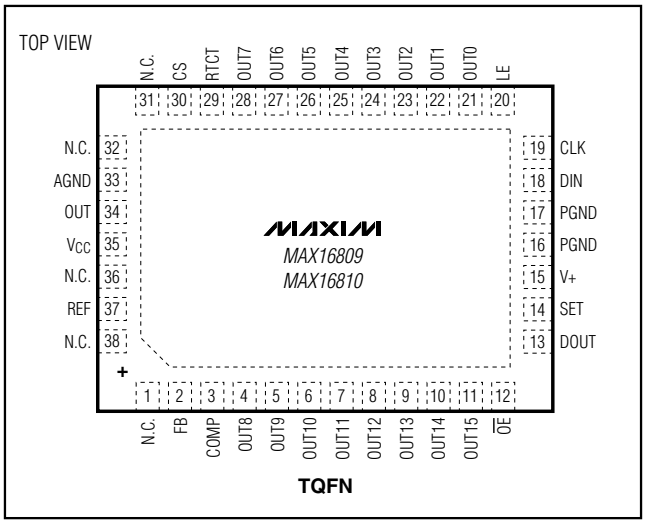
Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting AGND, PGND, the input bypass-capacitor ground lead, and the output-filter ground lead to a single point (star ground configuration). Also, minimize trace lengths to reduce stray capacitance, trace resistance, and radiated noise. The trace between the output voltage-divider and the FB pin must be kept short, as well as the trace between AGND and PGND.

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

Typical Operating Circuits (continued)



Pin Configuration



Chip Information

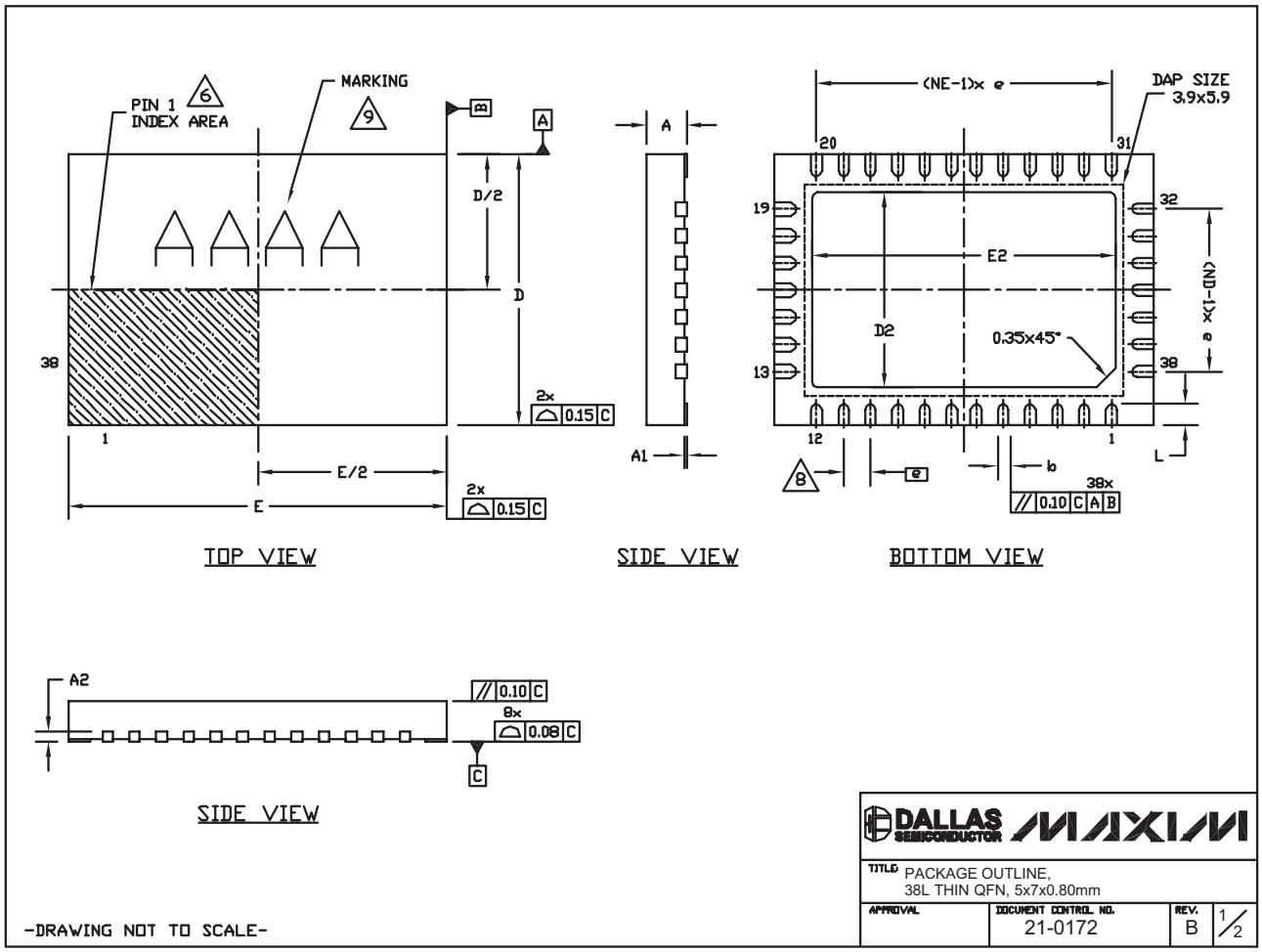
PROCESS: BiCMOS

Integrated 16-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

38L THIN QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S)
5. REFER JEDEC MO-220, WHKD-1.
6. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
7. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
9. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

	COMMON DIMENSIONS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2		0.20 REF.	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
e		0.50 BSC.	
E	6.90	7.00	7.10
L	0.35	0.40	.045
N		38	
ND		7	
NE		12	

	EXPOSED PAD DIMENSIONS					
	D2			E2		
PACKAGE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3857-1	3.50	3.60	3.70	5.50	5.60	5.70
T3857M-1	3.50	3.60	3.70	5.50	5.60	5.70

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 38L THIN QFN, 5x7x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0172	B	2/2

Revision History

Pages changed at Rev 1: 1, 14, 16, 22, 23