Data Sheet | December 21, 2007 | FN6612.0

1.5A 1.6MHz Low Quiescent Current High Efficiency Synchronous Buck Regulator

ISL9107 and ISL9108 are 1.6MHz synchronous step-down regulators with integrated power switches capable of delivering 1.5A output current, which is ideal for powering low-voltage microprocessors in compact devices such as PDAs and cellular phones. These devices are optimized for generating low output voltages down to 0.8V. The supply voltage range is from 2.7V to 5.5V allowing for the use of a single Li+ cell, three NiMH cells or a regulated 5V input. 1.6MHz pulse-width modulation (PWM) switching frequency allows using small external components. They have flexible operation mode selection of forced PWM mode and Skip (Low I_Q) mode with typical 17µA quiescent current for highest light load efficiency to maximize battery life.

The ISL9107 and ISL9108 integrate a pair of low ON-resistance P-Channel and N-Channel MOSFETs to maximize efficiency and minimize external component count.

The ISL9107 offers a typical 215ms Power-Good (PG) timer when powered up. The timer output can be reset by RSI. When shutdown, ISL9107 and ISL9108 discharge the output capacitor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown.

The ISL9107 and ISL9108 are offered in 8 Ld 2mmx3mm DFN package with 0.9mm typical height. The complete converter can occupy less than $1cm^2$ area.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9107IRZ-T	107	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9108IRZ-T	108	-40 to +85	8 Ld 2x3 DFN	L8.2x3

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

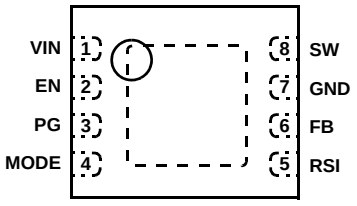
- Integrated Synchronous Buck Regulator with up to 95% Efficiency
- 2.7V to 5.5V Supply Voltage
- 1.5A Guaranteed Output Current
- 17µA Quiescent Supply Current in Skip (Low I_Q) Mode
- Selectable Forced PWM Mode and Skip Mode
- Less Than 1µA Logic Controlled Shutdown Current
- 100% Maximum Duty Cycle for Lowest Dropout
- Discharge Output Capacitor when Shutdown
- Internal Digital Soft-Start
- Enable, Peak Current Limiting, Short Circuit Protection
- Over-Temperature Protection
- Power-Good Function (for ISL9107 only)
- 8 Ld 2mmx3mm DFN
- Pb-Free (RoHS Compliant)

Applications

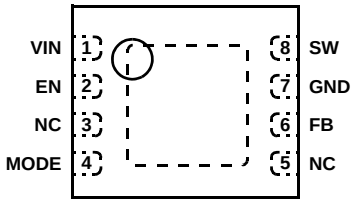
- Single Li-Ion Battery-Powered Equipment
- DSP Core Power
- PDAs and Palmtops

Pinouts

ISL9107
(8 LD 2X3 DFN)
TOP VIEW



ISL9108
(8 LD 2X3 DFN)
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

VIN . . . . . -0.3V to 6.5V
EN, MODE . . . . . -0.3V to VIN + 0.3V
PG, RSI (Note 1) . . . . . -0.3V to VIN + 0.3V
SW . . . . . -1.5V to 6.5V
FB . . . . . -0.3V to 2.7V

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current . . . . . 0A to 1.5A
Ambient Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Notes 2, 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x3 DFN Package	78	11

Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. For ISL9107 only.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, V_{IN} = V_{EN} = 3.6V, L = 2.2µH, C_1 = 10µF, C_2 = 10µF, I_{OUT} = 0A (see the Typical Application Circuit on page 7).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Undervoltage Lockout Threshold	V_{UVLO}	Rising	-	2.5	2.7	V
		Falling	2.2	2.4	-	V
Quiescent Supply Current	I_{VIN}	MODE = V_{IN}, no load at the output	-	17	30	µA
		MODE = GND, no load at the output	-	5	8	mA
Shut Down Supply Current	I_{SD}	V_{IN} = 5.5V, EN = LOW	-	0.05	2	µA
OUTPUT REGULATION						
FB Regulation Voltage	V_{FB}	T_A = 0°C to +85°C	0.784	0.8	0.816	V
		T_A = -40°C to +85°C	0.78	0.8	0.82	V
FB Bias Current	I_{FB}	VFB = 0.75V	-	0.1	-	µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V)	-	0.2	-	%/V
COMPENSATION						
Error Amplifier Trans-conductance		Design info only	-	20	-	µA/V
SW						
P-Channel MOSFET ON-Resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.12	0.22	Ω
		V_{IN} = 2.7V, I_O = 200mA	-	0.16	0.27	Ω
N-Channel MOSFET ON-Resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.11	0.22	Ω
		V_{IN} = 2.7V, I_O = 200mA	-	0.15	0.27	Ω
N-Channel Bleeding MOSFET ON-Resistance			-	90	-	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}	V_{IN} = 5.5V	1.8	2.1	2.6	A
Maximum Duty Cycle			-	100	-	%
PWM Switching Frequency	f_S	T_A = -40°C to +85°C	1.35	1.6	1.75	MHz
SW Minimum On-Time		MODE = LOW (forced PWM mode)	-	-	100	ns
Soft Start-Up Time			-	1.1	-	ms

Electrical Specifications Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, V_{IN} = V_{EN} = 3.6V, L = 2.2µH, C_1 = 10µF, C_2 = 10µF, I_{OUT} = 0A (see the Typical Application Circuit on page 7). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PG (NOTE 1)						
Output Low Voltage		Sinking 1mA, VFB = 0.7V	-	-	0.3	V
Delay Time			150	215	275	ms
PG Pin Leakage Current		PG = V_{IN} = 3.6V	-	0.01	0.1	µA
Minimum Supply Voltage for Valid PG Signal			1.2	-	-	V
Internal PGOOD Low Rising Threshold		Percentage of Nominal Regulation Voltage	89.5	92	94.5	%
Internal PGOOD Low Falling Threshold		Percentage of Nominal Regulation Voltage	85	88	91	%
Internal PGOOD High Rising Threshold		Percentage of Nominal Regulation Voltage	108.2	110.7	113.2	%
Internal PGOOD High Falling Threshold		Percentage of Nominal Regulation Voltage	104	107	110	%
Internal PGOOD Delay Time			-	50	-	µs
RSI (NOTE 1), EN, MODE						
Logic Input Low			-	-	0.4	V
Logic Input High			1.4	-	-	V
Logic Input Leakage Current		Pulled up to 5.5V	-	0.1	1	µA
Thermal Shutdown			-	150	-	°C
Thermal Shutdown Hysteresis			-	25	-	°C

Pin Descriptions

PIN #	ISL9107 PIN NAME	ISL9108 PIN NAME	DESCRIPTION
1	VIN		Input supply voltage pin. Connect a 10µF ceramic capacitor to power ground.
2	EN		Enable pin. Enable the output when driven to high. Shut down the chip and discharge output capacitor when driven to low. Do not leave this pin floating.
4	MODE		Mode selection pin. Connect to logic high or VIN to enable skip mode; connect to logic low or ground for force PWM mode.
6	FB		Buck regulator output feedback pin. Connect to the output voltage through voltage divider resistors for adjustable output voltage.
7	GND		System ground.
8	SW		Switching node pin. Connect to one terminal of the inductor.
E-PAD	-		Exposed pad. It should be connected to ground for proper electrical performance. The exposed pad must also be connected to as much as possible for optimal thermal performance.
3	PG	NC	For ISL9107, it is 215ms timer output. It outputs 215ms delayed power-good signal when output voltage is within power-good window. It can be reset by a high RSI signal, then 215ms starts when RSI goes from high to low. For ISL9108, do not connect. Leave this pin floating.
5	RSI	NC	For ISL9107, this input resets the 215ms timer. Please refer to “Theory of Operation” on page 9 for more details. For ISL9108, do not connect. Leave this pin floating.

Typical Operating Performance

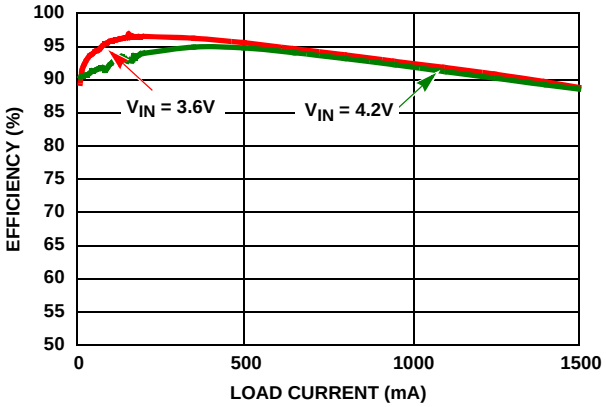


FIGURE 1. EFFICIENY vs LOAD CURRENT (V_{OUT} = 3.3V)

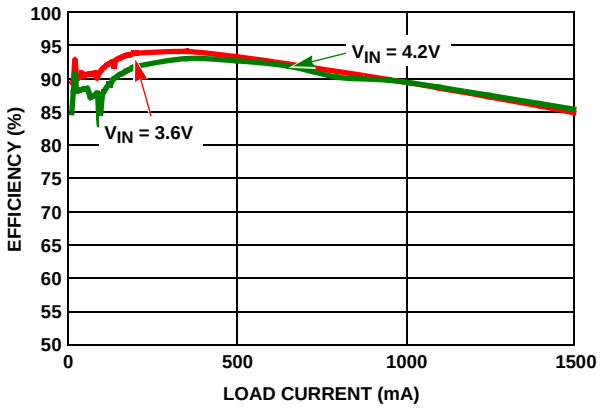


FIGURE 2. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 2.5V)

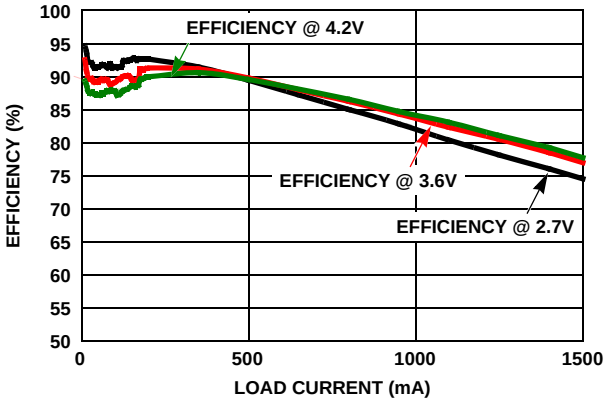


FIGURE 3. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 1.6V)

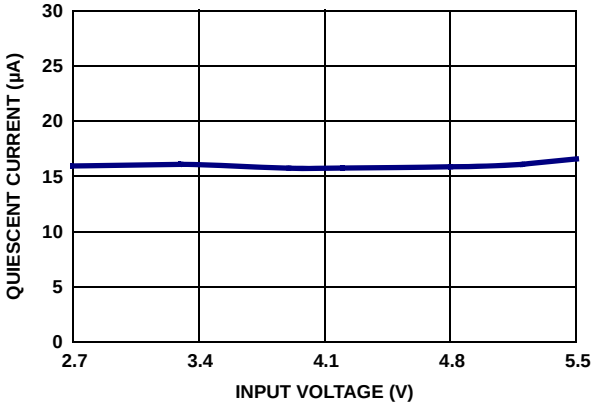


FIGURE 4. I_Q vs V_{IN} (MODE = V_{IN}, V_{OUT} = 1.6V, I_{OUT} = 0)

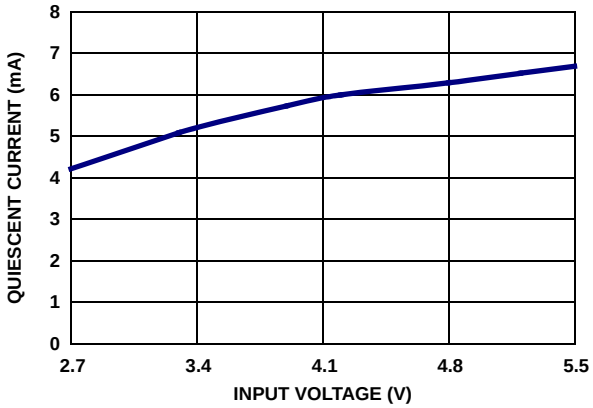


FIGURE 5. I_Q vs V_{IN} (MODE = GND, V_{OUT} = 1.6V, I_{OUT} = 0)

Typical Operating Performance (Continued)

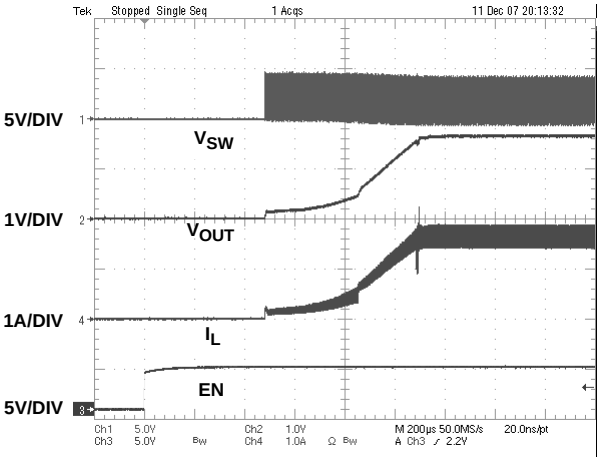


FIGURE 6. SOFT-START (V_{IN} = 4.2V, V_{OUT} = 1.6V, I_{OUT} = 1.5A)

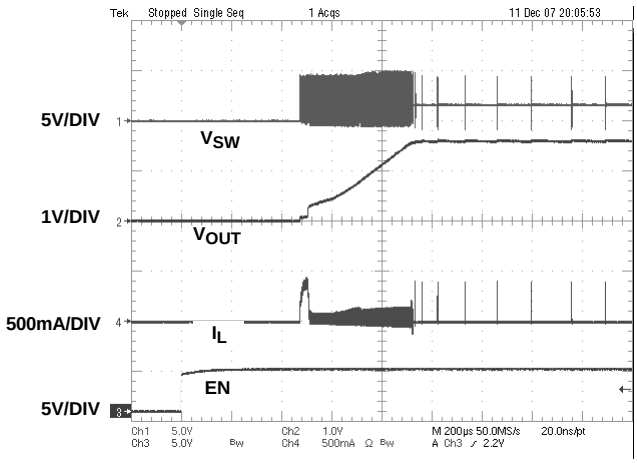


FIGURE 7. SOFT-START (V_{IN} = 4.2V, V_{OUT} = 1.6V, I_{OUT} = 1mA)

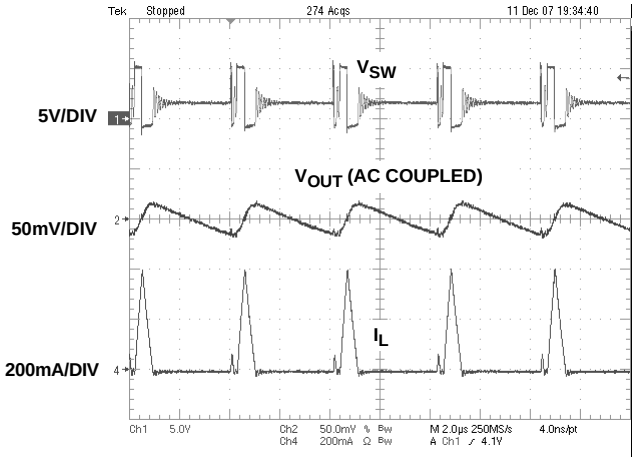


FIGURE 8. STEADY-STATE IN SKIP MODE (V_{IN} = 5.0V, V_{OUT} = 1.6V, I_{OUT} = 35mA)

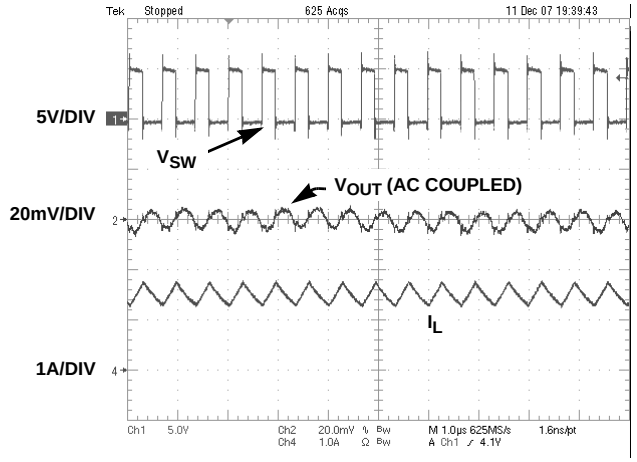


FIGURE 9. STEADY-STATE IN PWM MODE (V_{IN} = 5.0V, V_{OUT} = 1.6V, I_{OUT} = 1.5A)

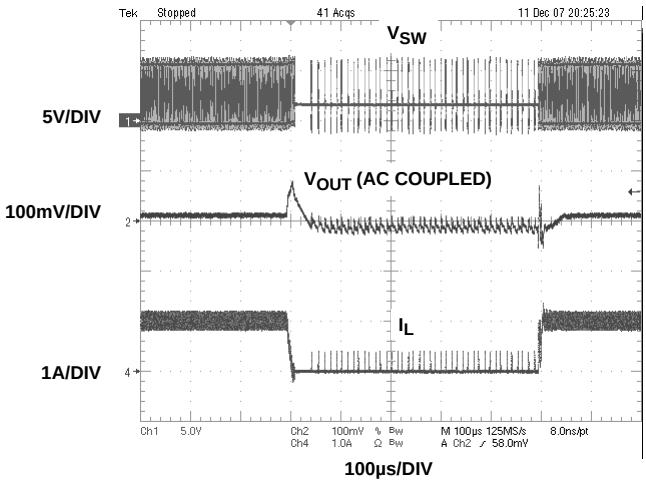


FIGURE 10. LOAD TRANSIENT TEST (MODE = V_{IN} = 5.0V; V_O = 1.6V; I_O = 0.01A~1A)

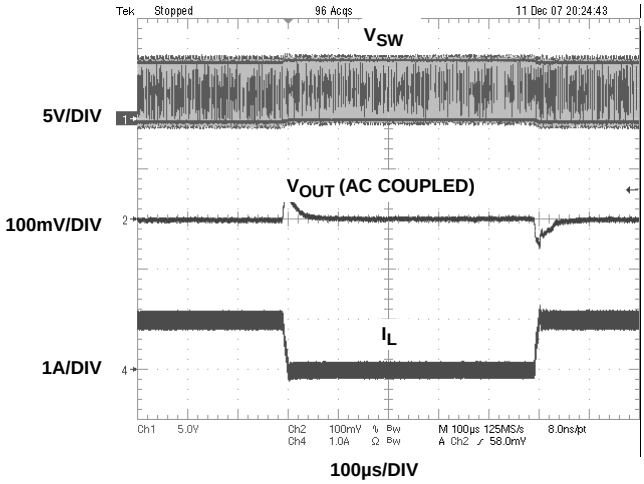


FIGURE 11. LOAD TRANSIENT TEST (MODE = GND, V_{IN} = 5.0V; V_O = 1.6V; I_O = 0.01A~1A)

Typical Operating Performance (Continued)

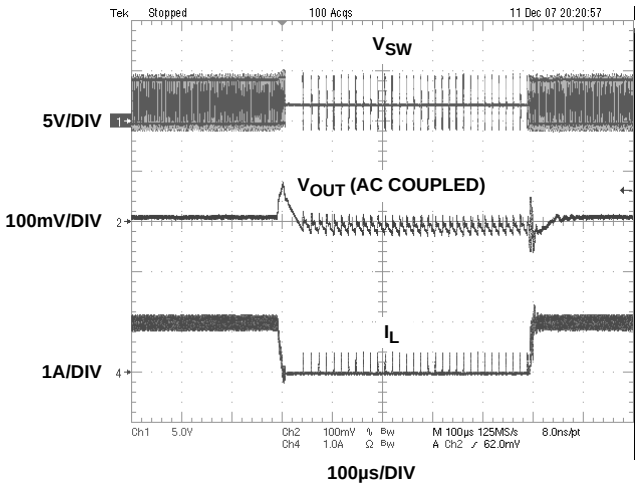


FIGURE 12. LOAD TRANSIENT TEST (MODE = V_{IN} = 4.2V; V_O = 1.6V; I_O = 0.01A~1A)

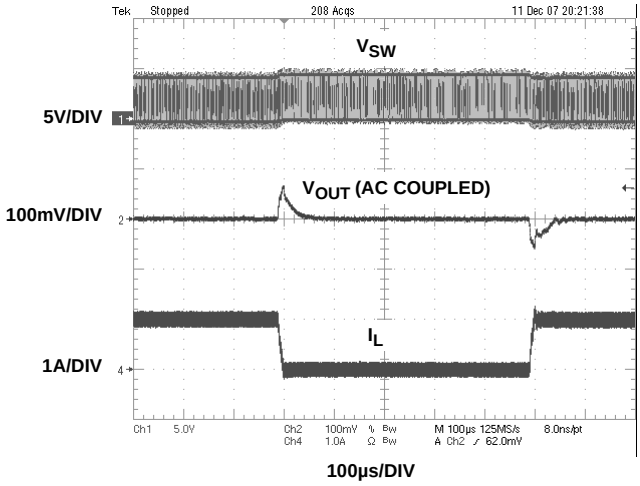


FIGURE 13. LOAD TRANSIENT TEST (MODE = GND, V_{IN} = 4.2V; V_O = 1.6V; I_O = 0.01A~1A)

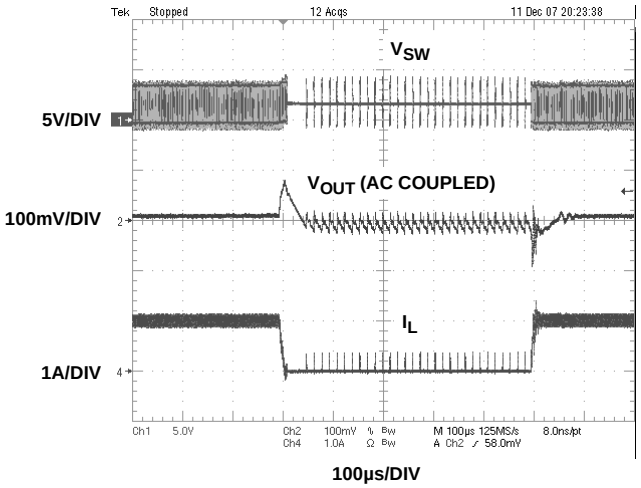


FIGURE 14. LOAD TRANSIENT TEST (MODE = V_{IN} = 3.6V; V_O = 1.6V; I_O = 0.01A~1A)

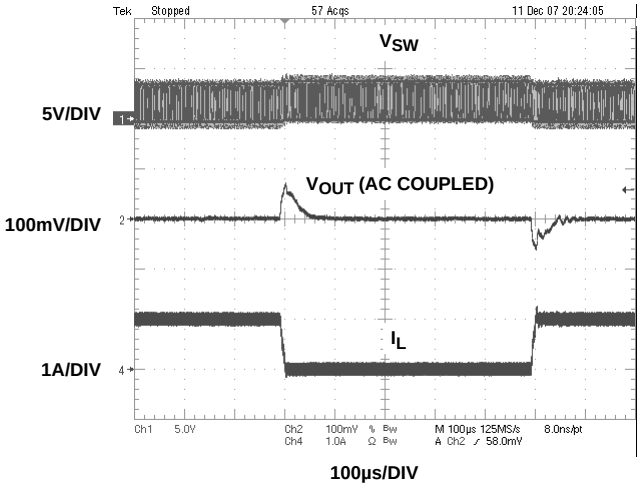
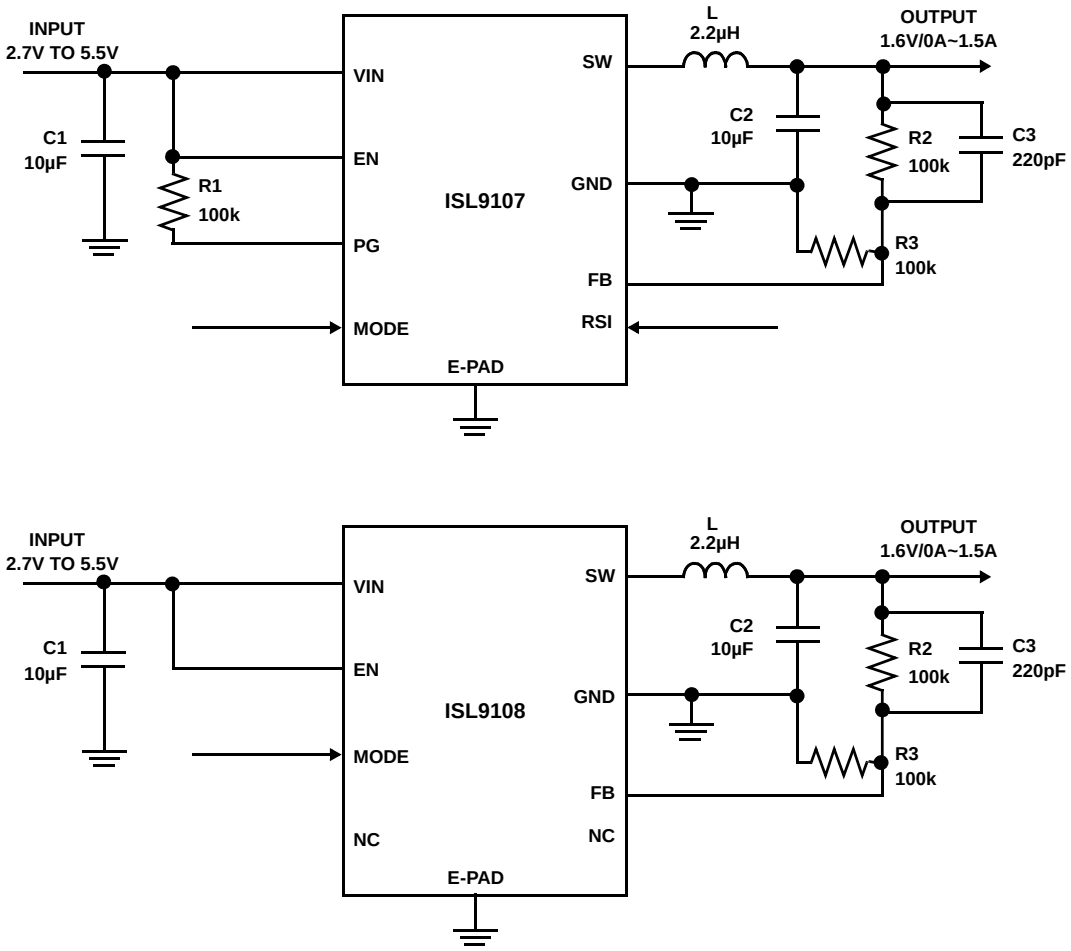


FIGURE 15. LOAD TRANSIENT TEST (MODE = GND, V_{IN} = 3.6V; V_O = 1.6V; I_O = 0.01A~1A)

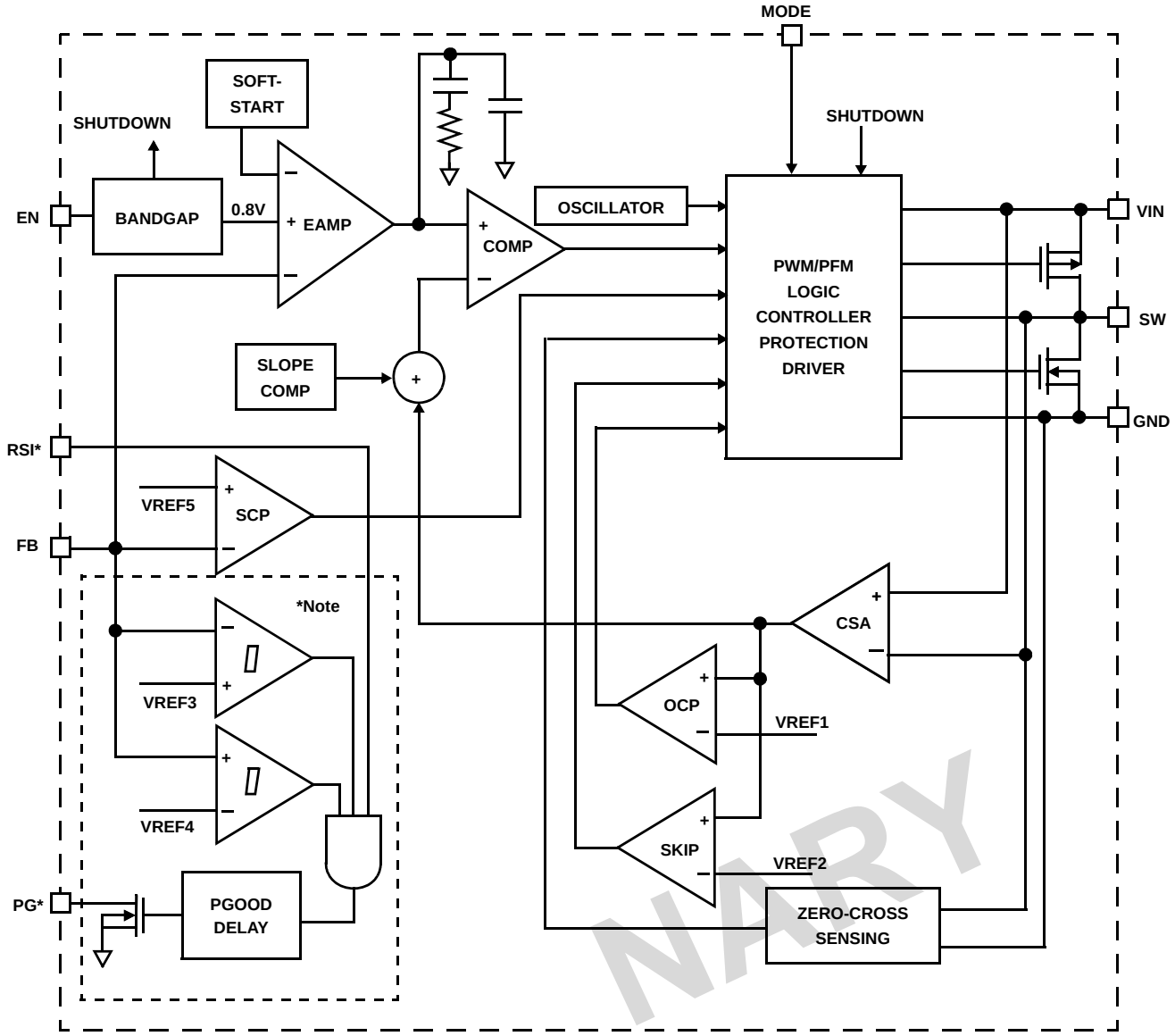
Typical Applications



PARTS	DESCRIPTION	MANUFACTURERS	PART NUMBER	SPECIFICATIONS	SIZE
L	Inductor	Sumida	CDRH4D15/SNP-2R2NC	2.2µH/2.0A/48mΩ	4.4mmx4.4mmx1.7mm
C1	Input capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V	2.0mmx1.25mmx1.25mm
C2	Output capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V	2.0mmx1.25mmx1.25mm
C3	Capacitor	Murata	GRM188R71H221KA01C	220pF/50V	1.6mmx0.8mmx0.8mm
R1(ISL9107)	Resistor	Various		100kΩ, SMD, 1%	1.6mmx0.8mmx0.45mm
R2, R3	Resistor	Various		100kΩ, SMD, 1%	1.6mmx0.8mmx0.45mm

FIGURE 16. TYPICAL APPLICATION DIAGRAM FOR ISL9107 AND ISL9108

Block Diagram



*Note: Only applies to ISL9107.

FIGURE 17. FUNCTIONAL BLOCK DIAGRAM

Theory of Operation

The ISL9107 and ISL9108 are step-down switching regulators optimized for battery-powered handheld applications. The regulators operate at typical 1.6MHz fixed switching frequency under heavy load condition to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulators can be selected to enter skip mode to reduce the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current under skip mode with no loading is typically only 17µA. The supply current is typically only 0.1µA when the regulator is disabled.

PWM Control Scheme

These devices use the peak-current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 17 shows the circuit functional block diagram. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-Channel MOSFET when it is turned on and the Current Sense Amplifier (CSA). The control reference for the current loops comes from the Error Amplifier (EAMP) of the voltage loop.

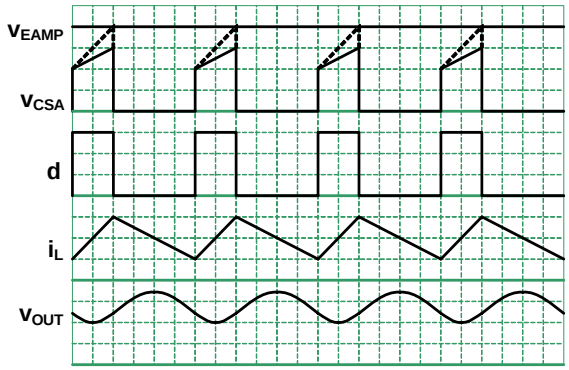


FIGURE 18. PWM OPERATION WAVEFORMS

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the P-Channel MOSFET starts ramping up. When the sum of the CSA output and the compensation slope reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-Channel MOSFET and to turn on the N-Channel MOSFET. The N-MOSFET remains on till the end of the PWM cycle. Figure 18 shows the typical operating waveforms during the normal PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the CSA output.

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the FB pin. The soft-start block only affects the operation during the start-up and will be discussed separately in “Soft Start-Up” on page 10. The EAMP is a transconductance amplifier, which converts the voltage error signal to a current output. The voltage loop is internally compensated by a RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage.

Skip Mode

With the MODE pin connected to logic high, the device enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 19 illustrates the skip mode operation. A zero-cross sensing circuit (as shown in Figure 17) monitors the N-Channel MOSFET current for zero crossing. When it is detected to cross zero for 8 consecutive cycles, the regulator enters the skip mode. During the 8 consecutive cycles, the inductor current could be negative. The counter is reset to zero when the sensed N-Channel MOSFET current does not cross zero during any cycle within the 8 consecutive cycles. Once the device enters the skip mode, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 17. Each pulse cycle is still synchronized by the PWM clock. The P-Channel MOSFET is turned on at the rising edge of clock and turned off when its current reaches 20% of the peak current limit. As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle over cycle. When the output voltage reaches 1.5% above it’s nominal voltage, the P-Channel MOSFET is turned off immediately and the inductor current is fully discharged to zero and stays at zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-Channel MOSFET will be turned on again, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage is sensed to drop below 1.5% of its nominal voltage value.

Enable

The enable (EN) pin allows the user to enable or disable the converter for purposes such as power-up sequencing. With the EN pin pulled to high, the converter is enabled, the internal reference circuit wakes up first and then the soft start-up begins. When the EN pin is pulled to logic low, the converter is disabled, the P-Channel MOSFET is turned off immediately and the output capacitor is discharged through internal discharge path.

Undervoltage Lockout (UVLO)

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the device is disabled.

Mode Selection

The MODE pin is provided on ISL9107 and ISL9108 to select the operation mode. When it is driven to logic low or ground, the regulator operates in forced PWM mode. Under forced PWM mode, the device remains at the fixed PWM operation (typical at 1.6MHz), regardless of if the load current is high or low.

When the MODE pin is driven to logic high or connected to input voltage V_{IN}, the regulator operates in either SKIP mode or fixed PWM mode depending on the different load conditions.

Overcurrent Protection

The overcurrent protection is provided when an overload condition happens. It is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 17. When the current at P-Channel MOSFET is sensed to reach the current limit, the OCP comparator is triggered to turn off the P-Channel MOSFET immediately.

Short-Circuit Protection

As shown in Figure 17, the device has a Short-Circuit Protection (SCP) comparator, which monitors the FB pin voltage for output short-circuit protection. When the FB voltage is lower than 0.2V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of its normal operation frequency.

Soft Start-Up

The soft start-up eliminates the inrush current during the circuit start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.2V; hence the PWM operating frequency is 1/3 of the normal frequency.

Power MOSFETs

The power MOSFETs are optimized to achieve better efficiency. The ON-resistance for the P-Channel MOSFET is typically 0.16Ω and the typical ON-resistance for the N-Channel MOSFET is 0.15Ω.

Low Dropout Operation

The ISL9107 and ISL9108 feature low dropout operation to maximize the battery life. When the input voltage drops to a level that the device can no longer operate under switching regulation to maintain the output voltage, the P-Channel MOSFET is completely turned on (100% duty cycle). The dropout voltage under such condition is the product of the load current and the ON-resistance of the P-Channel MOSFET. Minimum required input voltage V_{IN} under this condition is the sum of the output voltage plus the voltage drop cross the inductor and the P-Channel MOSFET switch.

Thermal Shut Down

The ISL9107 and ISL9108 provide a built-in thermal protection function. The thermal shutdown threshold temperature is typical +160°C with typical +25°C hysteresis. When the internal temperature is sensed to reach +150°C, the regulator is completely shut down and as the temperature is sensed to drop to +125°C (typical), the device resumes operation starting from the soft start-up.

RSI Signal

The RSI signal is an input signal, which can reset the PG signal. As shown in Figure 17, the power-good signal is gated by the RSI signal. When the RSI is high, the PG signal remains low, regardless of the output voltage condition. This function is provided on ISL9107 only.

Power-Good

The ISL9107 offers a power-good (PG) signal. When the output voltage is not within the power-good window, the PG pin outputs an open-drain low signal. When the output voltage is within the power-good window, an internal power-good signal is issued to turn off the open-drain MOSFET so that the PG pin can be externally pulled to high.

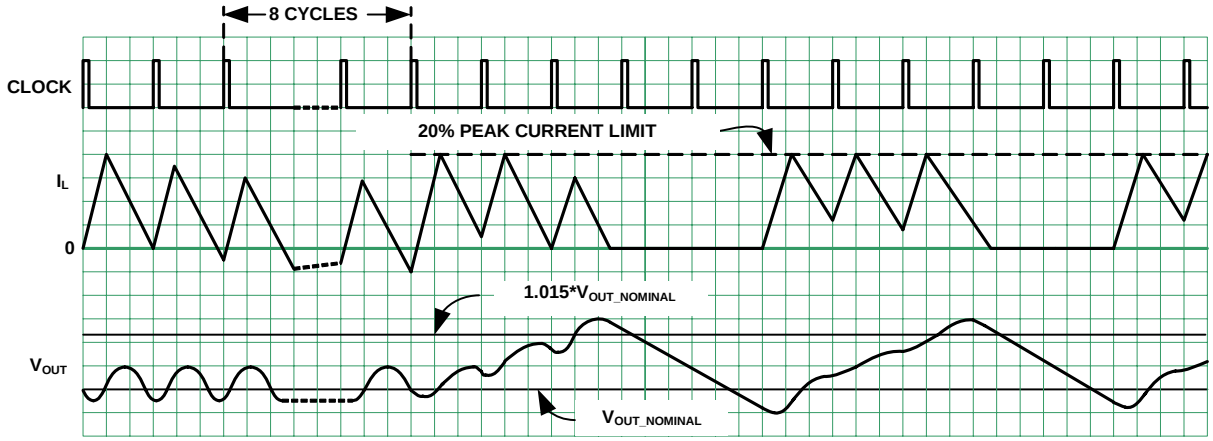


FIGURE 19. SKIP MODE OPERATION WAVEFORMS

The rising edge of the PG output is delayed by 215ms (typical) from the time the power-good signal is issued. This function is provided on ISL9107 only.

Applications Information

Inductor and Output Capacitor Selection

To achieve better steady state and transient response, typically a 2.2µH inductor can be used. The peak-to-peak inductor current ripple can be expressed as in Equation 1:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 1)}$$

In Equation 1, usually the typical values can be used but to have a more conservative estimation, the inductance should consider the value with worst case tolerance; and for switching frequency (f_S), the minimum f_S from the “Electrical Specifications” table on page 2 can be used.

To select the inductor, its saturation current rating should be at least higher than the sum of the maximum output current and half of the delta calculated from Equation 1. Another more conservative approach is to select the inductor with the current rating higher than the P-Channel MOSFET peak current limit.

Another consideration is the inductor DC resistance since it directly affects the efficiency of the converter. Ideally, the inductor with the lower DC resistance should be considered to achieve higher efficiency.

Inductor specifications could be different from different manufacturers so please check with each manufacturer if additional information is needed.

For the output capacitor, a ceramic capacitor can be used because of the low ESR values, which helps to minimize the output voltage ripple. A typical value of 10µF/6.3V ceramic capacitor should be enough for most of the applications and the capacitor should be X5R or X7R.

Input Capacitor Selection

The main function for the input capacitor is to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current from flowing back to the battery rail. A 10µF/6.3V ceramic capacitor (X5R or X7R) is a good starting point for the input capacitor selection.

Output Voltage Setting Resistor Selection

The voltage divider resistors (R_2 and R_3), as shown in Figure 16, set the desired output voltage value. The output voltage can be calculated using Equation 2:

$$V_O = V_{FB} \bullet \left(1 + \frac{R_2}{R_3}\right) \quad \text{(EQ. 2)}$$

where V_{FB} is the feedback voltage (typically it is 0.8V). The current flowing through the voltage divider resistors can be calculated as $V_O/(R_2 + R_3)$, so larger resistance is desirable to minimize this current. On the other hand, the FB pin has leakage current that will cause error in the output voltage setting. The leakage current has a typical value of 0.1µA. To minimize the accuracy impact on the output voltage, select the R_3 no larger than 200kΩ.

C_3 (shown in Figure 16) is highly recommended to be added for improving stability and achieving better transient response. C_3 can be calculated using Equation 3:

$$C_3 = \frac{1}{2 \times \pi \times R_2 \times 7.3kHz} \quad \text{(EQ. 3)}$$

Table 1 provides the recommended component values for some output voltage options.

Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well, especially under the high current, high switching frequency condition.

For ISL9107 and ISL9108, the power loop is composed of the output inductor (L), the output capacitor (C_{OUT}), the SW pin and the GND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide; the same type of traces should be used to connect the VIN pin, the input capacitor C_{IN} and its ground. The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the voltage feedback trace and other noise sensitive traces away from these noisy traces.

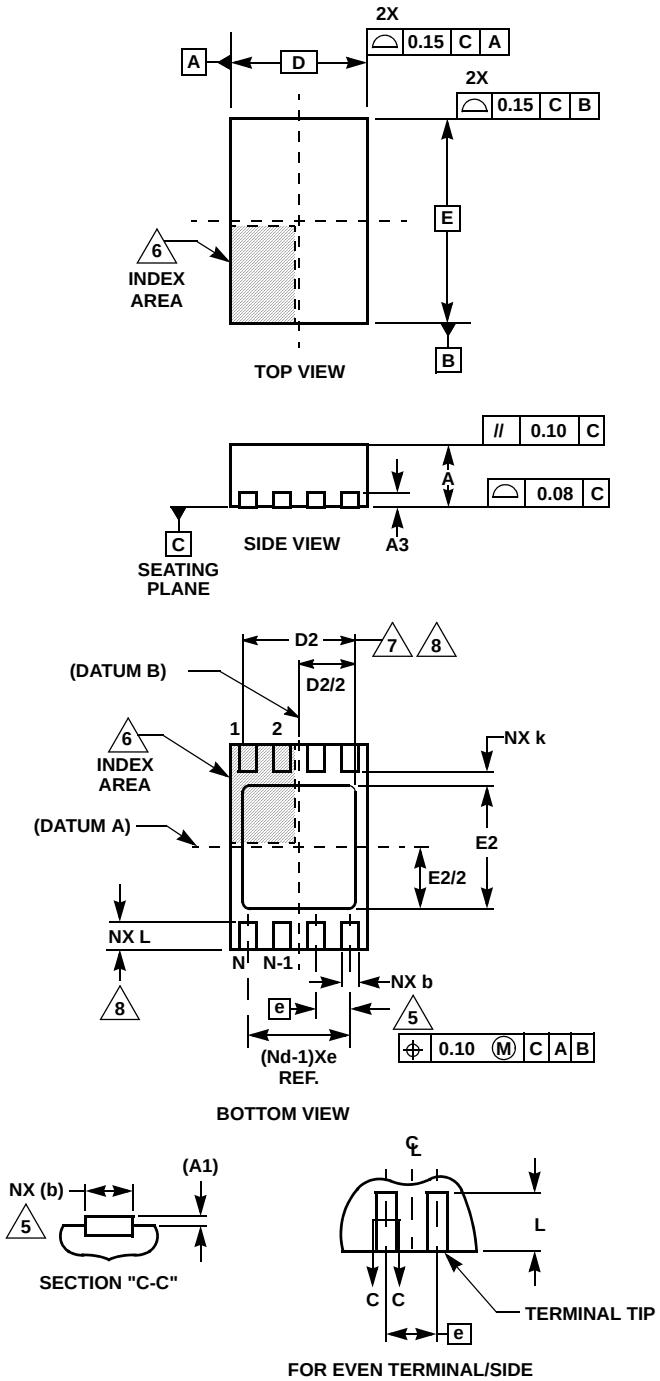
The input capacitor should be placed as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible as well.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for EMI performance.

TABLE 1. ISL9107 AND ISL9108 RECOMMENDED CIRCUIT CONFIGURATION vs V_{OUT}

V_{OUT} (V)	L (µH)	C_2 (µF)	R_2 (kΩ)	C_3 (pF)	R_3 (kΩ)
0.8	2.2	10	0	N/A	100
1.0	2.2	10	44.2	470	178
1.2	2.2	10	80.6	270	162
1.5	2.2	10	84.5	270	97.6
1.8	2.2	10	100	220	80.6
2.5	2.2~3.3	10~22	100	220	47.5
2.8	2.2~3.3	10~22	100	220	40.2
3.3	2.2~3.3	10~22	102	220	32.4

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.