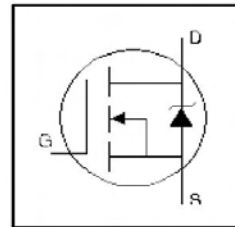


# IRL630PbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4V \text{ \& } 5V$
- 150°C Operating Temperature
- Fast Switching
- Ease of paralleling
  - Lead-Free

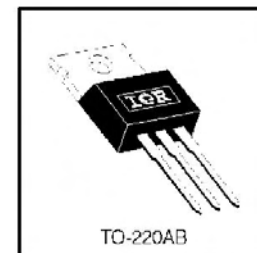


$V_{DSS} = 200V$
$R_{DS(on)} = 0.40\Omega$
$I_D = 9.0A$

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.




## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0V$	9.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0V$	5.7	
$I_{DM}$	Pulsed Drain Current ①	36	
$P_D @ T_C = 25^\circ C$	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	250	mJ
$I_{AR}$	Avalanche Current ①	9.0	A
$E_{AR}$	Repetitive Avalanche Energy ①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

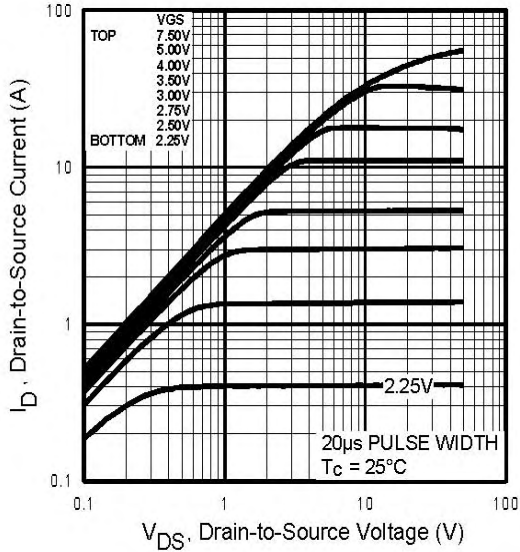
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(ON)</sub>	Static Drain-to-Source On-Resistance	—	—	0.40	Ω	V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 5.4A ②
		—	—	0.50		V <sub>GS</sub> = 4.0V, I <sub>D</sub> = 4.5A ②
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	4.8	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 5.4A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 10V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -10V
Q <sub>g</sub>	Total Gate Charge	—	—	40	nC	I <sub>D</sub> = 9.0A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	5.5		V <sub>DS</sub> = 160V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	24		V <sub>GS</sub> = 10V, See Fig. 6 and 13 ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.0	—	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	57	—		I <sub>D</sub> = 9.0A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	38	—		R <sub>G</sub> = 6.0Ω
t <sub>f</sub>	Fall Time	—	33	—		R <sub>D</sub> = 11Ω, See Fig. 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	1100	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	220	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	70	—		f = 1.0MHz, See Fig. 5

## Source-Drain Ratings and Characteristics

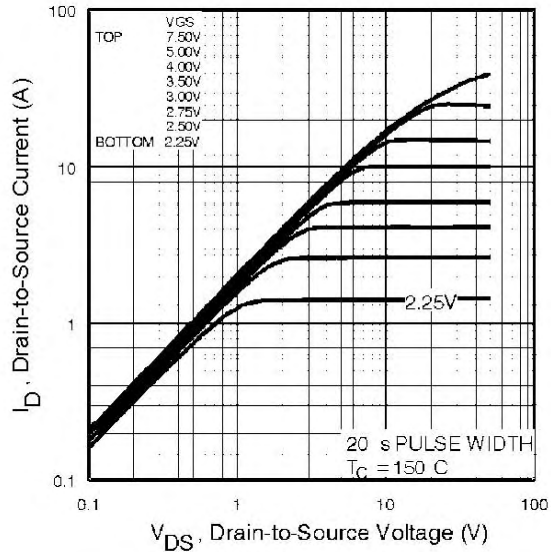
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	9.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	36		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 9.0A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	230	350	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 9.0A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.7	2.6	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

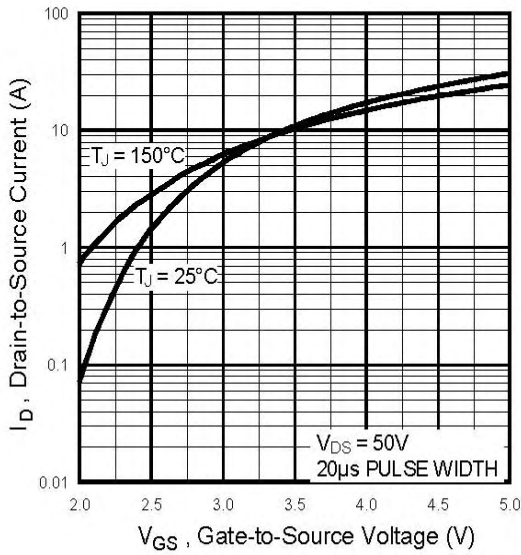
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 4.6mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 9.0A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 9.0A, di/dt ≤ 120A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.



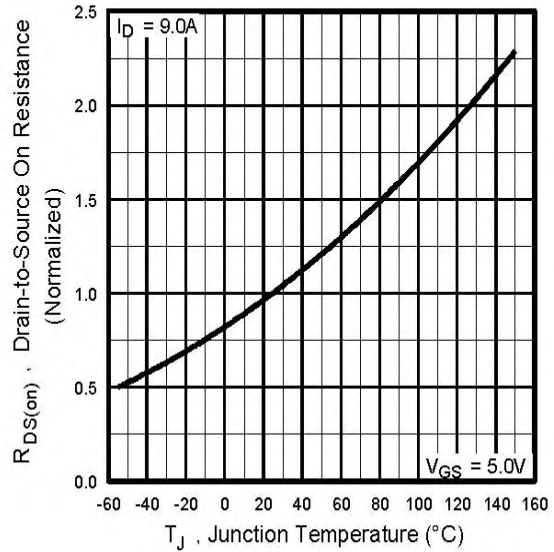
**Fig 1.** Typical Output Characteristics,  
 $T_C = 25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C = 150^\circ\text{C}$



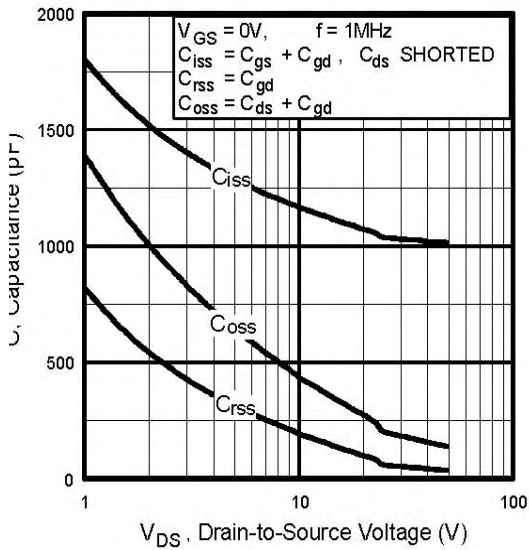
**Fig 3.** Typical Transfer Characteristics



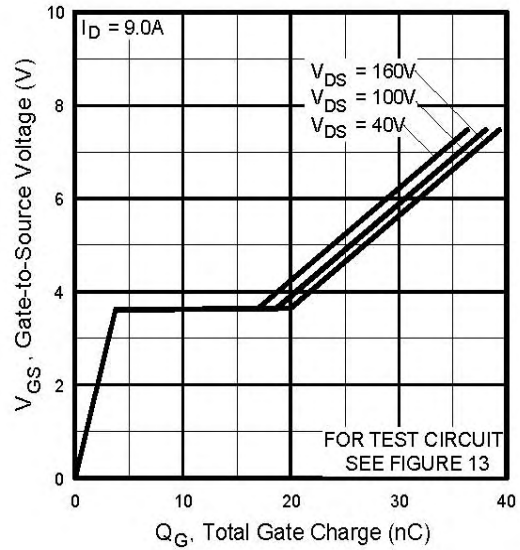
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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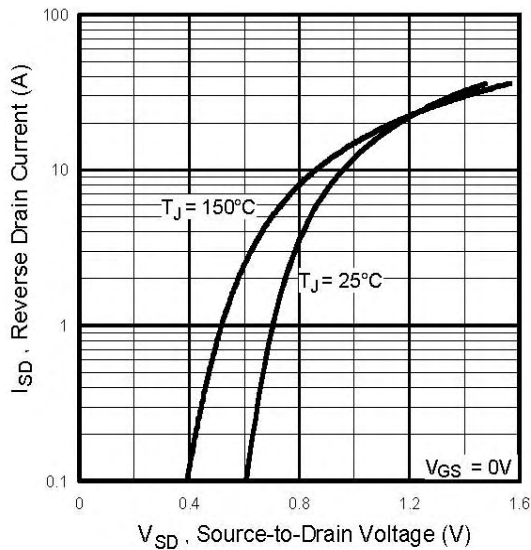
International  
**IRF** Rectifier



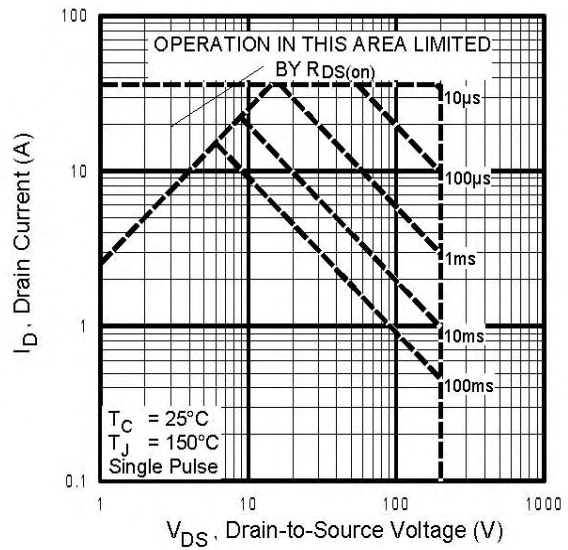
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



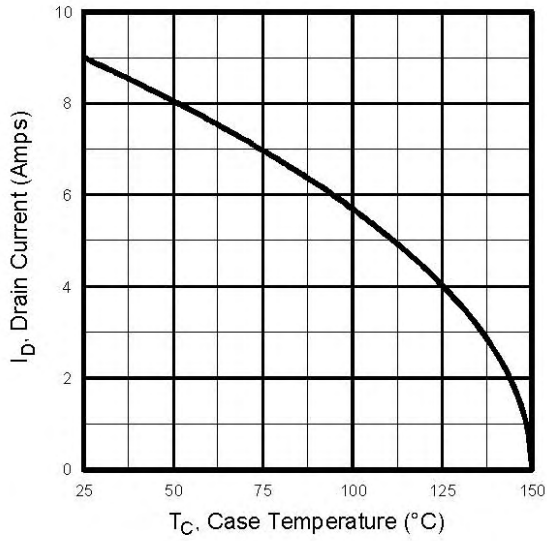
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



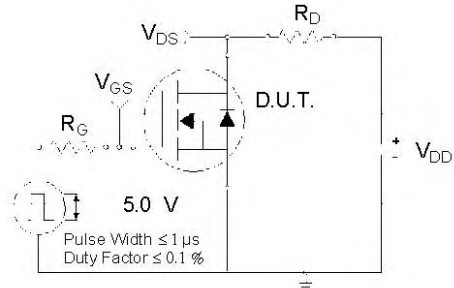
**Fig 7.** Typical Source-Drain Diode Forward Voltage



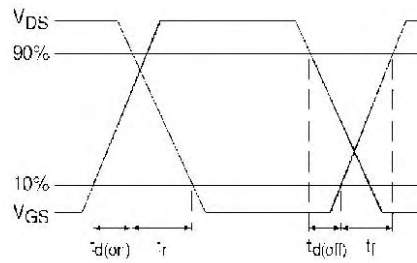
**Fig 8.** Maximum Safe Operating Area



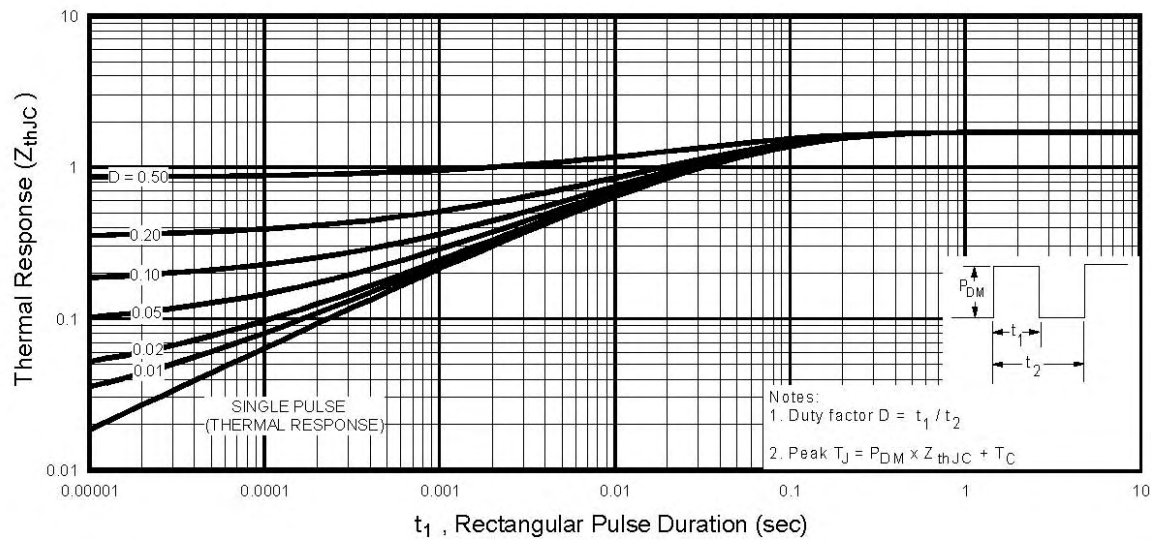
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



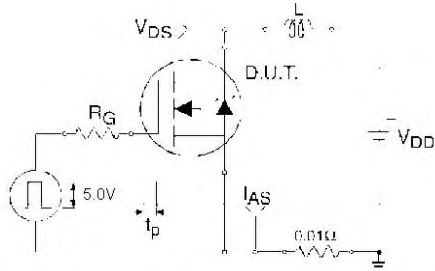
**Fig 10b.** Switching Time Waveforms



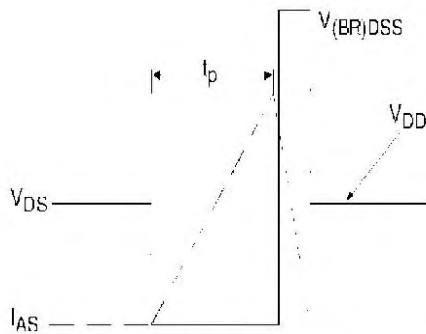
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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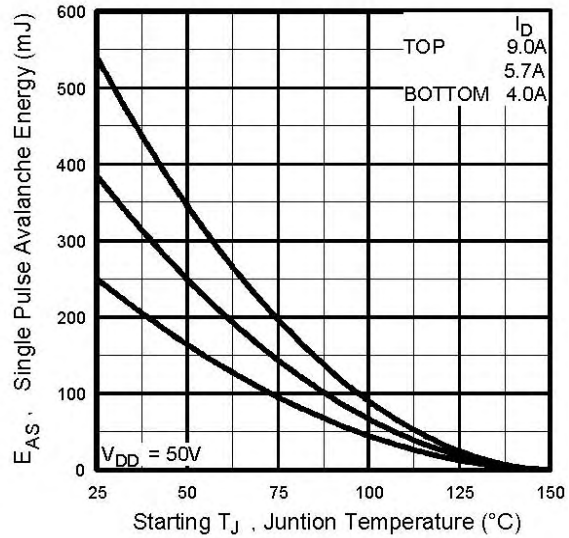
International  
**IR** Rectifier



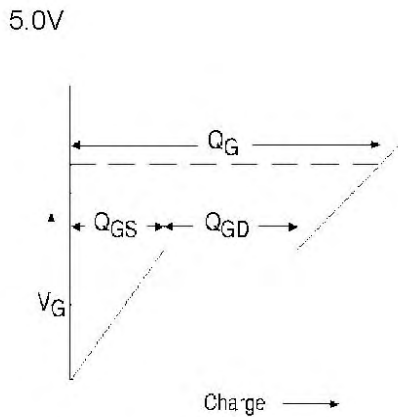
**Fig 12a.** Unclamped Inductive Test Circuit



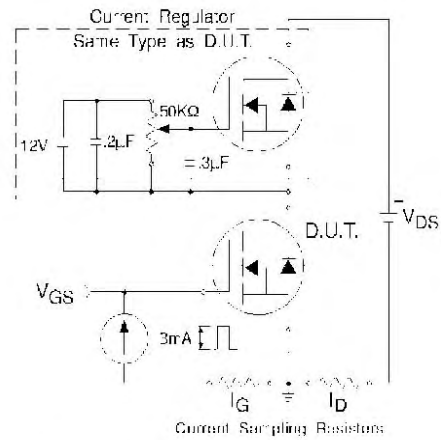
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



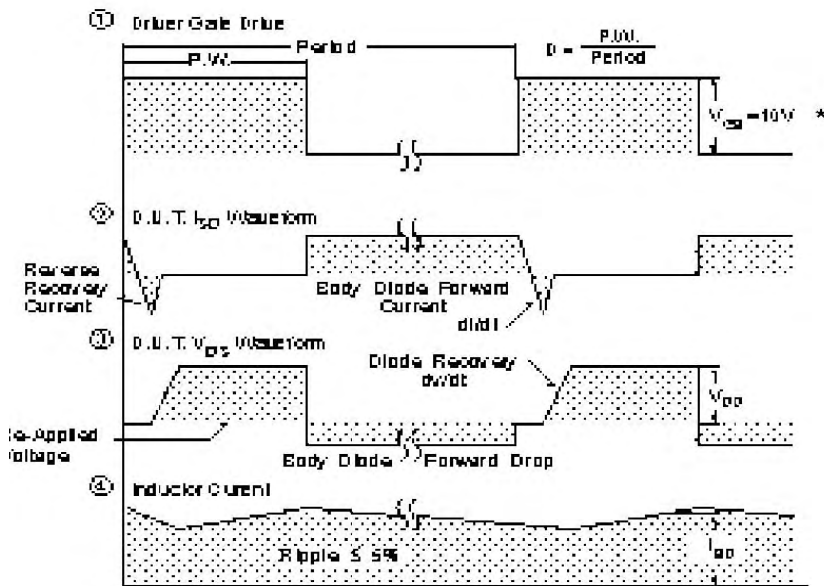
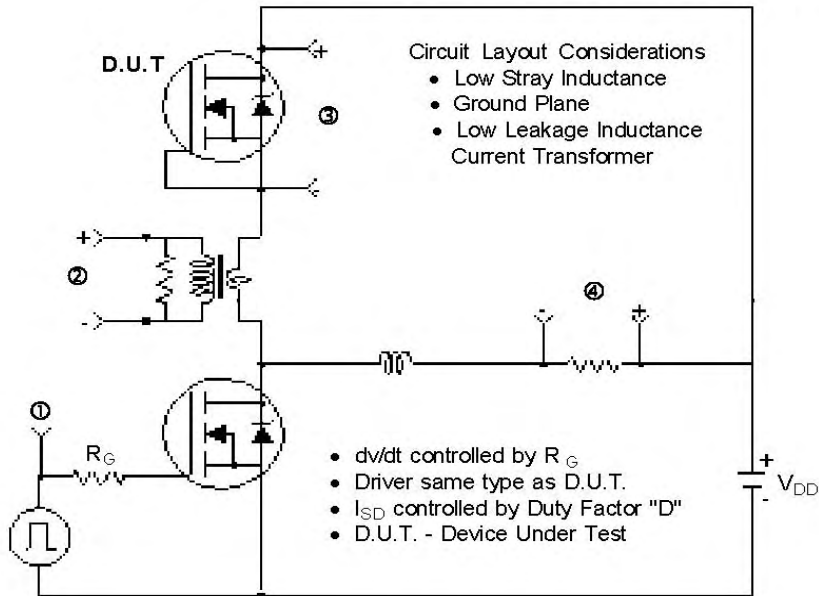
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

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**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

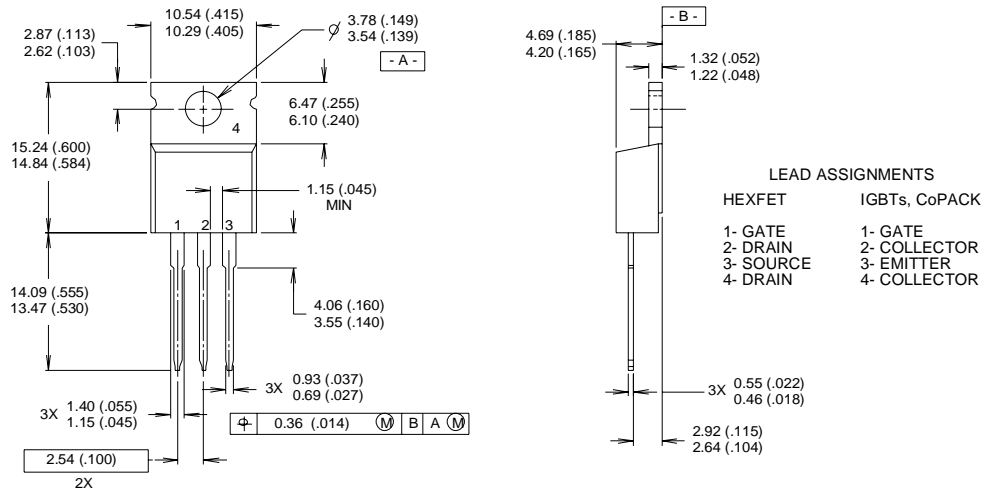
**Fig 14.** For N-Channel HEXFETS

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## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

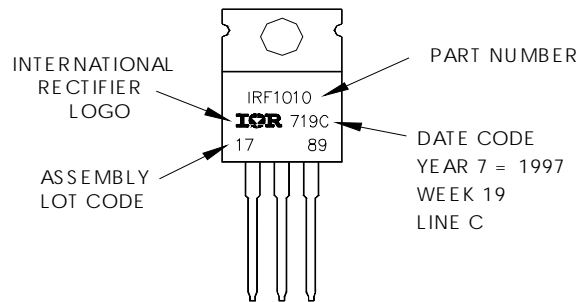


**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International  
**IR** Rectifier

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 TAC Fax: (310) 252-7903

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