HMC608LC4

v01.0707

GaAs PHEMT MEDIUM POWER AMPLIFIER, 9.5 - 11.5 GHz

Typical Applications

The HMC608LC4 is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios
- Military End-Use

Features

Output IP3: +33 dBm

Saturated Power: +27.5 dBm @ 23% PAE

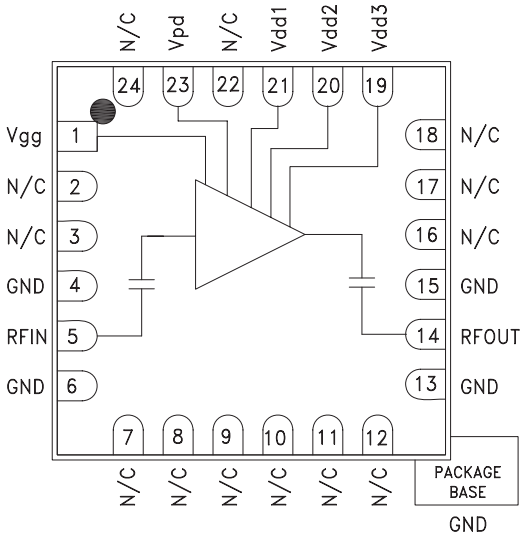
Gain: 29.5 dB

Supply: +5.0V @ 310 mA

50 Ohm Matched Input/Output

RoHS Compliant 4x4 mm SMT Package

Functional Diagram



General Description

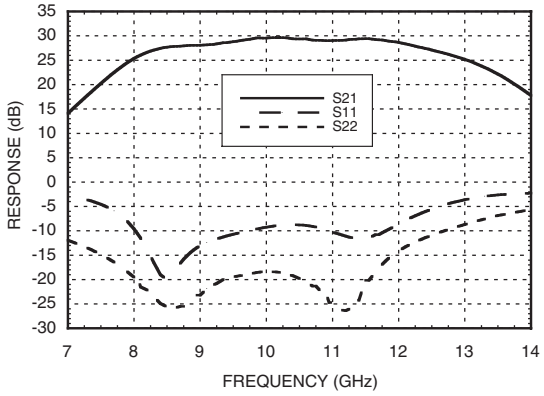
The HMC608LC4 is a high dynamic range GaAs PHEMT MMIC Medium Power Amplifier housed in a leadless “Pb free” SMT package. The amplifier has two modes of operation: high gain mode (Vpd pin shorted to ground); and low gain mode (Vpd pin left open). The electrical specifications in the table below are shown for the amplifier operating in high gain mode. Operating from 9.5 to 11.5 GHz, the amplifier provides 29.5 dB of gain, +27.5 dBm of saturated power and 23% PAE from a +5.0 V supply voltage. Noise figure is 6 dB while output IP3 is +33 dBm. The RF I/Os are DC blocked and matched to 50 Ohms for ease of use. The HMC608LC4 eliminates the need for wire bonding, allowing use of surface mount manufacturing techniques.

Electrical Specifications, T_A = +25° C, Vdd1, 2, 3 = 5V, Idd = 310 mA [1], Vpd = GND [2]

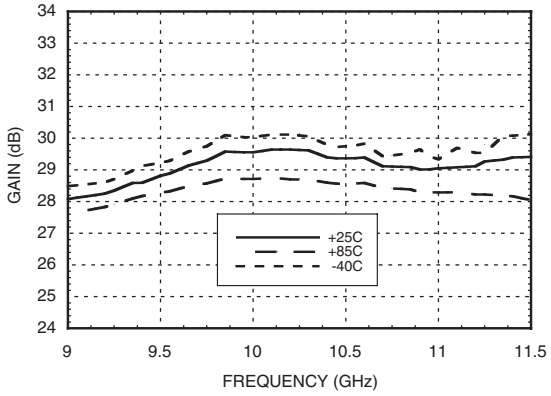
Parameter	Min.	Typ.	Max.	Units
Frequency Range		9.5 - 11.5		GHz
Gain [3]	27	29.5		dB
Gain Variation Over Temperature		0.02	0.03	dB/ °C
Input Return Loss		13		dB
Output Return Loss		19		dB
Output Power for 1 dB Compression (P1dB)	23	27		dBm
Saturated Output Power (Psat)		27.5		dBm
Output Third Order Intercept (IP3)		33		dBm
Noise Figure		6.0		dB
Supply Current (Idd = Idd1 +Idd2 +Idd3)(Vdd = +5V, Vgg = -2.6V Typ.) [3]		310	350	mA

[[1] Adjust Vgg between -3 to 0V to achieve Idd = 310 mA typical.
[2] Vpd= ground for high gain mode, Vpd = open for low gain mode.
[3] In low gain mode, typical gain is 22 dB and typical current is 67 mA.

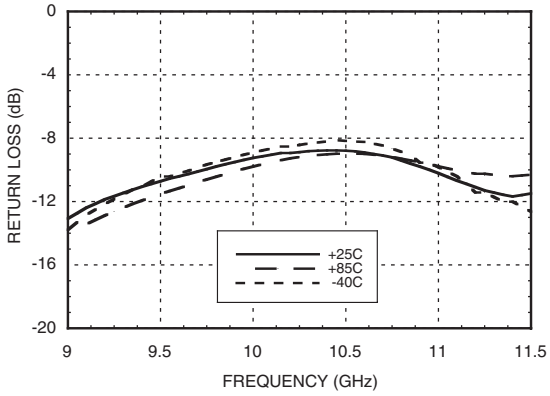
Broadband Gain & Return Loss



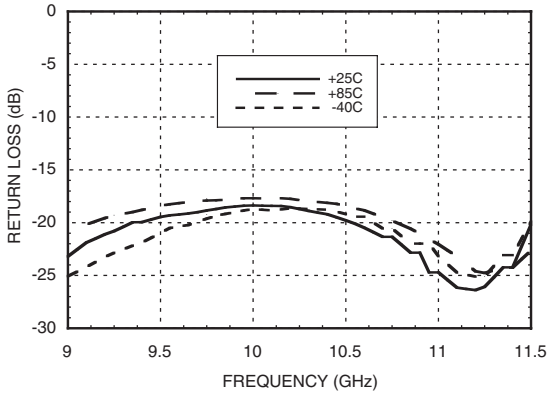
Gain vs. Temperature



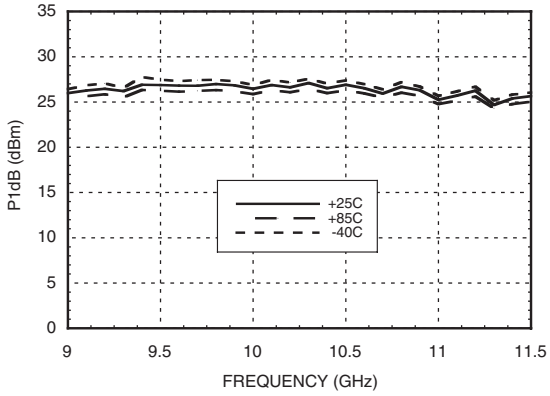
Input Return Loss vs. Temperature



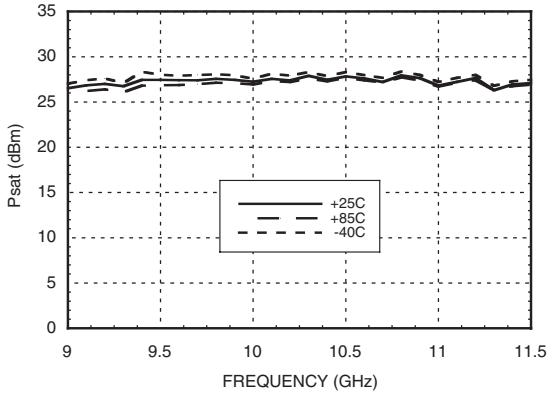
Output Return Loss vs. Temperature



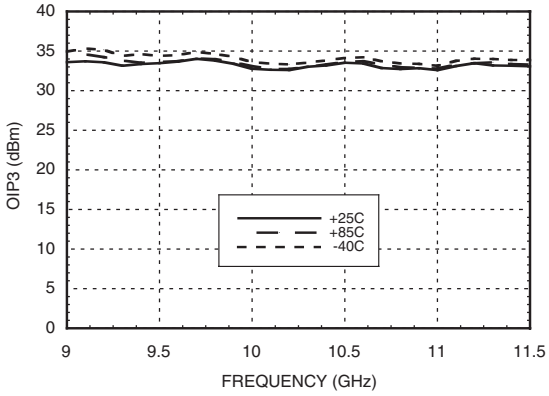
P1dB vs. Temperature



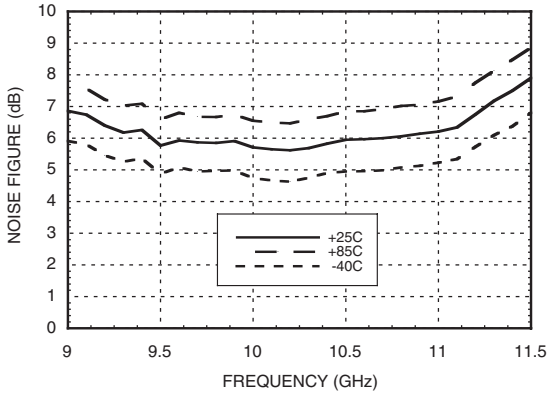
Psat vs. Temperature



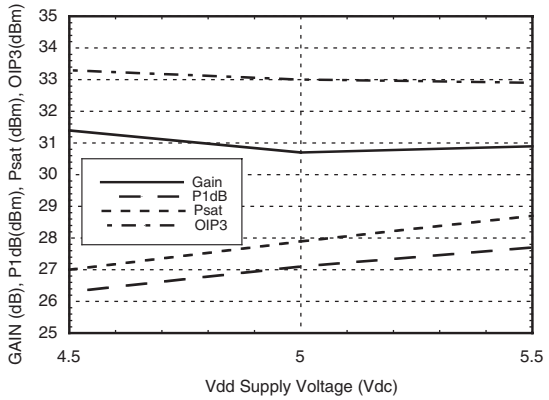
Output IP3 vs. Temperature



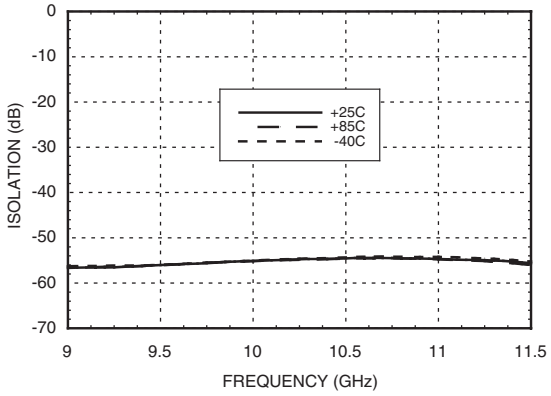
Noise Figure vs. Temperature



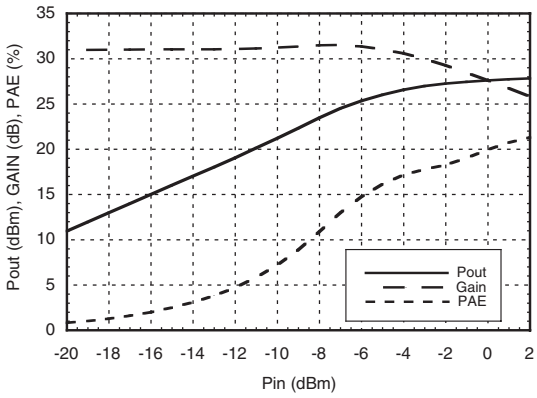
Gain, Power & OIP3 vs. Supply Voltage @ 10.3 GHz



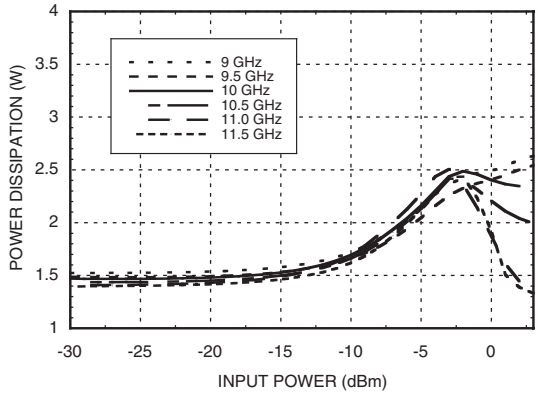
Reverse Isolation vs. Temperature



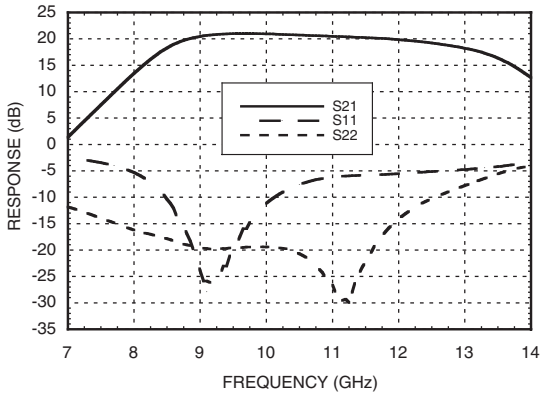
Power Compression @ 10.3 GHz



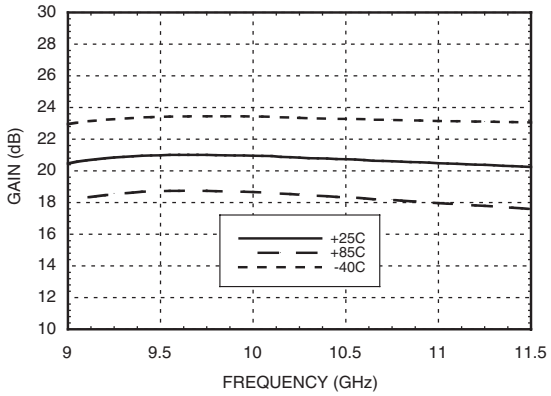
Power Dissipation



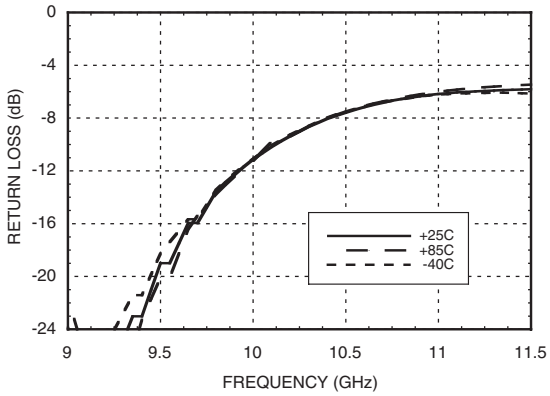
Low Gain Mode, Broadband Gain & Return Loss



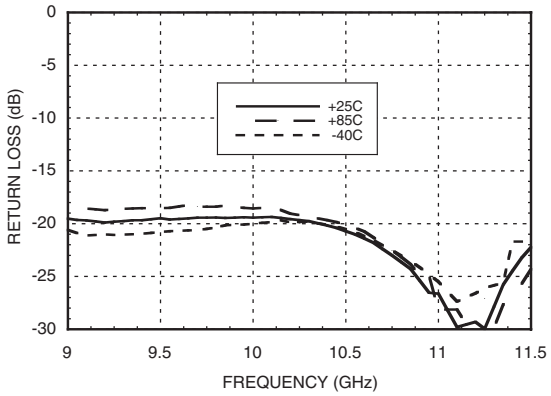
Low Gain Mode, Gain vs. Temperature



Low Gain Mode, Input Return Loss vs. Temperature



Low Gain Mode, Output Return Loss vs. Temperature



HMC608LC4

GaAs PHEMT MEDIUM POWER AMPLIFIER, 9.5 - 11.5 GHz

Absolute Maximum Ratings

Drain Bias Voltage (Vdd1, Vdd2, Vdd3)	7 Vdc
Gate Bias Voltage (Vgg)	-4.0 to -1.0 Vdc
RF Input Power (RFin)(Vdd = +5.0 Vdc)	+10 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 22.18 mW/°C above 85 °C)	2 W
Thermal Resistance (channel to ground paddle)	45 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

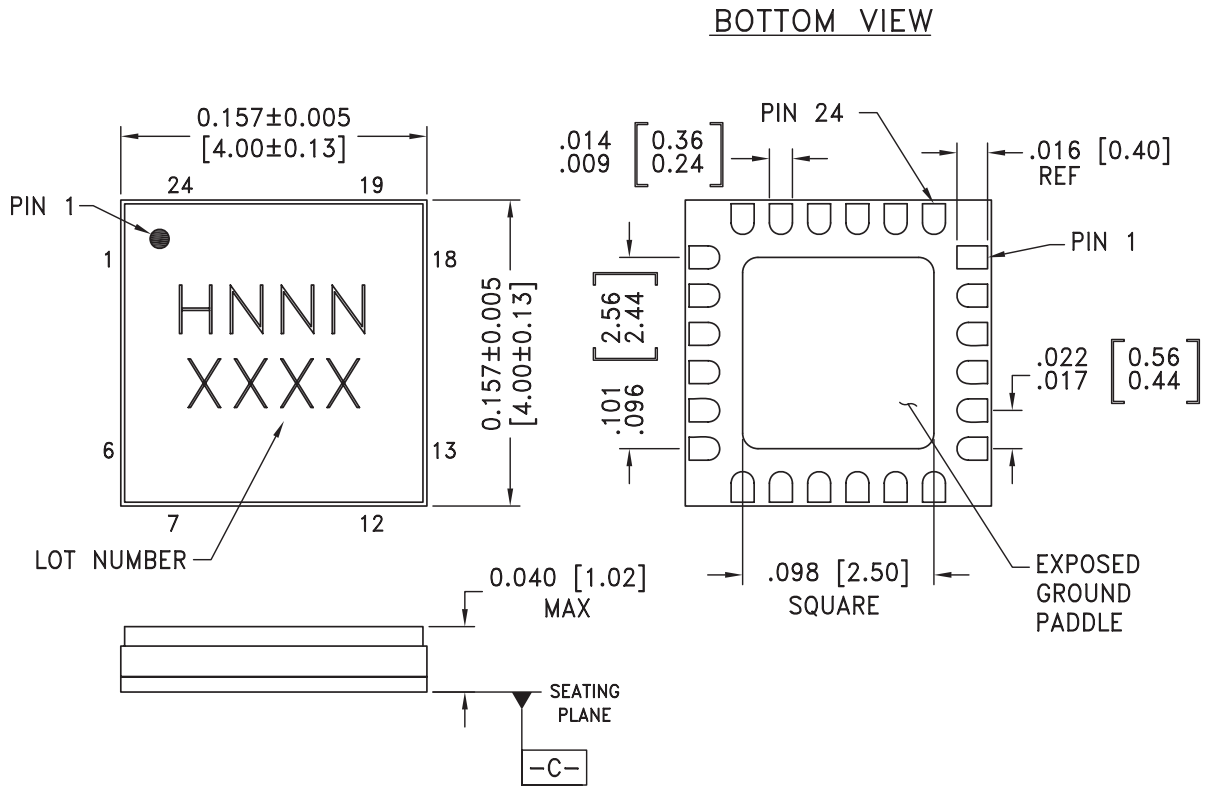
Typical Supply Current vs. Vdd

Vdd (Vdc)	Idd (mA)
+4.5	300
+5.0	310
+5.5	325

Note: Amplifier will operate over full voltage ranges shown above. Vgg adjusted to achieve Idd= 310 mA at +5.0V.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

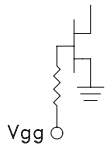
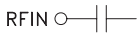
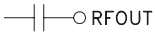
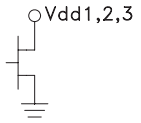
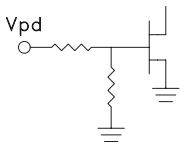
Outline Drawing



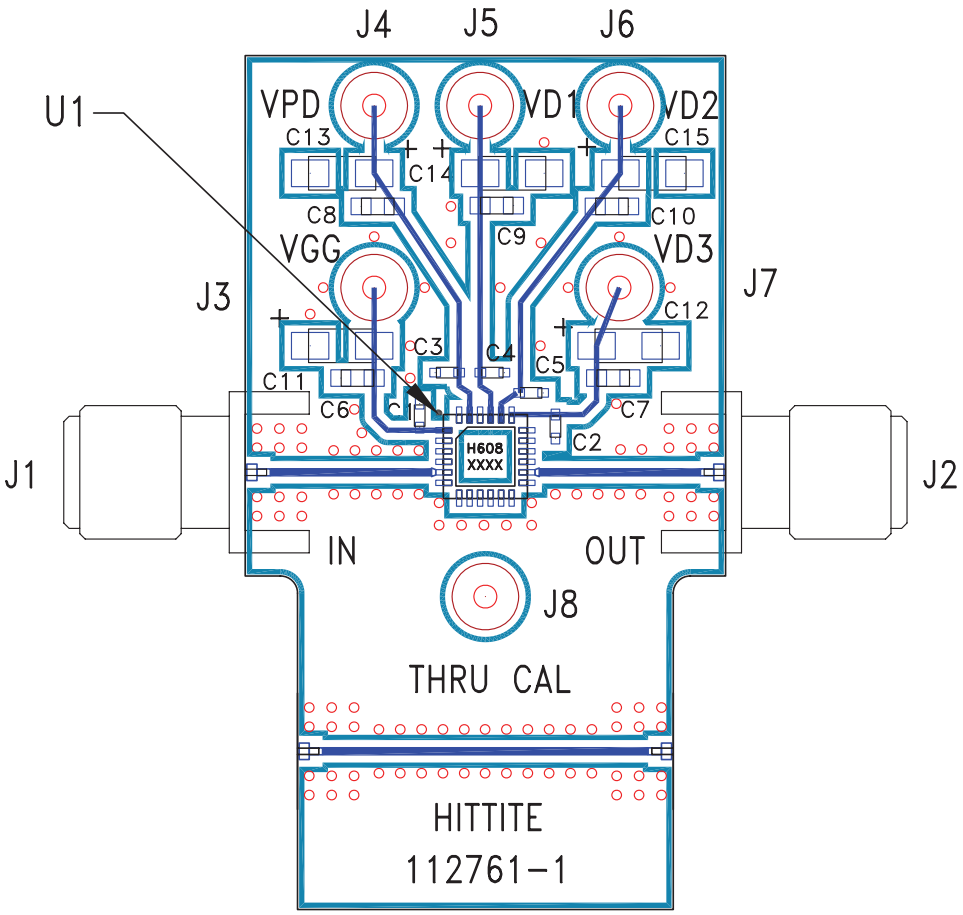
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA.
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL
3. DIMENSIONS ARE IN INCHES (MILLIMETERS).
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, BLACK INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
6. PACKAGE WARP SHALL NOT EXCEED 0.05MM DATUM –C–
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vgg	Gate control for amplifier. Adjust to achieve Id of 310 mA. Please follow "MMIC Amplifier Biasing Procedure" Application Note. External bypass capacitors of 100 pF, 1000 pF and 2.2 µF are required.	
2, 3, 7 - 12, 16 - 18, 22, 24	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
4, 6, 13, 15	GND	Package bottom has an exposed metal paddle that must also be connected to RF/DC ground.	
5	RFIN	This pin is AC coupled and matched to 50 Ohms.	
14	RFOUT	This pin is AC coupled and matched to 50 Ohms.	
21, 20, 19	Vdd1, Vdd2, Vdd3	Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1000pF, and 2.2 µF are required.	
23	Vpd	High gain (connect to ground) / low gain mode pin control (open circuit). External bypass capacitors of 100 pF, 1000 pF and 2.2 µF are required.	

Evaluation PCB



List of Materials for Evaluation PCB 112763 [1]

Item	Description
J1, J2	PC mount SMA connector
J3 - J8	DC Pin
C1 - C6	100 pF capacitor, 0402 pkg.
C6 - C10	1,000 pF Capacitor, 0603 pkg.
C11 - C15	2.2µF Capacitor, Tantalum
U1	HMC608LC4 Amplifier
PCB [2]	112761 Evaluation PCB

[1] Reference this number when ordering complete evlaution PCB

[2] Circuit Board Material: Rogers 4350.

The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

Notes: