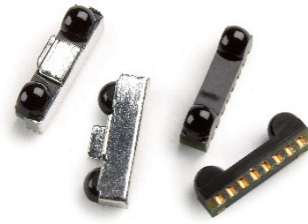


ASDL-3023

IrDA® Data Compliant Low Power 4Mbit/s
with Remote Control Infrared Transceiver



Data Sheet

Description

The ASDL-3023 is a new generation low profile high speed enhanced infrared (IR) transceiver module that provides the capability of (1) interface between logic and IR signals for through-air, serial, half-duplex IR data link, and (2) IR remote control transmission for universal remote control applications. The ASDL-3023 can be used for IrDA as well as remote control application without the need of any additional external components for multiplexing.

The ASDL-3023 is fully compliant to IrDA® Physical Layer specification version 1.4 low power from 9.6 kbit/s to 4.0 Mbit/s (FIR) and IEC825 Class 1 eye safety standards.

The ASDL-3023 can be shutdown completely to achieve very low power consumption. In the shutdown mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. It is also designed to interface to input/output logic circuits as low as 1.5V. These features are ideal for battery operated mobile devices such as PDAs and mobile phones that require low power consumption.

Applications

Mobile data communication and universal remote control

- Mobile Phones
- PDAs
- Digital Still Camera
- Printer
- Handy Terminal
- Industrial and Medical Instrument

Application Support Information

The Application Engineering Group is available to assist you with the application design associated with ASDL-3023 infrared transceiver module. You can contact them through your local sales representatives for additional details.

Features

General Features

- Operating temperature from -25° C ~ 85° C
 - Critical parameters are guaranteed over temperature and supply voltage
- Vcc Supply 2.4 to 3.6 V
- Interface to Various Super I/O and Controller Devices
 - Input/Output Interface Voltage of 1.5 V
- Miniature Package Miniature Package (shielded)
Height : 1.75 mm Height : 1.95 mm
Width : 7.5 mm Width : 8.0 mm
Depth : 2.75 mm Depth : 3.00 mm
- Moisture Level 3
- Power Saving using 3 ILED range (SIR, MIR/FIR, RC mode)
- LED stuck high protection
- High EMI Performance
- High ESD Performance
- Designed to Accommodate Light Loss with Cosmetic Windows
- IEC 825-Class 1 Eye Safe

IrDA® Features

- Fully Compliant to IrDA 1.4 Physical Layer Low Power Specifications from 9.6 kbit/s to 4.0 Mb/s
 - Link distance up to 30cm (minimum)
- Complete shutdown
- Low Power Consumption
 - Low shutdown current
 - Low idle current

Remote Control Features

- Wide angle and high radiant intensity
- Spectrally suited to remote control transmission function
- Minimum peak wavelength of 880nm
- 2 RC Transmission Mode
 - Single TXD (Programmable Mode)
 - Dual TXD (Direct)

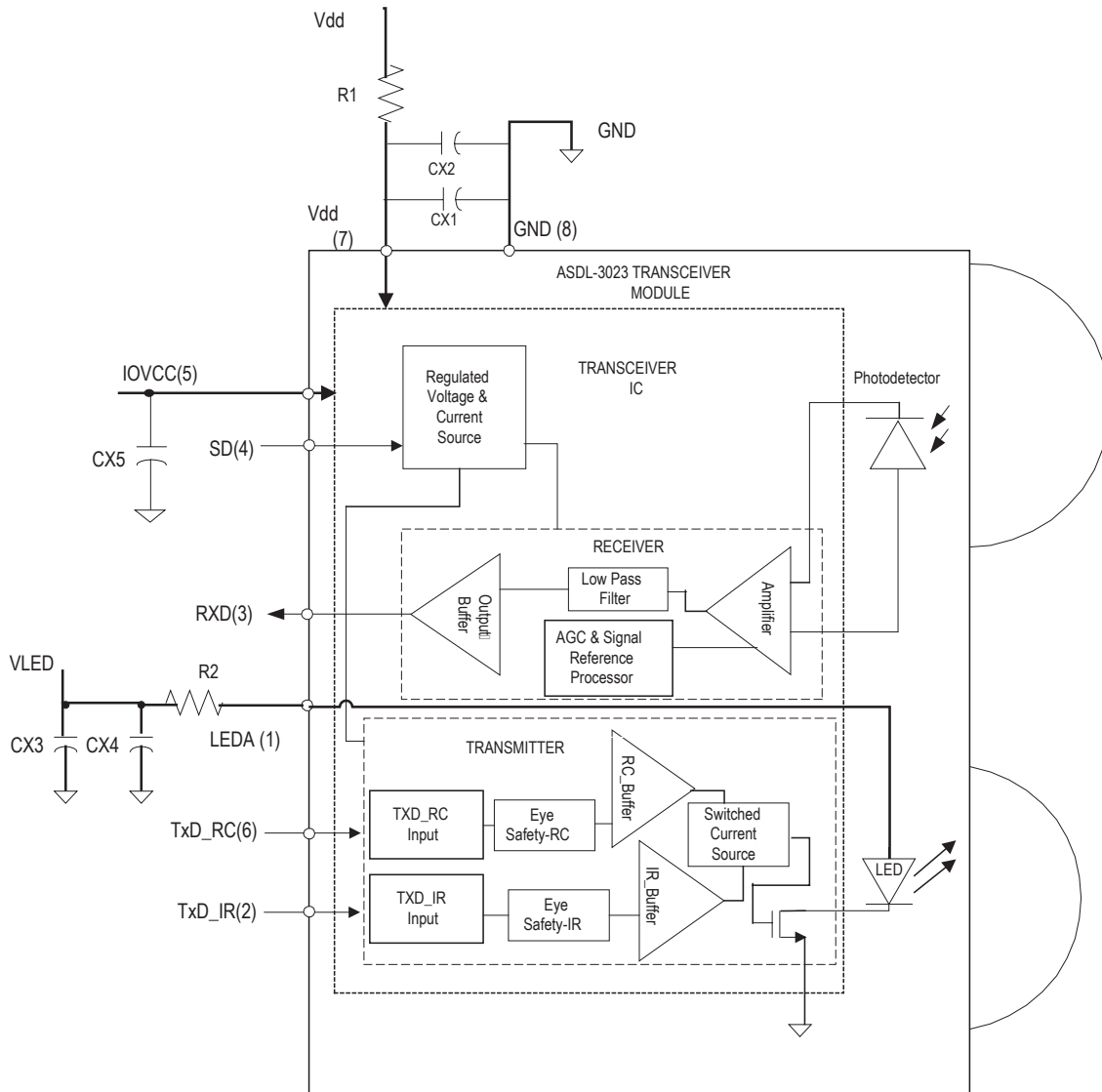


Figure 1a. Functional Block Diagram of ASDL-3023

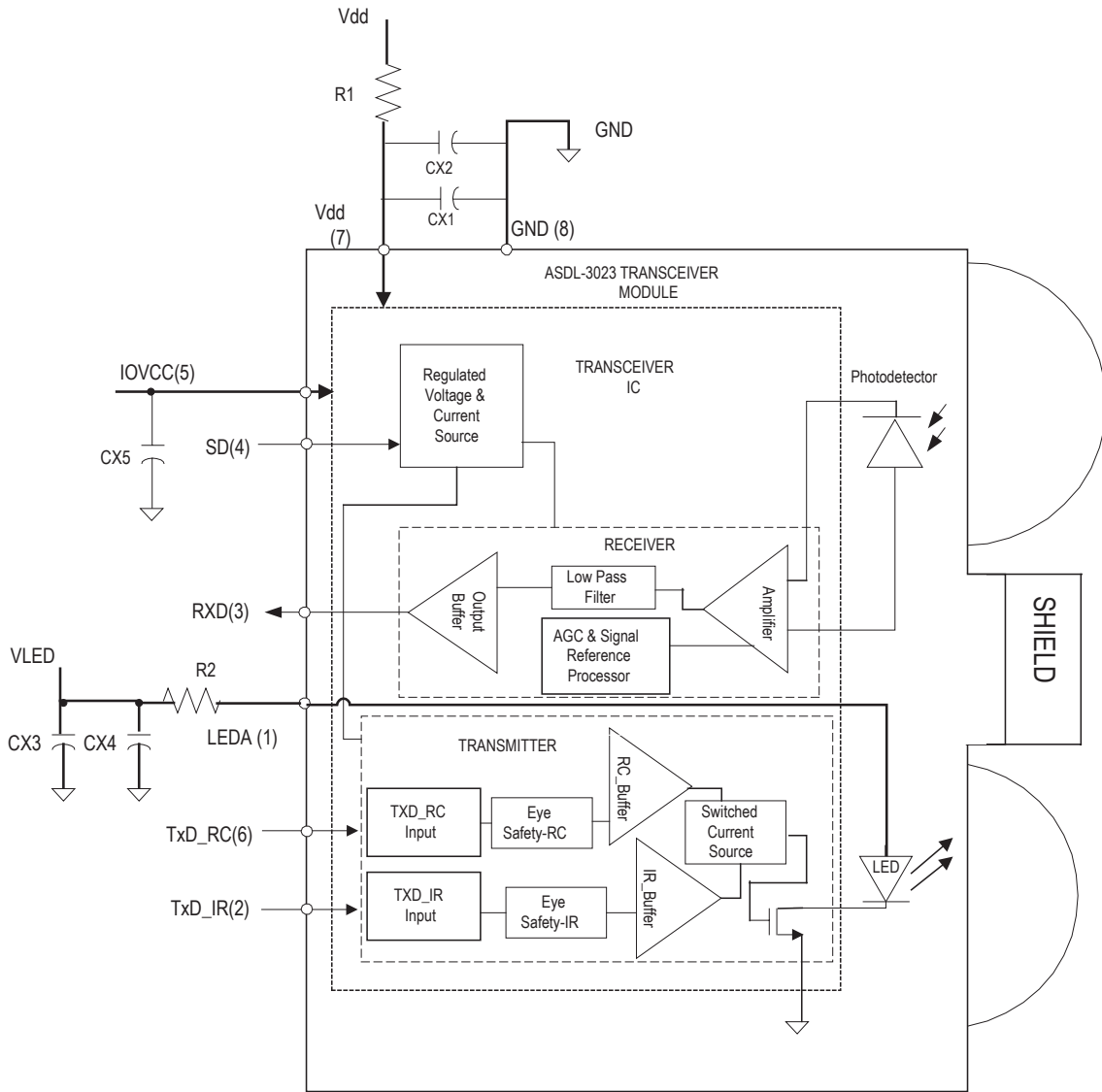


Figure 1b. Functional Block Diagram of ASDL-3023-S21

Order Information

Part Number	Packaging Type	Package	Quantity
ASDL-3023-021	Tape and Reel	Front Option	2500
ASDL-3023-008	Tape and Reel	Top Option	2500
ASDL-3023-S21 (Shielded)	Tape and Reel	Front Option	2500

Marking Information

The unit is marked with 'XYWLL' on the shield

Y = year

W = work week

LL = lot number

ASDL-3023-021, ASDL-3023-008 and ASDL-3023-S21

Pinout, Rear View

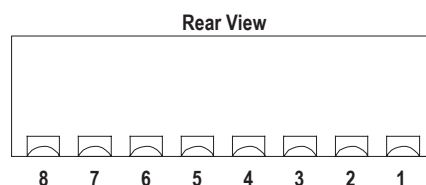


Figure 2a. Pin out for ASDL-3023-021 and ASDL-3023-008,

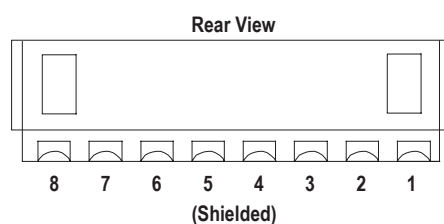


Figure 2b. Pin out for ASDL-3023-S21

I/O Pins Configuration Table

Pin	Symbol	Description	I/O Type	Notes
1	LEDA	LED Anode		Note 1
2	TxD_IR	IrDA transmitter data input.	Input. Active High	Note 2
3	RxD	IrDA receive data	Output. Active Low	Note 3
4	SD	Shutdown	Input. Active High	Note 4
5	IOVCC	Input/Output ASIC voltage		Note 5
6	TxD_RC	RC transmitter data input.	Input. Active High	Note 6
7	VCC	Supply Voltage		Note 7
8	GND	Ground		Note 8

Notes:

1. Tied through external resistor, R2, to Vled. Refer to the table below for recommended series resistor value.
2. This pin is used to transmit serial data when SD pin is low. If held high for longer than 50 μ s, the LED is turned off. Do NOT float this pin.
3. This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. The pin is in tri-state when the transceiver is in shutdown mode
4. Complete shutdown of IC and PIN diode. The pin is used for setting IR receiver bandwidth, range of IR LED current and RC drive programming mode. Refer to section on "Bandwidth Selection Timing" and "Remote Control Drive Modes" for more information. Do NOT float this pin. ***
5. Connect to ASIC logic controller supply voltage or Vcc. The voltage at this pin should be equal to or less than Vcc.
6. Logic high turns on the RC LED. If held high longer than 50 μ s, the RC LED is turned off. Do NOT float the pin.
7. (i) Regulated, 2.4V to 3.6V
(ii) This pin recommended to turn on before other pin.
8. Connect to system ground.

Recommended Application Circuit Components

Component	Recommended Value	Note
R1	4.7Ω, ±5%, 0.25 watt for Vcc ≤ 3.0V	
R2	2.7Ω, for 2.4 ≤ VLED ≤ 2.7V; 3.3Ω, for 2.7 < VLED ≤ 3.0V 3.9Ω, for 3.0 < VLED ≤ 3.3V 4.7Ω, for 3.3 < VLED ≤ 3.6V 5.6Ω, for 3.6 < VLED ≤ 4.2V 10Ω, for 4.2 < VLED ≤ 5V	
CX1, CX3, CX5	100 nF, ± 20%, X7R Ceramic	1
CX2, CX4	4.7μF, ± 20%, Tantalum	1

Notes: CX1, CX2, CX3 & CX4 must be placed within 0.7cm of ASDL-3023 to obtain optimum noise immunity

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ± 50°C/W.

Parameter	Symbol	Min.	Max.	Units	Conditions	Ref
Storage Temperature	T _S	-40	+100	°C		
Operating Temperature	T _A	-25	+85	°C		
LED Anode Voltage	V _{LEDA}	-0.3	6.5	V		
Supply Voltage	V _{CC}	-0.3	6	V		
Input Voltage : TXD, SD/Mode	V _I	-0.3	5.5	V		
Output Voltage : RXD	V _O	-0.3	5.5	V		
Peak IR LED Current	I _{IRLED(PK)}		200	mA	≤ 25% duty cycle, ≤ 90 μs pulse width	Fig 3
Peak RC LED Current	I _{RCLED(PK)}		300	mA	≤ 10% duty cycle, ≤ 90 μs pulse width	Fig 4

CAUTION: THE CMOS INHERENT TO THE DESIGN OF THIS COMPONENT INCREASES THE COMPONENT'S SUSCEPTIBILITY TO DAMAGE FROM ELECTROSTATIC DISCHARGE (ESD). IT IS ADVISED THAT NORMAL STATIC PRECAUTIONS BE TAKEN IN HANDLING AND ASSEMBLY OF THIS COMPONENT TO PREVENT DAMAGE AND/OR DEGRADATION WHICH MAY BE INDUCED BY ESD

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature	T_A	-25		+85	°C	
Supply Voltage	V_{CC}	2.4		3.6	V	
Input/Output Voltage	IOV_{CC}	1.5		3.6	V	
Logic Input Voltage for TXD, SD/Mode	Logic High	V_{IH}	$IOV_{CC}-0.5$	IOV_{CC}	V	
	Logic Low	V_{IL}	0	0.4	V	
Receiver Input Irradiance	Logic High	E_{IH}	0.0090	500	mW/cm^2	For in-band signals $\leq 115.2kbit/s$ ^[3] 0.576 Mbit/s \leq in-band signals ≤ 4.0 Mbit/s ^[3]
			0.0225	500		
	Logic Low	E_{IL}		0.3	$\mu W/cm^2$	For in-band signals ^[3]
IR LED (Logic High) Current Pulse Amplitude – SIR Mode	I_{LEDA}		65		mA	
IR LED (Logic High) Current Pulse Amplitude – MIR/FIR Mode	I_{LEDA}		150		mA	
RC LED (Logic High) Current Pulse Amplitude	I_{LEDA}		250		mA	
Receiver Data Rate		0.0096		4.0	Mbit/s	
Ambient Light						See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels

Note :

- An in-band optical signal is a pulse/sequence where the peak wavelength, λ_p , is defined as $850 \leq \lambda_p \leq 900$ nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

Electrical and Optical Specifications

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C, Vcc set to 3.0V and IOVcc set to 1.5V unless otherwise noted.

Receiver

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Viewing Angle	$2\theta_{1/2}$	30			°	
Peak Sensitivity Wavelength	λ_p		875		nm	
RxD_IrDA Output Voltage	Logic High	V_{OH}	$IOV_{CC} - 0.5$	IOV_{CC}	V	$I_{OH} = -200 \mu A, EI \leq 0.3 \mu W/cm^2$
	Logic Low	V_{OL}	0	0.4	V	
RxD_IrDA Pulse Width (SIR) [4, 5]	$t_{RPW(SIR)}$	1		4	μs	$\theta_{1/2} \leq 15^\circ, C_L = 9pF$
RxD_IrDA Pulse Width (MIR) [4, 6]	$t_{RPW(MIR)}$	100		500	ns	$\theta_{1/2} \leq 15^\circ, C_L = 9pF$
RxD_IrDA Pulse Width (Single) (FIR) [4, 7]	$t_{RPW(FIR)}$	80		175	ns	$\theta_{1/2} \leq 15^\circ, C_L = 9pF$
RxD_IrDA Pulse Width (Double) (FIR) [4, 7]	$t_{RPW(FIR)}$	200		290	ns	$\theta_{1/2} \leq 15^\circ, C_L = 9pF$
RxD_IrDA Rise & Fall Times	t_r, t_f		60		ns	$C_L = 9pF$
Receiver Latency Time [8]	t_L			100	μs	$EI = 9.0 \mu W/cm^2$
Receiver Wake Up Time [9]	t_{RW}			200	μs	$EI = 10 mW/cm^2$

Infrared (IR) Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
IR Radiant Intensity (SIR Mode)	I_{EH}	4	20		mW/sr	$IR_{ILED} = 65mA, \theta_{1/2} \leq 15^\circ, TxD_IR \geq V_{IH}, T_A = 25^\circ C$
IR Radiant Intensity (MIR/FIR Mode)	I_{EH}	10	50		mW/sr	$IR_{ILED} = 150mA, \theta_{1/2} \leq 15^\circ, TxD_IR \geq V_{IH}, T_A = 25^\circ C$
IR Viewing Angle	$2\theta_{1/2}$	30		60	°	
IR Peak Wavelength	λ_p	850	885	900	nm	
TxD_IrDA Logic Levels	High	V_{IH}	$IOV_{CC} - 0.5$	IOV_{CC}	V	
	Low	V_{IL}	0	0.5	V	
TxD_IrDA Input Current	High	I_H	0.02		μA	$V_I \geq V_{IH}$
	Low	I_L	-0.02		μA	$0 \leq V_I \leq V_{IL}$
Wake Up Time [10]	t_{TW}		180		ns	
Maximum Optical Pulse Width [11]	$t_{PW(Max)}$		25	120	μs	
TXD Pulse Width (SIR)	$t_{PW(SIR)}$		1.6		μs	$t_{PW(TXD_IR)} = 1.6 \mu s$ at 115.2 kbit/s
TXD Pulse Width (MIR)	$t_{PW(MIR)}$		217		ns	$t_{PW(TXD_IR)} = 217 ns$ at 1.152 Mbit/s
TXD Pulse Width (FIR)	$t_{PW(FIR)}$		125		ns	$t_{PW(TXD_IR)} = 125 ns$ at 4.0 Mbit/s
TxD Rise & Fall Times (Optical)	t_r, t_f			600	ns	$t_{PW(TXD_IR)} = 1.6 \mu s$ at 115.2 kbit/s
				40	ns	$t_{PW(TXD_IR)} = 125 ns$ at 4.0 Mbit/s
IR LED Anode On-State Voltage (SIR Mode)	V_{ON} (IR_{LEDA})		2.2		V	$IR_{ILED} = 65mA, IR_{VLED} = 3.6V, R = 4.7\Omega, VI(TxD) \geq VIH$
IR LED Anode On-State Voltage (MIR/FIR Mode)	V_{ON} (IR_{LEDA})		2.1		V	$IR_{ILED} = 150mA, IR_{VLED} = 3.6V, R = 4.7\Omega, VI(TxD_IR) \geq VIH$

Remote Control (RC) Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
RC Radiant Intensity	I_{EH}		80		mW/sr	$RC_{I_{LEDA}} = 250mA$, $\theta_{1/2} \leq 15^\circ$, $TxD_RC \geq V_{IH}$, $T_A = 25^\circ C$
RC Viewing Angle	$2\theta_{1/2}$	30		60	°	
RC Peak Wavelength	λ_p	880	885	900	nm	
TxD_RC Logic Levels	High	V_{IH}	$IOV_{CC}-0.5$	IOV_{CC}	V	
	Low	V_{IL}	0	0.5	V	
TxD_RC Input Current	High	I_H	0.02	1	μA	$V_I \geq V_{IH}$
	Low	I_L	-0.02	1	μA	$0 \leq V_I \leq V_{IL}$
RC LED Anode On-State Voltage	V_{ON} (RC_LED _A)		2		V	$RC_{I_{LEDA}}=250mA$, $RC_{V_{LED}} = 3.6V$, $R = 4.7\Omega$, $V_{I(TxD_RC)} \geq V_{IH}$

Transceiver

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Current	High	I_H	0.01	1	μA	$V_I \geq V_{IH}$
	Low	I_L	-1	-0.02	1	μA
Supply Current	Shutdown	I_{CC1}		1	μA	$V_{SD} \geq IOV_{CC}-0.5$, $T_A=25^\circ C$
	Idle (Standby)	I_{CC2}	2.0	2.9	mA	$V_{I(TxD)} \leq V_{IL}$, $EI=0$
	Active	I_{CC3}	3.5		mA	$V_{I(TxD)} \geq V_{IL}$, $EI=10mW/cm^2$

Note:

- [4] An in-band optical signal is a pulse/sequence where the peak wavelength, λ_p is defined as $850\text{ nm} \leq \lambda_p \leq 900\text{ nm}$, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification version 1.4.
- [5] For in-band signals 115.2 kbit/s where $9\text{ }\mu W/cm^2 \leq EI \leq 500\text{ mW/cm}^2$.
- [6] For in-band signals 1.152 Mbit/s where $22\text{ }\mu W/cm^2 \leq EI \leq 500\text{ mW/cm}^2$.
- [7] For in-band signals 4 Mbit/s where $22\text{ }\mu W/cm^2 \leq EI \leq 500\text{ mW/cm}^2$.
- [8] Latency is defined as the time from the last TxD_IrDA light output pulse until the receiver has recovered full sensitivity.
- [9] Receiver Wake Up Time is measured from Vcc power ON to valid RxD_IrDA output.
- [10] Transmitter Wake Up Time is measured from Vcc power ON to valid light output in response to a TxD_IrDA pulse.
- [11] The Max Optical PW is defined as the maximum time which the IR LED will turn on, this is to prevent the long Turn On time for the IR LED.

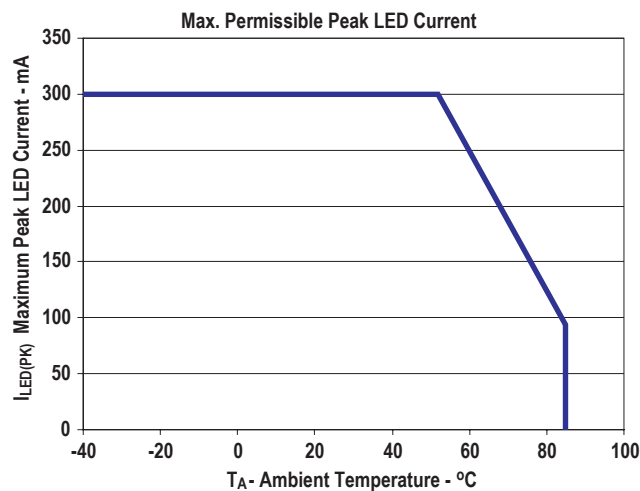


Figure 3. Maximum Peak IR LED current vs. ambient temperature. Derated based on T_{JMAX} = 100°C.

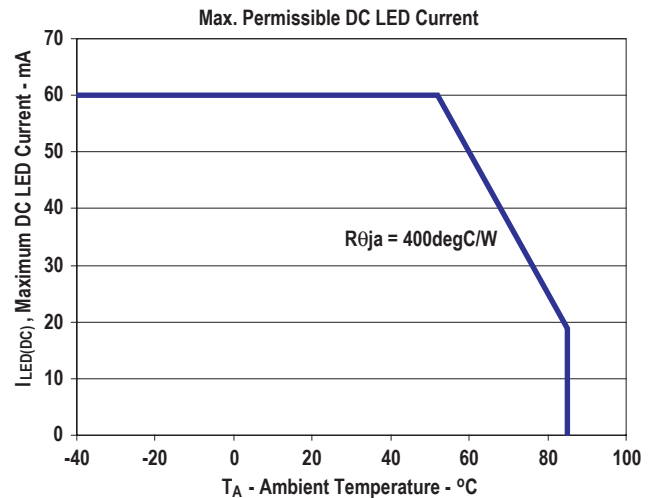


Figure 4. Maximum Peak RC LED current vs. ambient temperature. Derated based on T_{JMAX} = 100°C.

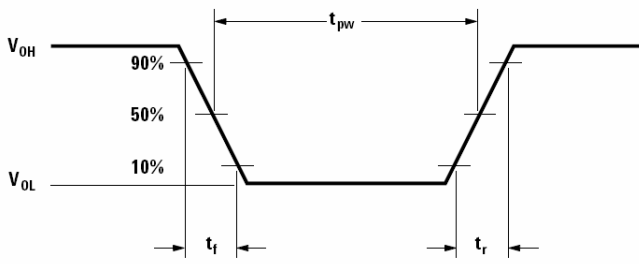


Figure 5a. Timing Waveform - RXD Output Waveform

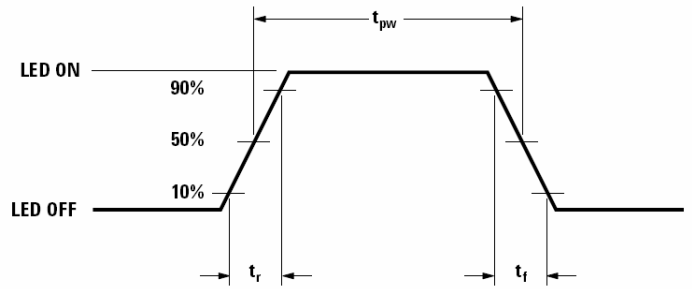


Figure 5b. Timing Waveform - LED Optical Waveform

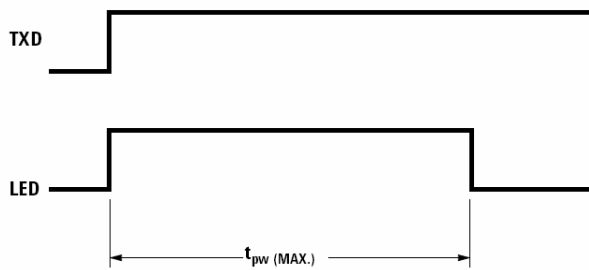


Figure 5c. Timing Waveform – TXD "Stuck-on" Protection Waveform

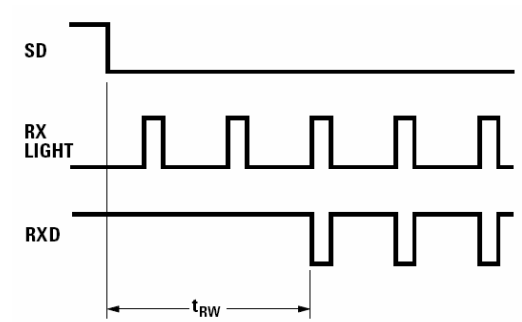


Figure 5d. Timing Waveform – Receiver Wakeup Time Waveform

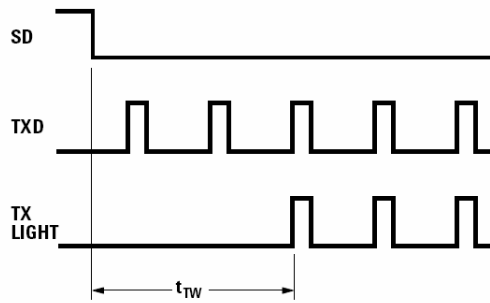
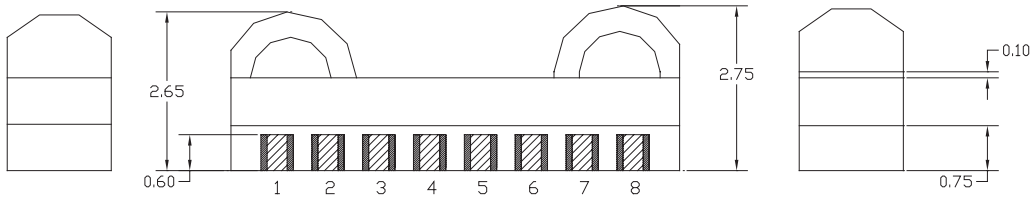
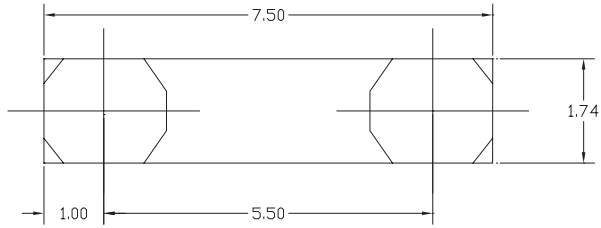
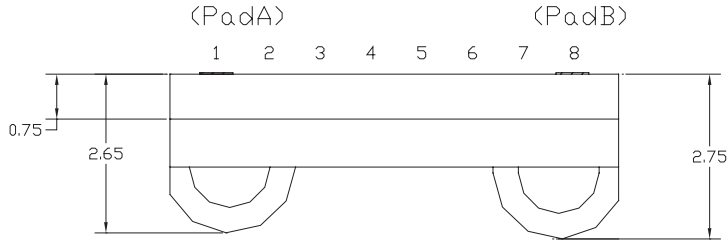


Figure 5e. Timing Waveform – TXD Wakeup Time Waveform

Package Dimension: ASDL-3023-021 (Shieldless, Front) and ASDL-3023-008 (Shieldless, Top)

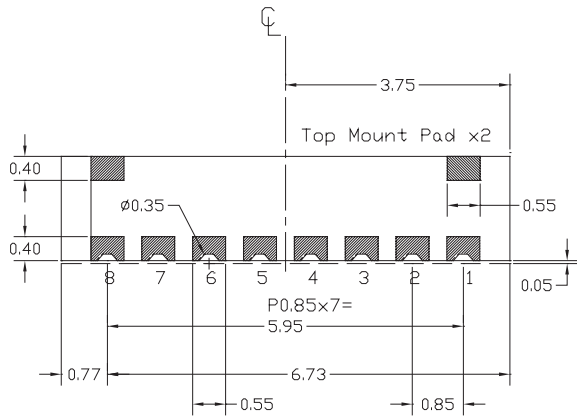


PIN ASSIGNMENT:

- 1=LEDA
- 2=TXD_IR
- 3=RXD
- 4=SD
- 5=IOVCC
- 6=TXD_RC
- 7=VDD
- 8=GND

Note:
Top Mount Enable Mount Pad x2 at location opposite Pin 1 and Pin 8.

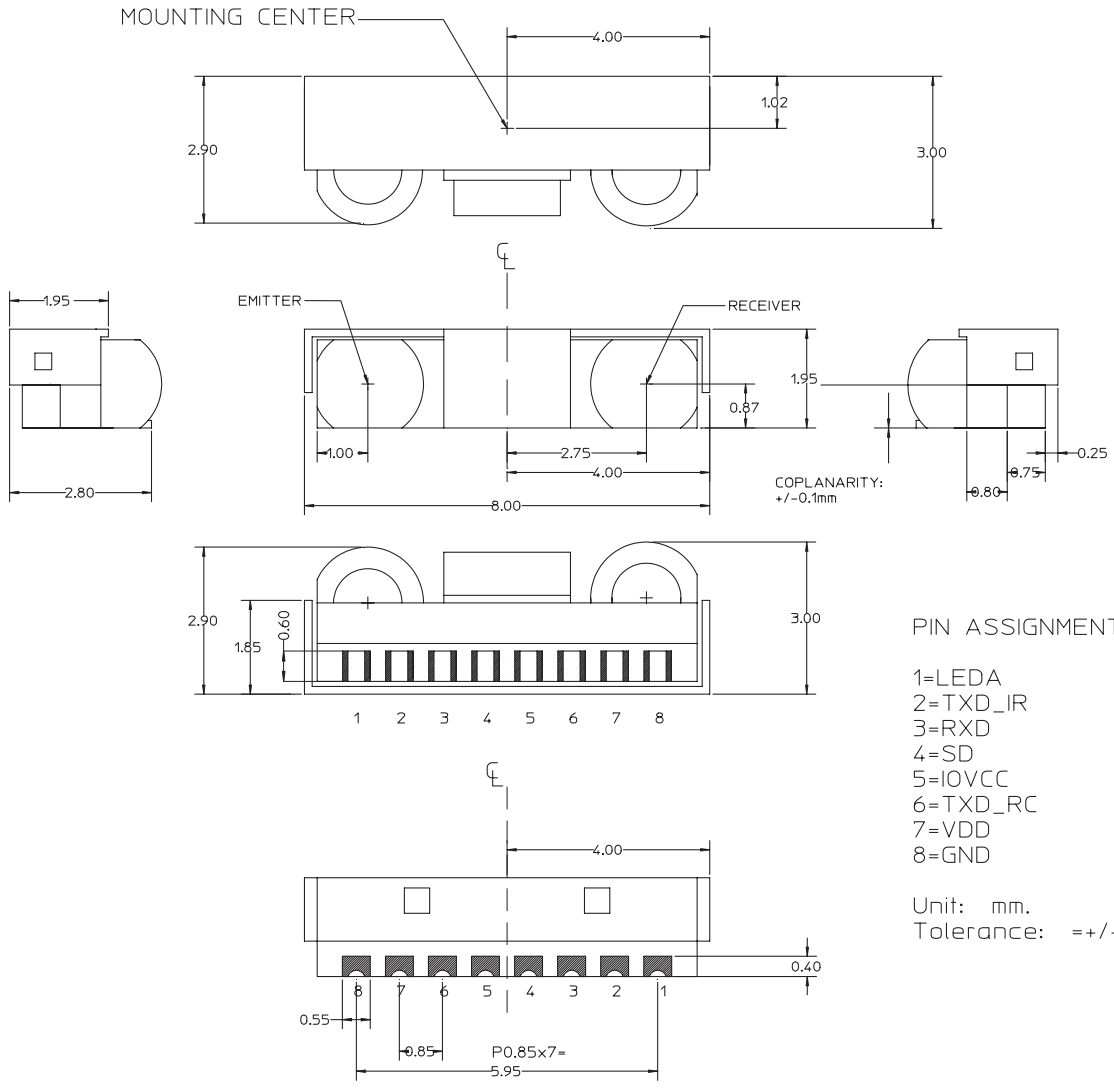
Unit: mm.
Tolerance: ± 0.2 mm.



Remarks:

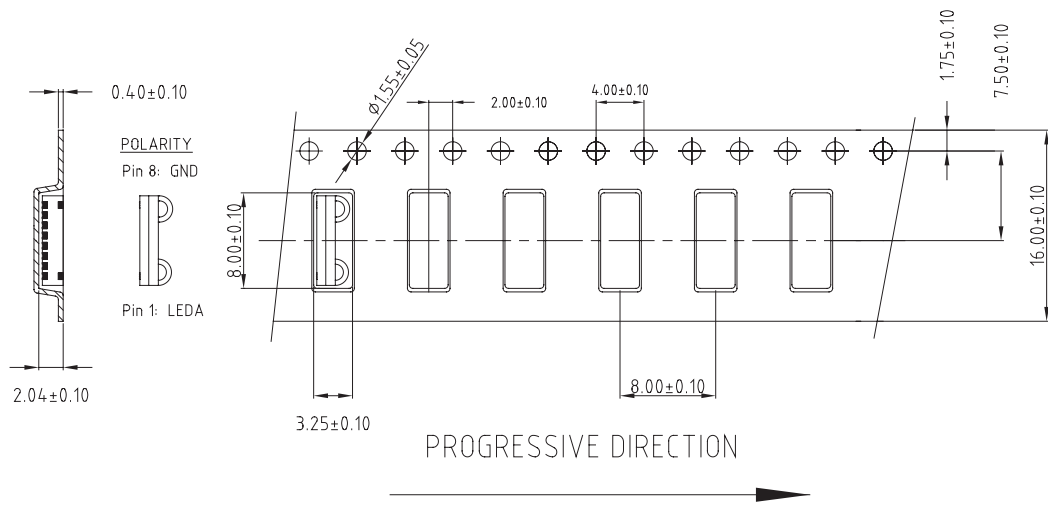
- 1) Top Mount Enable Pads (x2) opposite site of castellation holes.
- 2) These pads are not plated through vias, but only surface pads.
- 3) Pad A: Opposite of Pin1; isolated.
Pad B: Opposite of Pin8, interconnected to Pin8/Gnd.

Package Dimension: ASDL-3023-S21 (Shielded, Front)

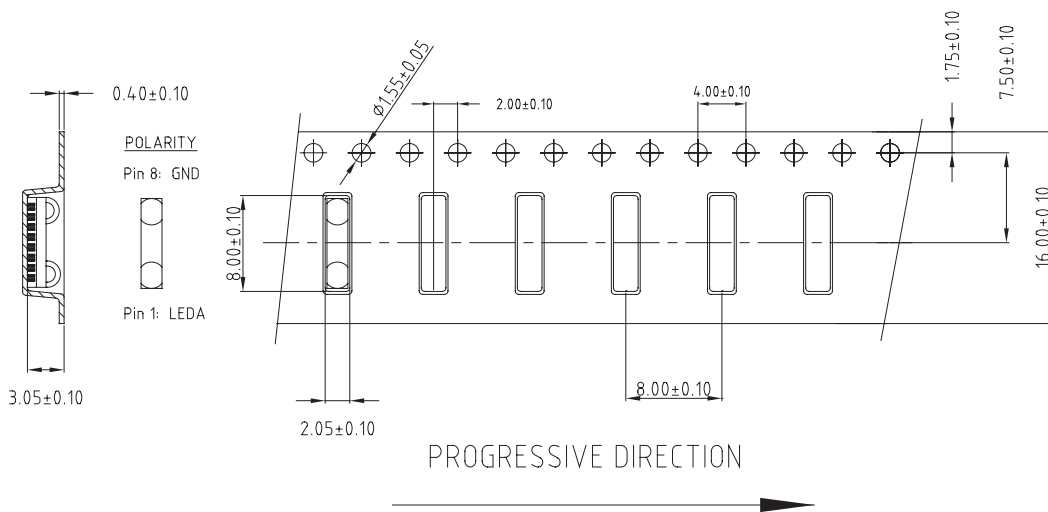


Tape & Reel Dimensions

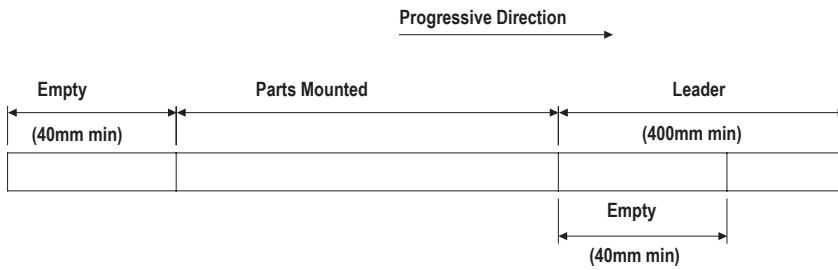
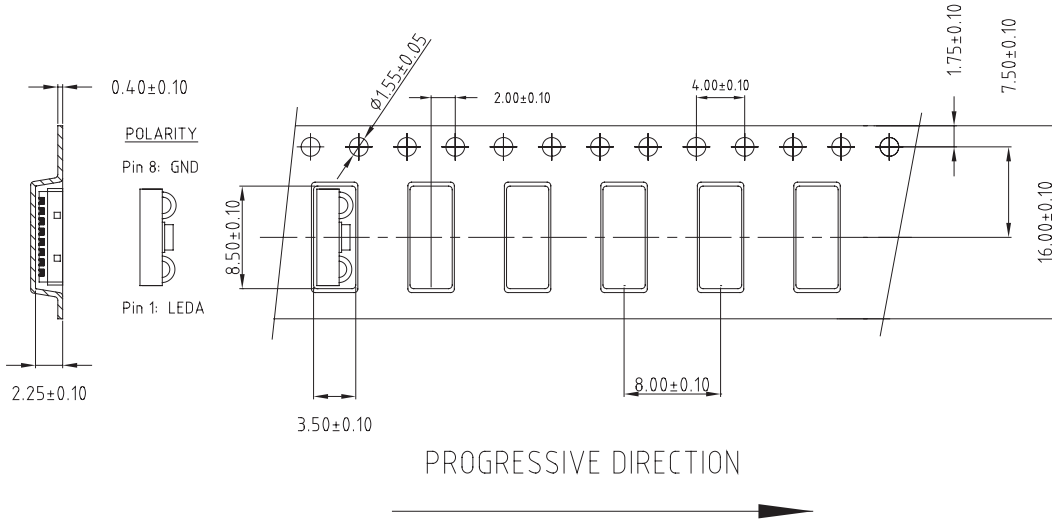
ASDL-3023-021 (Shieldless, Front)



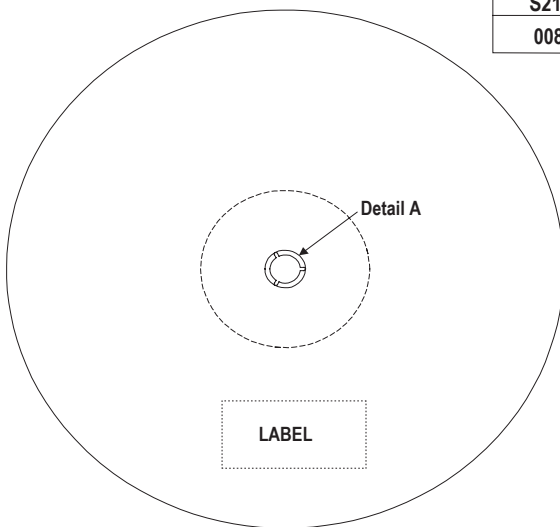
ASDL-3023-008 (Shieldless, Top)



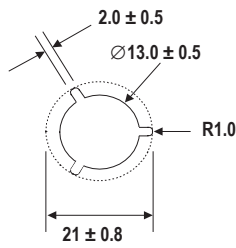
ASDL-3023-S21 (Shielded, Front)



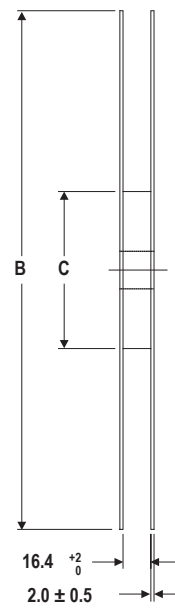
Option #	"B"	"C"	Quantity
021	330	80	2500
S21	330	80	2500
008	330	80	2500



Unit: mm



Detail A



ASDL-3023 Moisture Proof Packaging

All ASDL-3023 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 3.

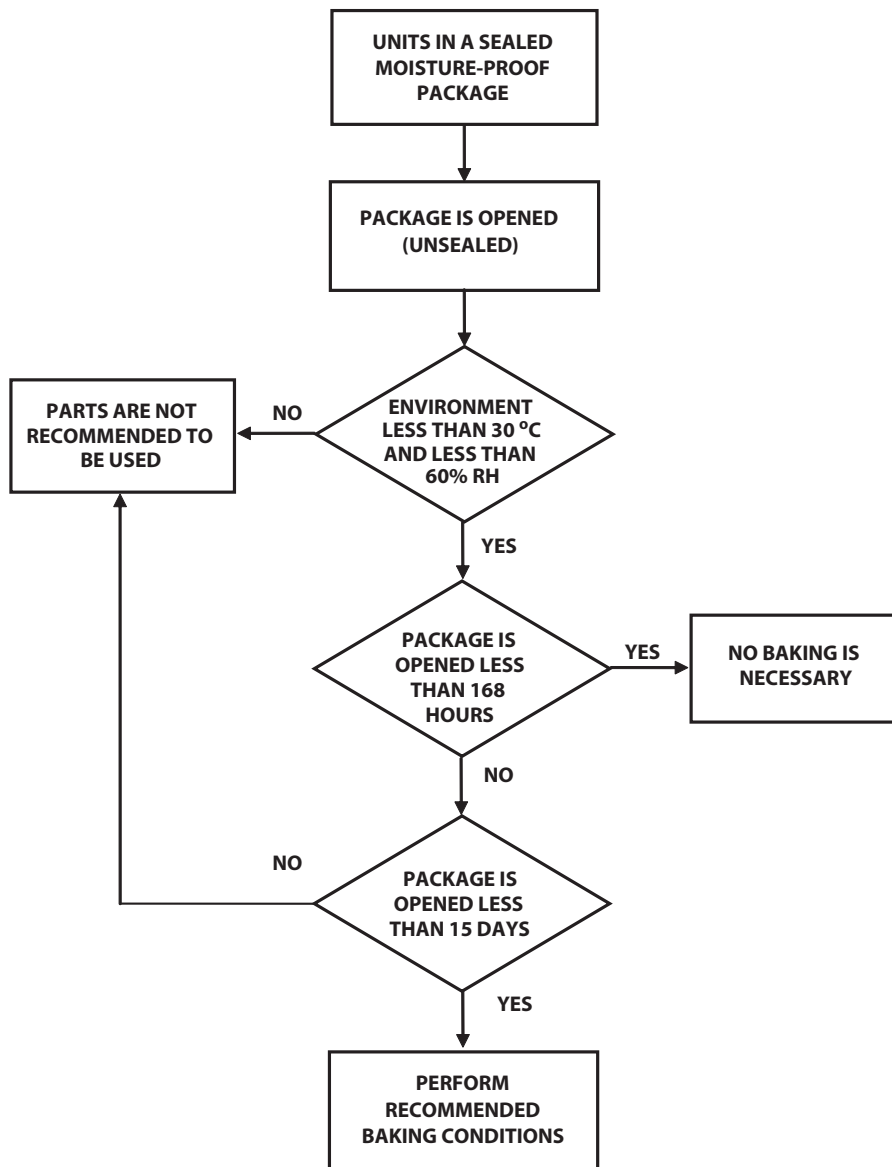


Figure 6. Baking Conditions Chart

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from unsealing to soldering

After removal from the bag, the parts should be soldered within 7 days if stored at the recommended storage conditions. When MBB (Moisture Barrier Bag) is opened and the parts are exposed to the recommended storage conditions more than 7 days but less than 15 days the parts must be baked before reflow to prevent damage to the parts.

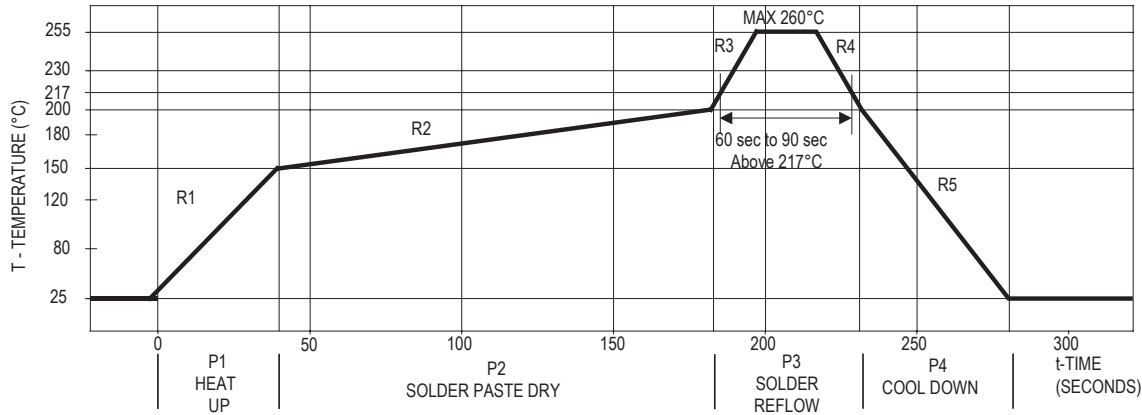
Note: To use the parts that exposed for more than 15 days is not recommended.

Baking Conditions

Package	Temp	Time
In reels	60 °C	≥ 48hours
In bulk	100 °C	≥ 4hours

Baking should only be done once.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum $\Delta T/\Delta \text{time}$ or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3	200°C to 260°C	3°C/s
	P3, R4	260°C to 200°C	-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point, 217°C		> 217°C	60s to 90s
Peak Temperature		260°C	-
Time within 5°C of actual Peak Temperature		-	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different $\Delta T/\Delta \text{time}$ temperature change rates or duration. The $\Delta T/\Delta \text{time}$ rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and ASDL-3023 pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and ASDL-3023 pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 90 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and ASDL-3023 pins to change dimensions evenly, putting minimal stresses on the ASDL-3023.

It is recommended to perform reflow soldering no more than twice.

Appendix A: ASDL-3023 SMT Assembly Application Note

Solder Pad, Mask and Metal Stencil

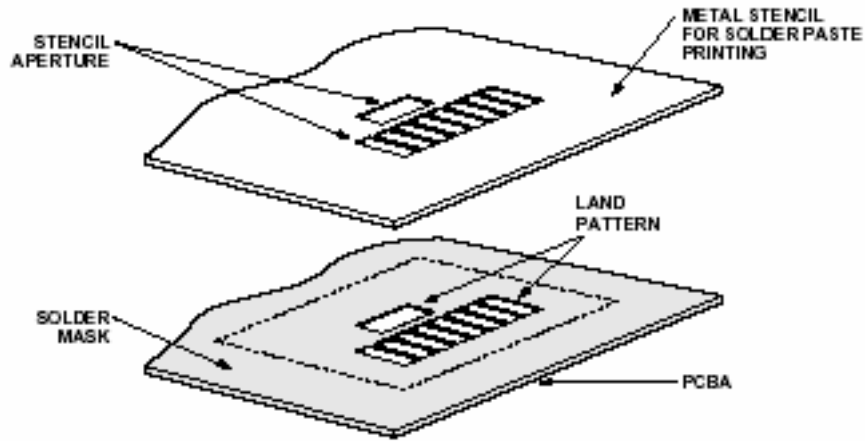
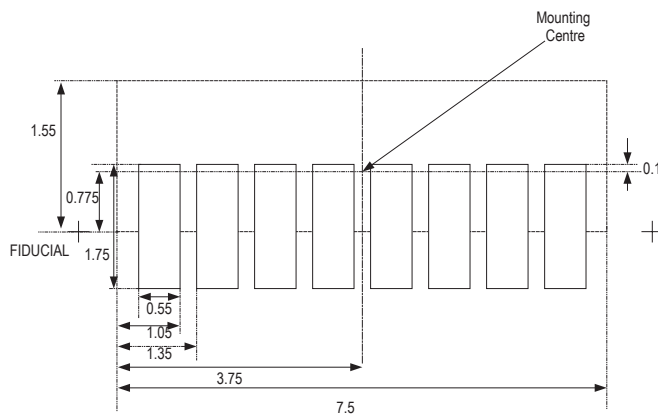


Figure A1. Stencil and PCBA

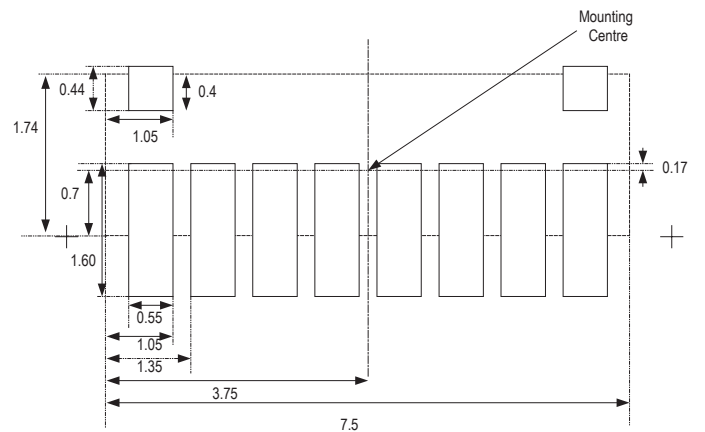
Recommended land pattern for ASDL-3023-021



UNIT: mm

Figure A2a. Recommended land pattern, ASDL-3023-021

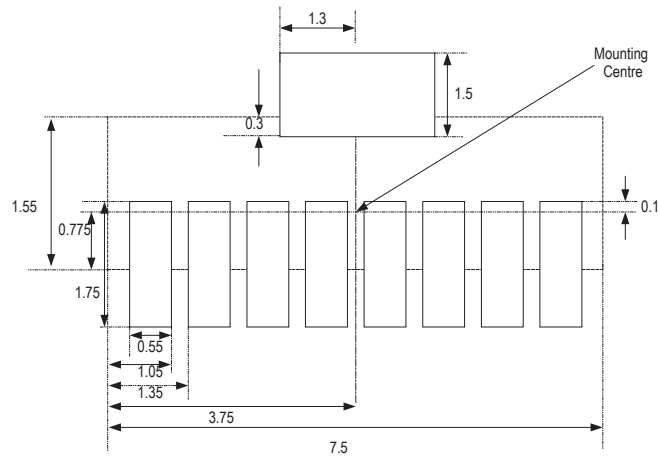
Recommended land pattern for ASDL-3023-008



UNIT: mm

Figure A2c. Recommended land pattern, ASDL-3023-008

Recommended land pattern for ASDL-3023-S21



UNIT: mm

Figure A2b. Recommended land pattern, ASDL-3023-S21

Recommended Metal solder Stencil Aperture

It is recommended that only a 0.11 mm (0.004 inch) or a 0.127 mm (0.005 inch) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the Table 1 below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used. Aperture opening for shield pad is 2.6 mm x 1.5 mm(for ASDL-3023-S1) as per land pattern. Compared to 0.127mm stencil thickness 0.11mm stencil thickness has longer length in land pattern. It is extended outwardly from transeiver to capture more solder paste volume.

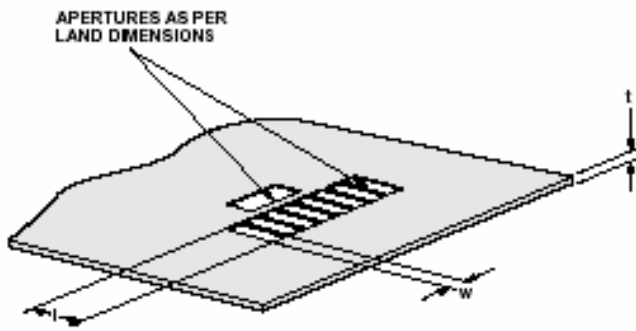


Figure A3. Solder stencil aperture

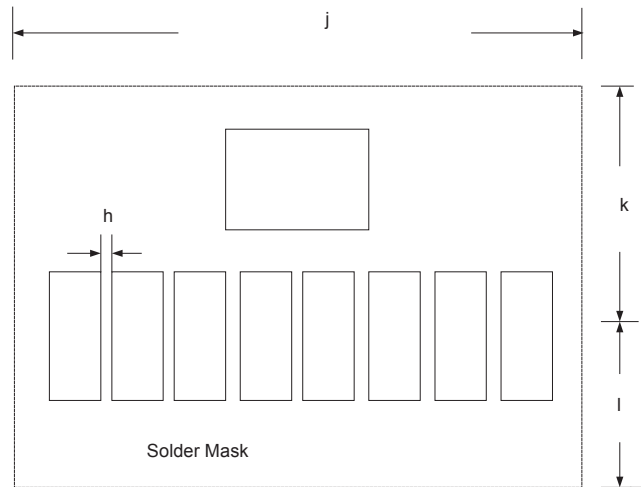
Table 1.

Stencil thickness, t(mm)	Aperture size(mm)	
	Length,l	Width,w
0.127mm	1.75+/-0.05	0.55+/-0.05
0.11mm	2.4+/-0.05	0.55+/-0.05

Adjacent Land Keepout and Solder Mask Areas

Adjacent land keepout is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area. The minimum solder resist strip width required to avoid solder bridging adjacent pads is 0.2mm. It is recommended that two fiducially crosses be placed at mid length of the pads for unit alignment.

Note: Wet/Liquid Photo-imaginable solder resist/mask is recommended

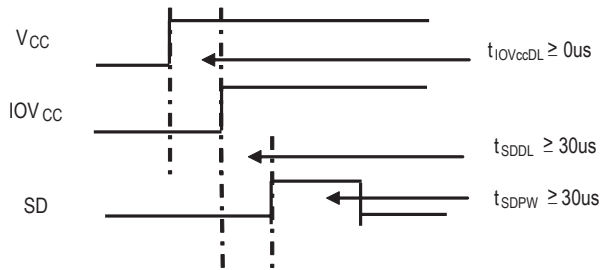


Dimension	mm
h	0.2
l	3.0
k	3.85
j	10.1

Power-Up Sequencing

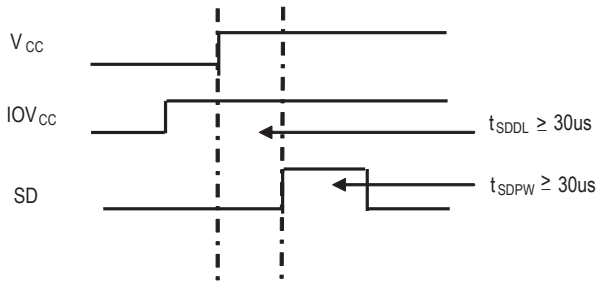
To have a proper operation for ASDL-3023, the following power-up sequencing must be followed.

(a) It's strongly recommended that Vcc must come prior to IOVcc.

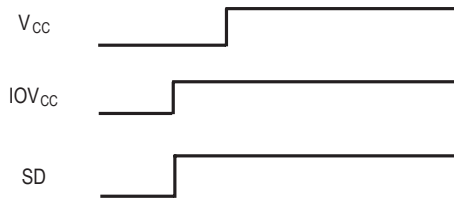


(b) It is not recommended to turn on IOVcc before Vcc while SD is low.

However, for application that IOVcc come prior to Vcc while SD is low, SD pin has to set high to assure proper functionality.



(c) Setting IOVcc high before Vcc while SD is high is forbidden.



Note:

$t_{IOVccDL}$: IOVcc delay time

t_{SDDL} : SD delay time

t_{SDPW} : Shutdown Input Pulse Width

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