

## DESCRIPTION

The ULN2803/2804 series are high-voltage, high-current darlington arrays comprised of eight NPN darlington

pairs. All units feature integral clamp diodes for switching inductive loads.

## FEATURES

- Output current.....500mA
- High Sustaining Voltage.....50V Min.
- Output Clamp Diode
- Inputs Compatible With Various Types of Logic

Type	Input Resistor	Designation
ULN2803	2.7K $\Omega$	TTL, 5V C - MOS
ULN2804	10.5K $\Omega$	6 ~ 15V P -MOS, C -MOS

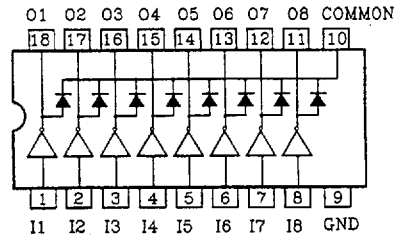
## MAXIMUM RATING(Ta=25°C unless otherwise)

Characteristic	Symbol	Rating	Unit
Output Sustaining Voltage	$V_{CE(SUS)}$	50	V
Output Current	$I_{OUT}$	500	mA
Input Voltage	$V_{IN}$	-0.5~+30	V
Input Current	$I_{IN}$	25	mA
Clamp Diode	Reverse Voltage	$V_R$	50 V
	Forward Current	$I_F$	500 mA
GND Terminal Current	$I_{GND}$	3.2	A
Power Dissipation	$P_D$	1.47	W
Operating Temperature	$T_{opr}$	-40~85	°C
Storage Temperature	$T_{stg}$	-55~150	°C

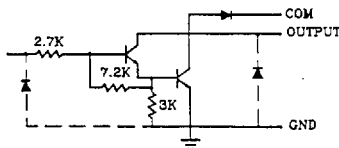
18 DIP



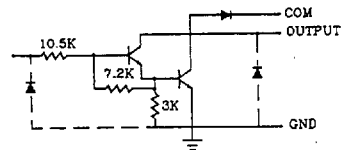
## PIN CONNECTION (TOP VIEW)



ULN2803



ULN2804



### RECOMMENDED OPERATING CONDITIONS(T<sub>a</sub>=-40-85°C)

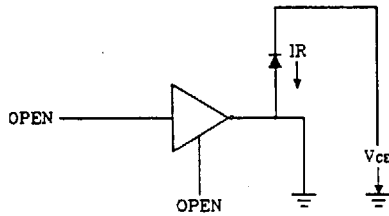
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	V <sub>CE(SUS)</sub>		0	-	50	V
Output Current	I <sub>OUT</sub>	T <sub>PW</sub> =25mS,DF=8%, 8 Circuits	0	-	400	mA
		T <sub>PW</sub> =25mS,DF=25% 8 Circuits	0	-	200	
Input Voltage	V <sub>IN</sub>		0	-	30	V
Clamp Diode Reverse Voltage	V <sub>R</sub>		-	-	50	V
Clamp Diode Forward Current	I <sub>F</sub>		-	-	400	mA
Power Dissipation	P <sub>D</sub>		-	-	0.52	W

### ELECTRICAL CHARACTERISTICS(T<sub>a</sub>=25°C unless otherwise noted)

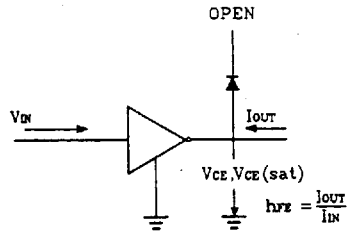
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT		
Output leak Current	I <sub>CEX</sub>	1	V <sub>CE</sub> =50V, T <sub>a</sub> =25°C	-	-	50	μ A		
			V <sub>CE</sub> =50V, T <sub>a</sub> =85°C	-	-	100			
			V <sub>CE</sub> =50V, V <sub>IN</sub> =1V	-	-	500			
Collector-Emitter Saturation Voltage	V <sub>CE(sat)</sub>	2	I <sub>OUT</sub> =350mA, I <sub>IN</sub> =500μ A	-	1.3	1.6	V		
			I <sub>OUT</sub> =200mA, I <sub>IN</sub> =350μ A	-	1.1	1.3			
			I <sub>OUT</sub> =100mA, I <sub>IN</sub> =250μ A	-	0.9	1.1			
Input Current	I <sub>IN(on)</sub>	3	V <sub>IN</sub> =3.85V	-	0.93	1.35	mA		
			V <sub>IN</sub> =5V	-	0.35	0.5			
			V <sub>IN</sub> =12V	-	1.0	1.45			
Input Voltage	V <sub>IN(ON)</sub>	4	I <sub>OUT</sub> =500μ A, T <sub>a</sub> =85°C	50	65	-	μ A		
			5	V <sub>CE</sub> =2V, I <sub>OUT</sub> =200mA	-	-		2.4	V
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =250mA	-	-		2.7	
V <sub>CE</sub> =2V, I <sub>OUT</sub> =300mA	-	-		3.0					
ULN2803	V <sub>IN(ON)</sub>	5	V <sub>CE</sub> =2V, I <sub>OUT</sub> =125mA	-	-	5.0			
			V <sub>CE</sub> =2V, I <sub>OUT</sub> =200mA	-	-	6.0			
			V <sub>CE</sub> =2V, I <sub>OUT</sub> =275mA	-	-	7.0			
ULN2804	V <sub>IN(ON)</sub>	5	V <sub>CE</sub> =2V, I <sub>OUT</sub> =350mA	-	-	8.0			
DC Current Transistor Ratio	h <sub>FE</sub>	2	V <sub>CE</sub> =2V, I <sub>OUT</sub> =350mA	1000	-	-			
Clamp Diode Reverse Current	I <sub>E</sub>	6	V <sub>R</sub> =50V, T <sub>a</sub> =25°C	-	-	50	μ A		
			V <sub>R</sub> =50V, T <sub>a</sub> =85°C	-	-	100			
Clamp Diode Forward Voltage	V <sub>F</sub>	7	I <sub>F</sub> =350mA	-	-	2.0	V		
Input Capacitance	C <sub>IN</sub>			-	15	-	pF		
Turn-On Delay	t <sub>ON</sub>	8	V <sub>OUT</sub> =50V, R <sub>L</sub> =163Ω C <sub>L</sub> =15 pF	-	0.1	-	μ S		
Turn-Off Delay	t <sub>OFF</sub>			-	0.2	-			

## TEST CIRCUIT

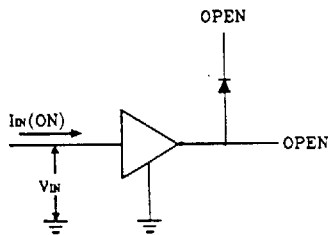
1.  $I_{CEX}$



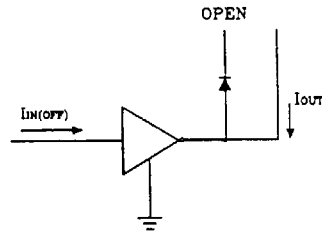
2.  $V_{CE(sat)}$ ,  $h_{FE}$



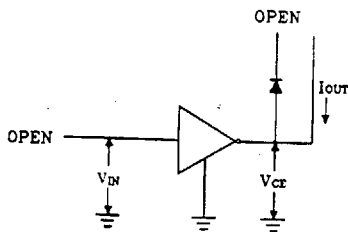
3.  $I_{IN(ON)}$



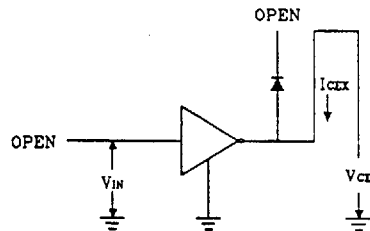
4.  $I_{IN(OFF)}$



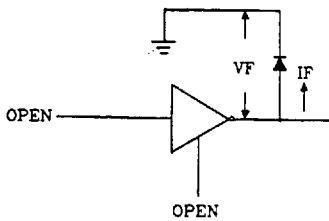
5.  $V_{IN(ON)}$



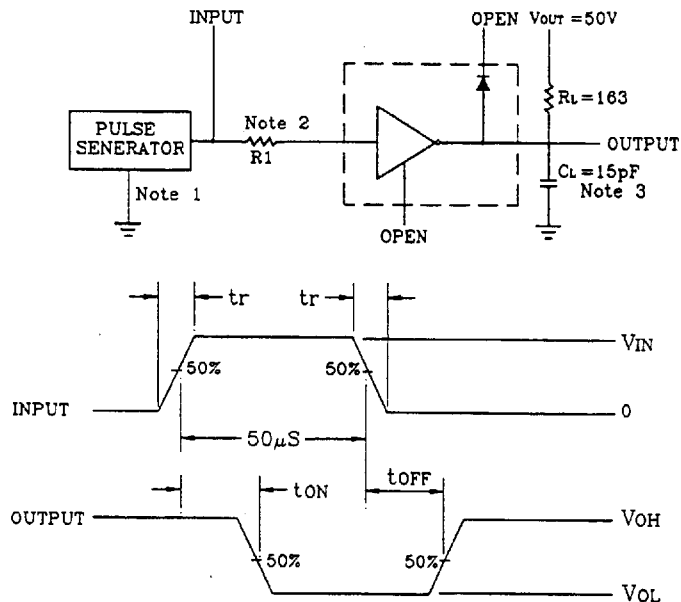
6.  $I_R$



7.  $V_F$



## 8. $t_{ON}$ , $t_{OFF}$



Notes: 1. Pulse Width  $50\mu s$ , Duty Cycle 10%

Output Impedance  $50\Omega$

$t_r \leq 5ns$ ,  $t_f \leq 10ns$

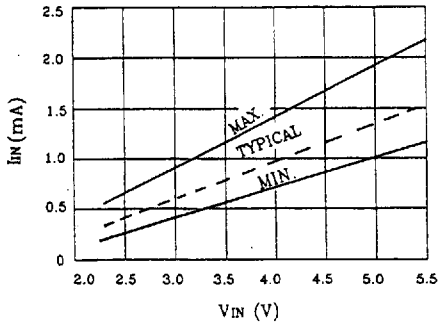
2. See below

Input Conditions

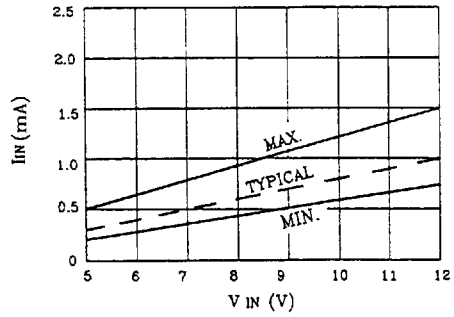
TYPE NUMBER	$R_I$	$V_{IH}$
ULN2803	0	3V
ULN2804	0	8V

3.  $C_L$  includes prob and jig capacitance.

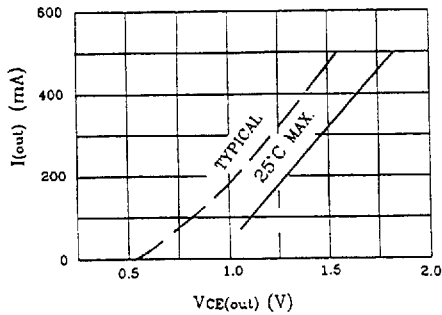
**ULN2803  $I_{IN} - V_{IN}$**



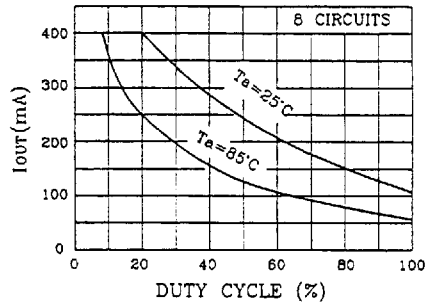
**ULN2804  $I_{IN} - V_{IN}$**



**$F_D - T_a$**



**$I_{OUT} - V_{CE(out)}$**



**$I_{OUT} - \text{DUTY CYCLE}$**

