TOSHIBA Photocoupler GaAlAs Ired & Photo IC

TLP559

Digital Logic Ground Isolation Line Receiver Microprocessor System Interfaces Switching Power Supply Feedback Control Transistor Inverter

The TOSHIBA TLP559 consists of a GaAlAs high–output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP package.

TLP559 has no internal base connection, and a faraday shield integrated on the photodetector chip provides an effective common mode noise transient immunity.

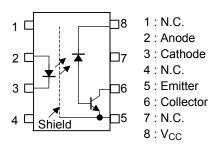
So this is suitable for application in noisy environmental condition.

- Isolation voltage: 2500Vrms (min.)
- Switching speed: $t_{pHL} = 0.3\mu s$ (typ.) $t_{pLH} = 0.5\mu s$ (typ.) (RL = 1.9k Ω)
- TTL compatible
- UL recognized: UL1577, file No.E67349

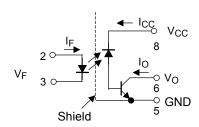
Unit in mm 2.5MIN. 2.54 ± 0.25 11-10C4 **TOSHIBA** 11-10C4

Weight: 0.54g

Pin Configuration (top view)



Schematic



Absolute Maximum Ratings (Ta = 25°C)

	Characteristic	Symbol	Rating	Unit	
TED	Forward current	(Note 1)	l _F	25	mA
	Pulse forward current	(Note 2)	I _{FP}	50	mA
	Peak transient forward current	(Note 3)	I _{FPT}	1	Α
	Reverse voltage		V _R	5	V
	Diode power dissipation	(Note 4)	PD	45	mW
	Output current		IO	8	mA
ō	Peak output current		l _{OP}	16	mA
Detector	Output voltage		V _O	-0.5~15	V
ă	Supply voltage		V _{CC}	-0.5~15	V
	Output power dissipation	(Note 5)	PO	100	mW
Оре	erating temperature range		T _{opr}	-55~100	°C
Sto	rage temperature range	T _{stg}	-55~125	°C	
Lea	Lead solder temperature (10s) (Note 6			260	°C
Isol	Isolation voltage (AC, 1 min., R.H. ≤ 60%) (Note 7)			2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- (Note 1) Derate 0.8mA above 70°C.
- (Note 2) 50% duty cycle,1ms pulse width. Derate 1.6mA / °C above 70°C.
- (Note 3) Pulse width $\leq 1 \mu s$, 300pps.
- (Note 4) Derate 0.9mW / °C above 70°C.
- (Note 5) Derate 2mW / °C above 70°C.
- (Note 6) Soldering portion of lead: up to 2mm from body of the devise.
- (Note 7) Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min.	Тур.	Max.	Unit
LED	Forward voltage	V _F	I _F = 16mA	_	1.65	1.85	V
	Forward voltage temperature coefficient	ΔV _F / ΔTa	ΔTa I _F = 16mA		-2	-	mV / °C
	Reverse current	I _R	V _R = 5V	_	-	10	μΑ
	Capacitance between terminal	C _T	V _F = 0, f = 1MHz	1	45	1	pF
Detector	High level output current	I _{OH} (1)	$I_F = 0mA, V_{CC} = V_O = 5.5V$	_	3	500	nA
		I _{OH} (2)	$I_F = 0mA, V_{CC} = V_O = 15V$	_	_	5	
		Іон	I _F = 0mA, V _{CC} = 15V V _O = 15V, Ta = 70°C	-	_	50	μΑ
	High level supply voltage	Icch	I _F = 0mA, V _{CC} = 15V	_	0.01	1	μA
Coupled	Current transfer ratio	t transfer ratio I_O/I_F $I_F = 16\text{mA}, V_{CC} = 4.5V$ $V_O = 0.4V$		20	40	_	%
	Low level output voltage	V _{OL}	I _F = 16mA, V _{CC} = 4.5V I _O = 2.4mA	_	_	0.4	V
	Resistance (input-output)	R _S	R.H. ≤ 60%, V _S = 500V _{DC} (Note 7)	5×10 ¹⁰	10 ¹⁴	_	Ω
	Capacotance (input-output)	CS	$V_S = 0$, $f = 1MHz$ (Note 7)	_	0.8	_	pF

Switching Characteristics (Ta = 25°C, V_{CC} = 5V)

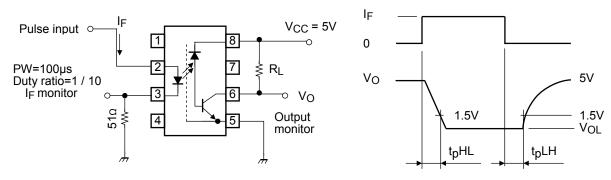
Characteristic		Symbol	Test Cir– cuit	Test Condition	Min.	Тур.	Max.	Unit
Propagation delay time	(H→ L)	t _{pHL}	1	I_F = 16mA, R_L = 1.9kΩ	-	0.2	0.8	μs
Propagation delay time	(L→ H)	t _{pLH}	'		_	0.3	0.8	μs
Common mode transient immunity at logic high output	(Note 8)	CM _H	- 2	I_F = 0mA, V_{CM} = 400 V_{p-p} R _L = 4.1k Ω	2000	10000	l	V / µs
Common mode transient immunity at logic high output	(Note 8)	CML		$I_F = 16 \text{mA}, V_{CM} = 400 V_{p-p}$ R _L = 4.1k Ω	-2000	-10000		V / μs

(Note 8) CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$).

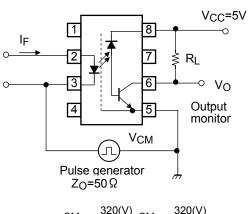
 CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O < 2.0V$).

(Note 9) Maximum electrostatic discharge voltage for any pins: 100V (C = 200pF, R = 0)

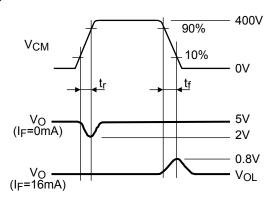
Test Circuit 1: Switching Time Test Circuit

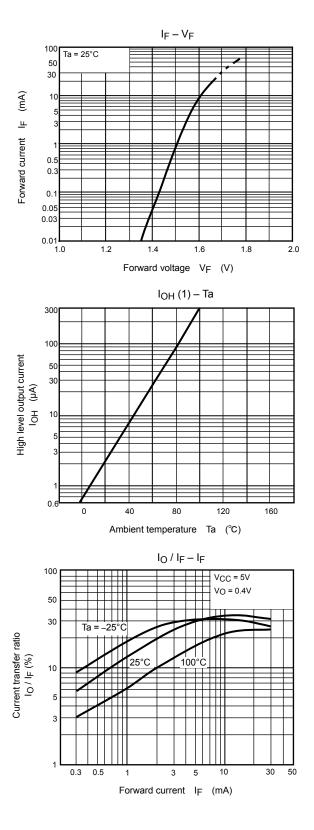


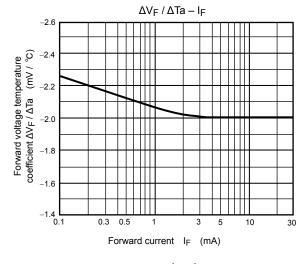
Test Circuit 2: Common Mode Noise Immunity Test Circuit

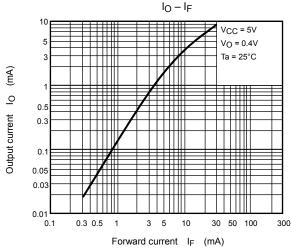


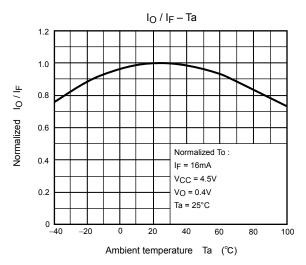
$$\text{CM}_{H} = \frac{320(\text{V})}{t_{\Gamma}(\mu s)}, \text{CM}_{L} = \frac{320(\text{V})}{t_{f}(\mu s)}$$



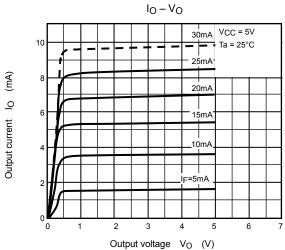


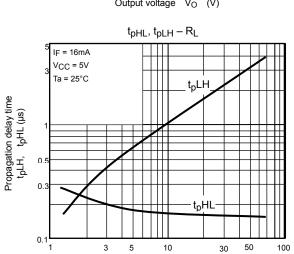




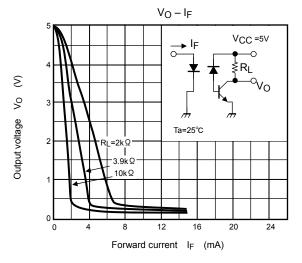


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Load resistance R_L $(k\Omega)$



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