

## Portable Equipment Application. Notebook Application.

### Features

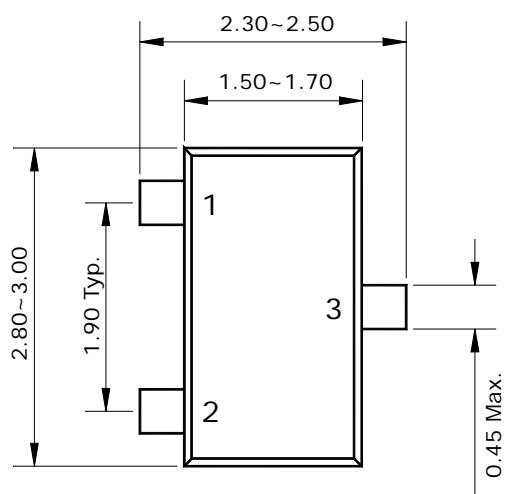
- Low  $V_{GS(th)}$  :  $V_{GS(th)} = 0.6 \sim 1.2V$
- Small footprint due to small package
- Low  $R_{DS(on)}$  :  $R_{DS(on)} = 33m\Omega$  (Typ.)

### Ordering Information

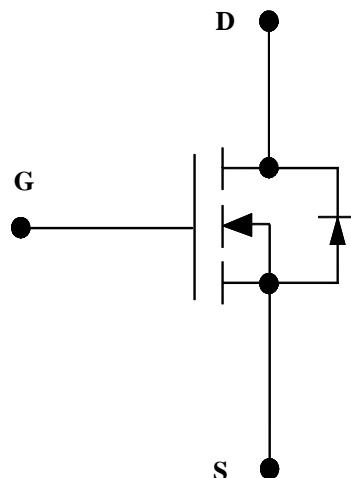
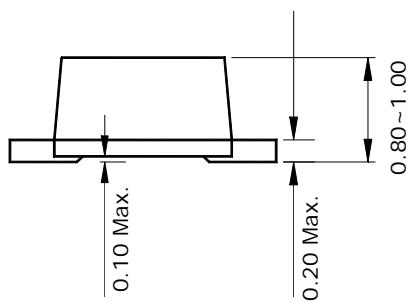
Type NO.	Marking	Package Code
STK001SF	K01	SOT-23F

### Outline Dimensions

unit : mm



Block Diagram



#### PIN Connections

1. Gate
2. Source
3. Drain

**Absolute maximum ratings**

(Ta=25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V <sub>DSS</sub>	20	V
Gate-source voltage	V <sub>GSS</sub>	±12	V
Drain current (DC) **	I <sub>D</sub>	3.2	A
Drain current (Pulsed) *	I <sub>DP</sub>	12.8	A
Total Power dissipation **	P <sub>D</sub>	0.35	W
Avalanche current (Single) ②	I <sub>AS</sub>	3.2	A
Single pulsed avalanche energy ②	E <sub>AS</sub>	30	mJ
Avalanche current (Repetitive) ①	I <sub>AR</sub>	3.2	A
Repetitive avalanche energy ①	E <sub>AR</sub>	2.5	mJ
Junction temperature	T <sub>J</sub>	150	°C
Storage temperature range	T <sub>sta</sub>	-55~150	

\* Limited by maximum junction temperature

\*\* Device mounted on a glass-epoxy board

Characteristic	Symbol	Typ.	Max	Unit
Thermal resistance	R <sub>th(J-a)</sub> **	-	357	°C/W

**N-CH Electrical Characteristics**

(Ta=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0	20	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	0.6	-	1.2	V
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V	-	-	±10	μA
Drain-source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =1.6A	-	33	50	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =1.6A	-	46	70	mΩ
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =3.2A	-	10.5	-	S
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =10V, f=1MHz	-	395	-	pF
Output capacitance	C <sub>oss</sub>		-	97	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	44	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, I <sub>D</sub> =3.2A R <sub>G</sub> =10Ω	-	3.2	-	ns
Rise time	t <sub>r</sub>		-	2.8	-	
Turn-off delay time	t <sub>d(off)</sub>		-	20	-	
Fall time	t <sub>f</sub>		-	2.8	-	
Total gate charge	Q <sub>g</sub>	V <sub>DD</sub> =10V, V <sub>GS</sub> =4.5V I <sub>D</sub> =3.2A	-	6.8	10	nC
Gate-source charge	Q <sub>gs</sub>		-	0.8	1.2	
Gate-drain charge	Q <sub>gd</sub>		-	0.9	1.1	

**Source-Drain Diode Ratings and Characteristics**

(Ta=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Source current	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	0.5	A
Source current(Plusd) ①	I <sub>SM</sub>		-	-	2.0	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =0.5A	-	0.7	1.2	V
Reverse recovery time	t <sub>rr</sub>	I <sub>s</sub> =3.2A, V <sub>DD</sub> =10V dI <sub>S</sub> /dt=70A/us	-	24	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	120	-	uC

Note :

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

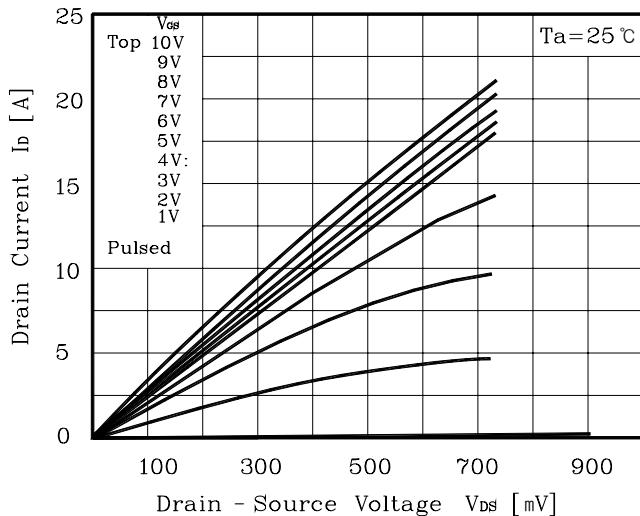
② L=3.0mH, I<sub>AS</sub>=3.8A, V<sub>DD</sub>=10V, R<sub>G</sub>=25Ω

③ Pulse Test : Pulse Width &lt; 300us, Duty cycle≤ 2%

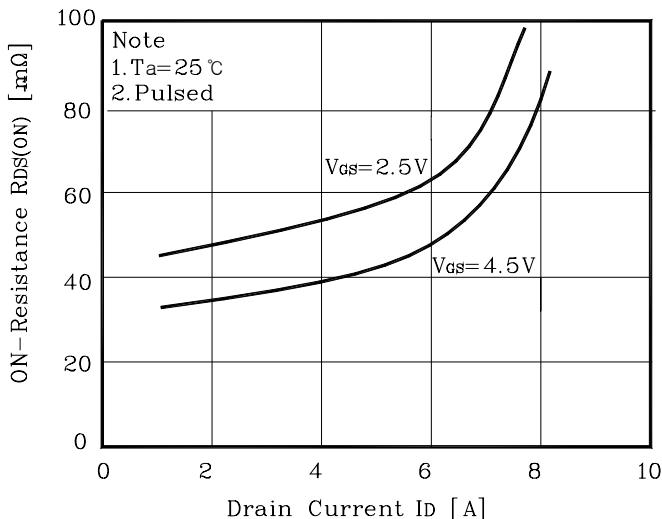
④ Essentially independent of operating temperature

## N-CH Electrical Characteristic Curves

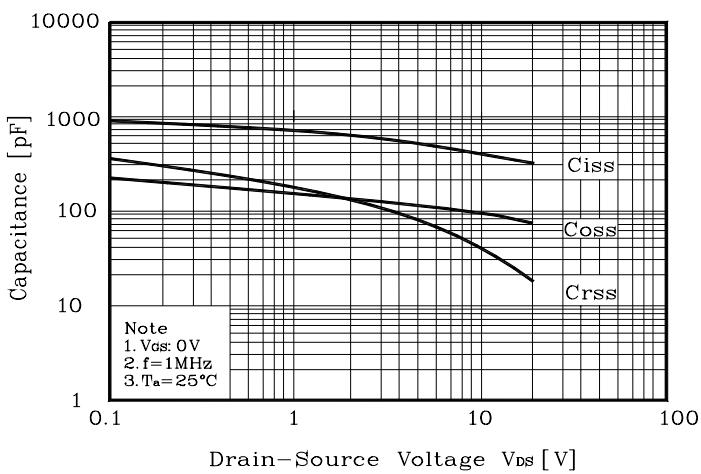
**Fig. 1  $I_D$  -  $V_{DS}$**



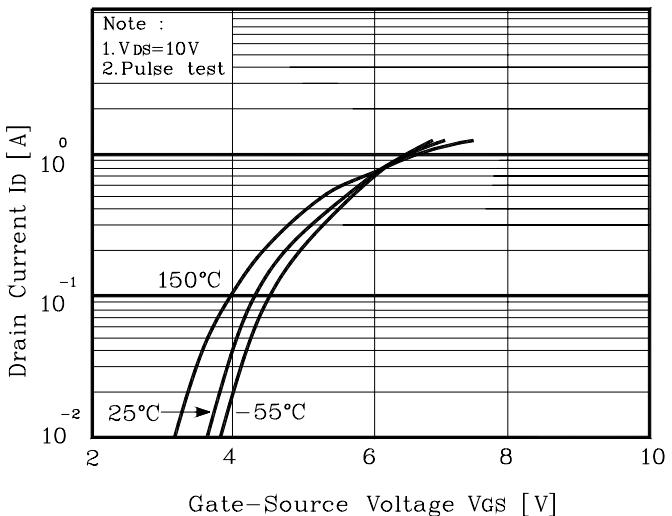
**Fig. 3  $R_{DS(on)}$  -  $I_D$**



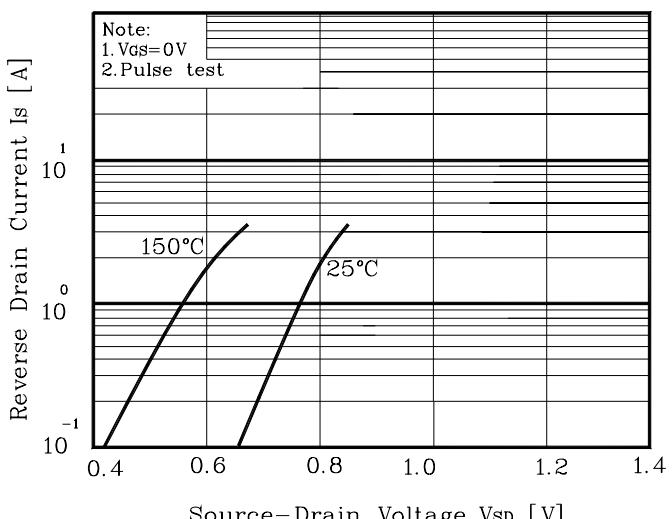
**Fig. 5 Capacitance -  $V_{DS}$**



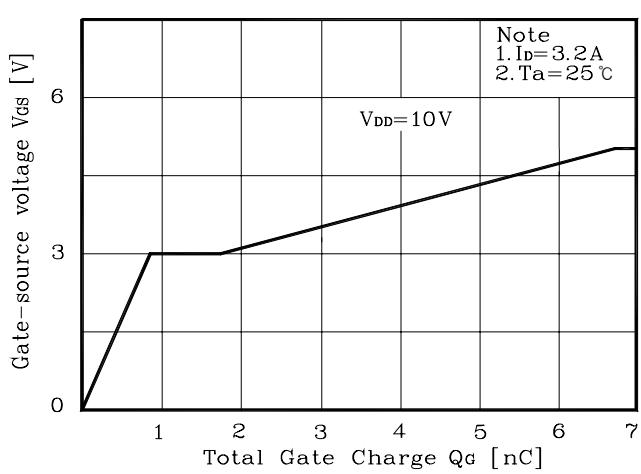
**Fig. 2  $I_D$  -  $V_{GS}$**



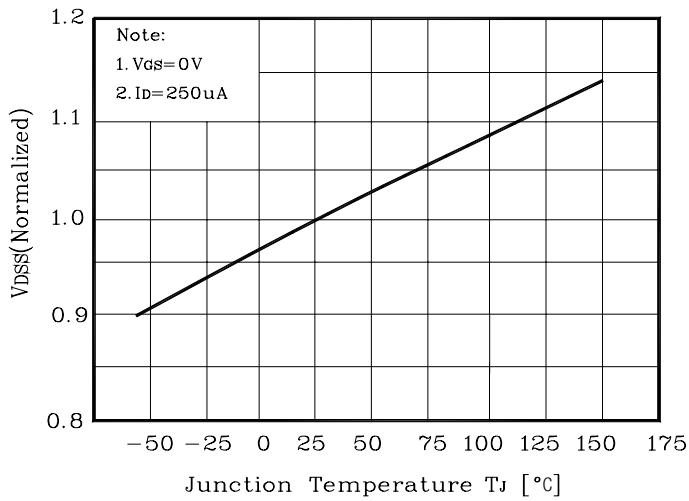
**Fig. 4  $I_S$  -  $V_{SD}$**



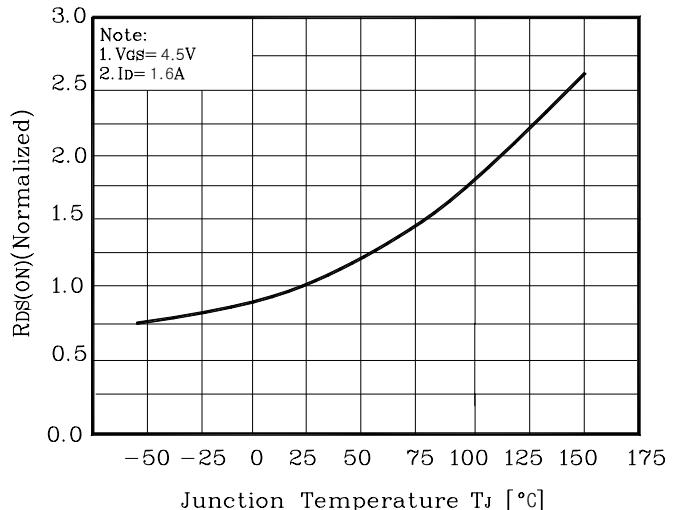
**Fig. 6  $V_{GS}$  -  $Q_G$**



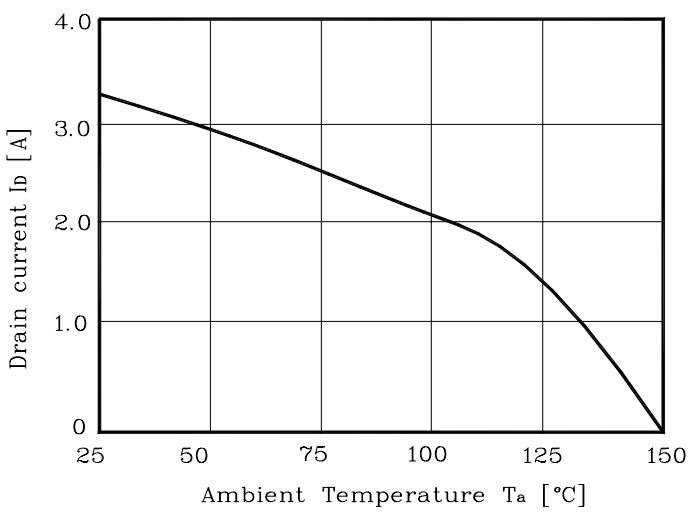
**Fig. 7  $V_{DSS}$  -  $T_J$**



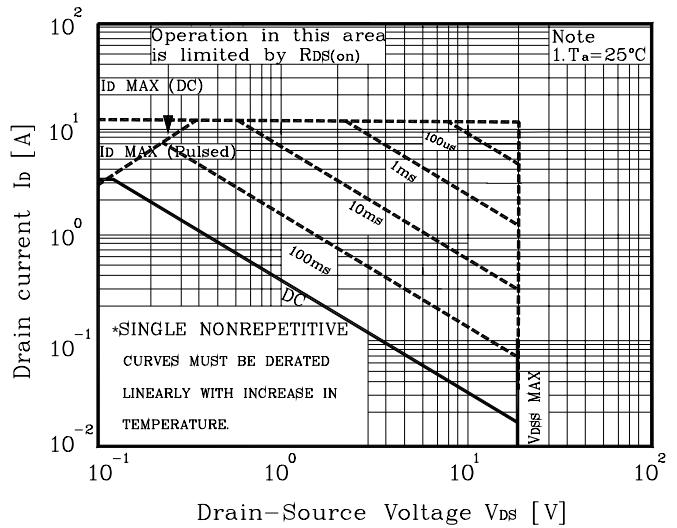
**Fig. 8  $R_{DS(on)}$  -  $T_J$**



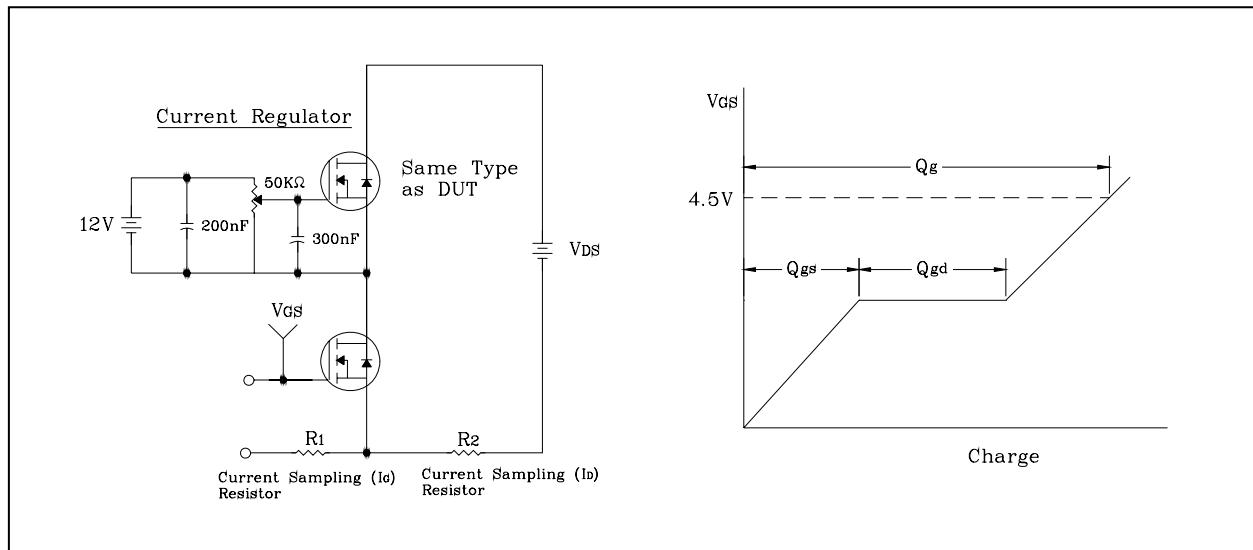
**Fig. 9  $I_D$  -  $T_a$**



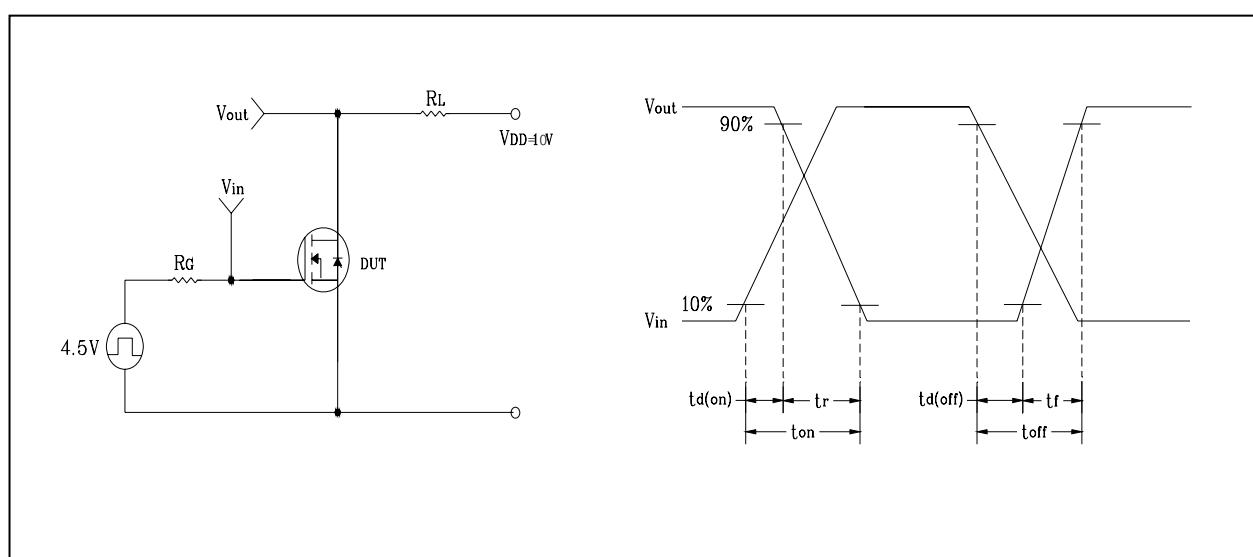
**Fig. 10 Safe Operating Area**



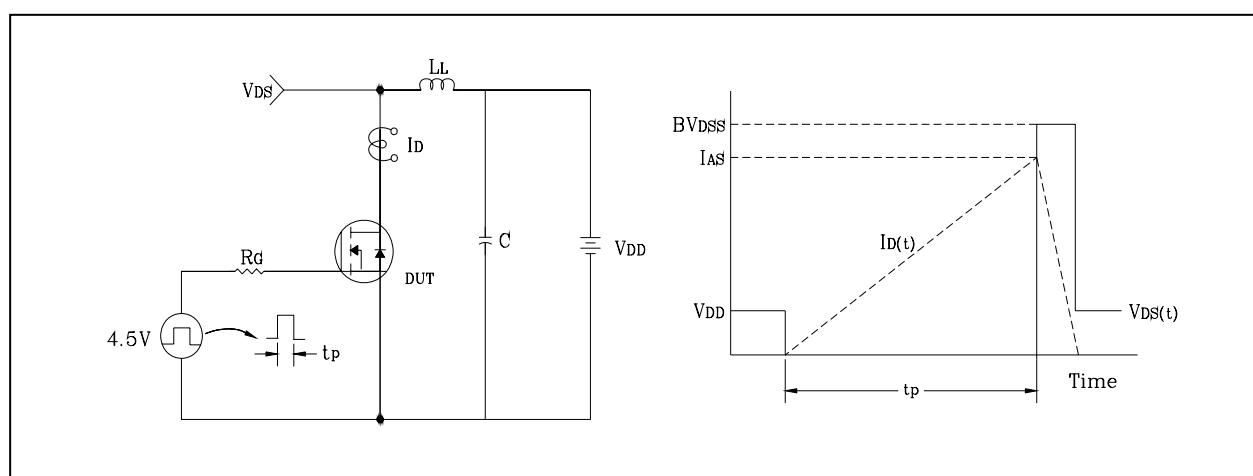
**Fig. 11 Gate Charge Test Circuit & Waveform**



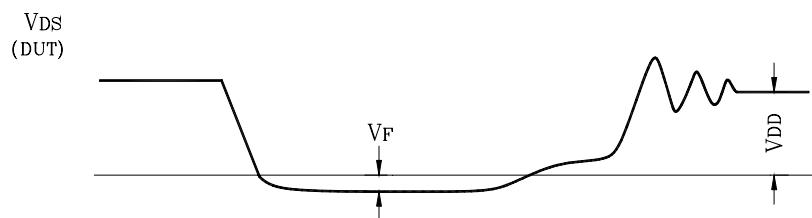
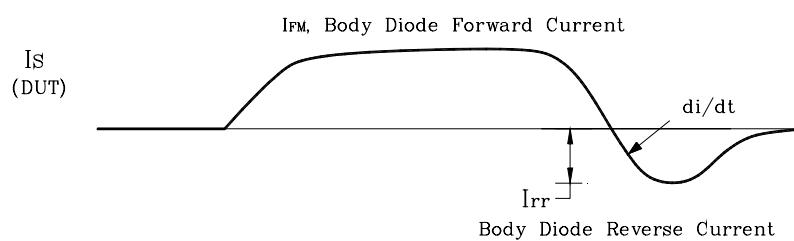
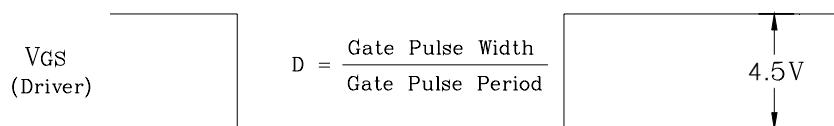
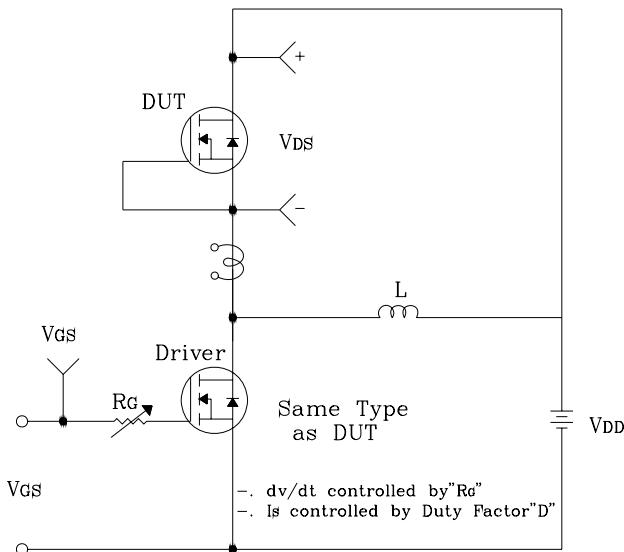
**Fig. 12 Resistive Switching Test Circuit & Waveform**



**Fig. 13 E<sub>AS</sub> Test Circuit & Waveform**



**Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform**



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