PCI 9056

32-bit, 66MHz PCI Bus Mastering I/O Accelerator for Motorola PowerQUICC™ and Generic 32-bit, 66MHz Local Bus Designs

Connectivity

- 32-bit, 66MHz PCI r2.2 compliant
- Motorola PowerQUICC and generic 32-bit, 66MHz local bus modes
- 3.3V I/O, 5V tolerant bus interfaces
- PICMG 2.1 r2.0 Hot Swap Silicon
- 256-ball, 17 x 17 mm, 1.00 mm fine pitch PBGA (FPBGA)

Performance

- Zero wait state burst operation
  - PCI bus bursts to 264 MB/sec
  - Local bus bursts to 264 MB/sec
- 2 DMA Channels
  - Block & Scatter/Gather transfers
  - DMA descriptor ring management
  - Demand Mode & EOT H/W controls
- Direct Master data transfers
  - Generate any PCI transaction
  - Read ahead and programmable read prefetch counter
- Direct Slave data transfers
  - Access 8-, 16-, and 32-bit local bus devices
  - Deferred reads, deferred writes, read ahead, posted writes, programmable read prefetch counter

Control

- I_2O r1.5 messaging unit
- Eight mailbox and two doorbell registers
- PCI arbiter supports 7 external masters
- Host mode reset/interrupt signal configuration
- PCI $D3_{COLD}$ Power Management Event (PME) generation support
- Serial EEPROM interface
- JTAG boundary scan

PLX TECHNOLOGY
THE I/O INTERCONNECT SOLUTION

Highest Performance 32-bit PCI Bus Mastering I/O Accelerator for Your Embedded Applications

The PCI 9056 offers flexible connectivity and high performance I/O acceleration features to enable leading edge PCI, CompactPCI, and embedded host designs.

Motorola® MPC 850/860 PowerQUICC Designs

The PCI 9056 is the perfect match for the industry leading 32-bit communications processor, the Motorola MPC 850/860 PowerQUICC. The PCI 9056 provides a direct connection to PowerQUICC devices, enabling high-speed 32-bit, 66MHz PCI performance utilizing PLX's Data Pipe Architecture™ technology.

Generic 32-bit, 66MHz Local Bus Designs

The PCI 9056 provides direct connection to two generic industry standard interconnect buses. Designers use these 32-bit, 66MHz buses for a myriad of high-speed devices ranging from processors, to DSPs, to memories, to custom ASICs and FPGAs. The PCI 9056 Data Pipe Architecture technology enables high-speed, 32-bit, 66MHz PCI I/O with those devices.

Move Your 32-bit Embedded Designs Up to 66MHz Operation

As PCI evolves to meet the ever increasing I/O demands of leading edge communications systems, PLX continues to provide high performance PCI I/O acceleration solutions. Based on the architecture of the industry-leading PCI 9054, the PCI 9056 offers a variety of enhancements for the needs of today's telecom, networking, and I/O adapter designs:

- 32-bit, 66MHz PCI operation
- 32-bit, 66MHz local bus operation
- Dynamic DMA descriptor ring management with Valid bit semaphore control
- PICMG 2.1 r2.0 Hot Swap Silicon, including Bias Voltage, Early Power, and Initialy Not Responding Support
- PCI Power Management r1.1 $D3_{COLD}$ Power Management Event (PME) generation
- PCI arbiter supporting 7 external masters
- Reset and interrupt pins configurable for embedded host applications
- JTAG boundary scan

The PCI 9056 is register compatible with the PCI 9054, enabling easy software migration.

PCI 9056 Features

The PCI 9056 32-bit, 66MHz PCI I/O accelerator is the most advanced, 32-bit general-purpose bus mastering device available for Motorola MPC 850/860 PowerQUICC and generic 32-bit, 66MHz local bus based designs. The PCI 9056 incorporates PLX's industry leading Data Pipe Architecture technology, featuring DMA engines, programmable Direct Master and Direct Slave data transfer modes, and PCI messaging functions.

Interfaces

PCI

- 32-bit, 66MHz r2.2 operation
  - Zero wait state bursts to 264 MB/s
  - Dual Address Cycle (DAC) support as a PCI bus master
  - Vital Product Data (VPD)
  - 3.3V I/O, 5V tolerant
- PICMG 2.1 r2.0 Hot Swap Silicon
  - Programming Interface 0 (PI=0)
  - Bias Voltage Support
  - Early Power Support
  - Intially Not Responding Support
- PCI Hot Plug r1.0
- PCI Power Management r1.1
  - Supports D0, D1, D2, $D3_{HOT}$, and $D3_{COLD}$ power states
  - $D3_{COLD}$ Power Management Event (PME) generation to meet PC 2001 Windows 98/2000 communication adapter logo certification requirements

Local Bus

- Three local bus options on the device
  - M Mode: Motorola MPC 850/860 PowerQUICC and PowerPC 80x/82x
  - C Mode: De-multiplexed address and data buses for Intel i960(r), DSPs, custom ASICs and FPGAs, and others
  - J Mode: Multiplexed address and data buses for Intel i960, IBM PowerPC 401, IDT RC32364, DSPs, PLX IOP 480, and others
- 32-bit, 66MHz operation
  - Zero wait state bursts to 264 MB/s
  - 3.3V I/O, 5V tolerant
  - Asynchronous clock inputs to PCI and local bus

Serial EEPROM

- Stores configuration register power on, reset values
- An alternative to expansion ROM for storing Vital Product Data (VPD)
- Supports 2 Kbit/4 Kbit microwire devices with sequential read

Data Pipe Architecture

DMA

Service DMA descriptors, mastering on both bus interfaces during data transfer

- Two independent channels provide flexible prioritization scheme
- Each channel has its own bi-directional 64 Lword (256 byte) deep FIFO
- Block Mode services a single DMA descriptor in PCI 9056 registers
- Scatter/Gather Mode services DMA descriptor linked lists in memory
  - Burst descriptors from PCI or local bus memory
  - Descriptor lists either linear (static) or circular (dynamic) with Valid bit semaphore control
- Direct Hardware DMA controls
  - Demand Mode to pause/resume
  - End of Transfer (EOT) to abort
- Programmable local bus burst length, including infinite
  - Enhanced M Mode supports bursts beyond PowerQUICC 16 byte limit

Direct Master

Service local bus masters by mastering on the PCI bus

- Two local bus address spaces map to PCI bus: one to memory; one to I/O
- Generate all PCI memory and I/O transaction types, including Memory Write and Invalidate (MWI)
- Independent 32 Lword (128 byte) read and 64 Lword (256 byte) write FIFOs
- Read ahead and programmable read prefetch counter
- PowerQUICC deferred reads and IDMA (M mode only)

Direct Slave

Service PCI bus masters by mastering on the local bus

- Two general-purpose and one expansion ROM PCI address spaces map to local bus memory
  - Each address space may specify 8-, 16-, or 32-bit local bus data transfers
- Independent 32 Lword (128 byte) read and 64 Lword (256 byte) write FIFOs
- Deferred reads, deferred writes, posted writes, read ahead, and programmable read prefetch counter
- Programmable READY# time out and recovery

Advanced Performance Features Common to DMA, Direct Master, and Direct Slave

- Zero wait state PCI and local bus bursts
- Deep FIFOs prolong bursts
- Unaligned PCI and local bus transfers of any byte length
- On-the-fly Endian conversion
- Programmable local bus wait states
- Parity checking on both buses

Messaging

- Provides industry standard I_2O r1.5 messaging unit
- Supports general-purpose messaging for proprietary message schemes
  - Eight 32-bit mailbox registers for polled environments
  - Two 32-bit doorbell registers for interrupt driven environments

Embedded Host Features

- PCI arbiter supports 7 external masters
- Reset and interrupt signals configurable for embedded host operation
- Type 0/1 Configuration support allows local bus master to configure PCI bus and devices

Package

- 256-ball fine pitch PBGA (FPBGA)
  - 17 mm x 17 mm, 1.00 mm ball pitch
  - Low power 2.5V CMOS core
  - 3.3V I/O, 5V tolerant
  - Industrial temperature range operation
  - IEEE 1149.1 JTAG boundary scan

Backward Compatibility

- The PCI 9056 register set is backward compatible with the PCI 9054, with new registers added for functionality enhancements

Related PLX Products

- Support for 64-bit, 66MHz PCI with 32-bit, 66MHz C, J, and M Local Bus Support is provided by the PCI 9656
  - See the PCI 9656 product brief for details

PCI 9056 Applications

Motorola PowerQUICC Designs

The PCI 9056 is ideal for MPC 850/860-based PowerQUICC designs that target datacom and telecom applications such as high-speed routers/switches, Frame Relay adapters, WAN/LAN controllers, and modem cards.

The PCI 9056 simplifies these designs by providing an enhanced direct-connect interface to the PowerQUICC processor family. The flexible 3.3V, 5V tolerant I/O buffers, combined with local bus operation up to 66MHz, are ideally suited for current and future PowerQUICC processors.

The PCI 9056 supports the PowerQUICC IDMA channels for data transfer between the integrated PowerQUICC communication channels and PCI.

In addition, the PCI 9056 exploits PLX's leading edge Data Pipe Architecture technology, allowing unlimited bursts, as illustrated in the figure below.

❶ For PowerQUICC IDMA operation, the PCI 9056 transfers data to the PCI bus under the control of the IDMA handshake protocol using Direct Master transfers.

❷ Simultaneously, the two PCI 9056 DMA channels run as masters on both buses to perform bi-directional data transfers between the local bus and the PCI bus.

This is a prime example of how the PCI 9056 gives PowerQUICC designers greater flexibility in implementing multiple simultaneous I/O transfers.

Generic 32-bit, 66MHz Local Bus Designs

The PCI 9056 also supports two generic de facto standard bus interfaces, one with demultiplexed and the other with multiplexed address and data busses. Due to their high speed and relative simplicity, these C and J bus modes have been embraced by designers of a wide variety of devices including processors, DSPs, memories, custom ASICs, and FPGAs.

CompactPCI Adapters

The PCI 9056 is the ideal choice for CompactPCI adapters in industrial, telecom, and networking applications. These applications include WAN/LAN controllers, modem cards, Frame Relay adapters, and telephony cards for telecom switches and remote-access systems.

The PCI 9056 has integrated key features to enable live insertion and extraction of CompactPCI Hot Swap adapters. The PCI 9056 is PICMG 2.1 r2.0 Hot Swap Silicon, supporting Programming Interface 0 (PI=0). It includes Bias Voltage and Early power support for ease of Hot Swap board design. Further, the PCI 9056 includes an option to suppress PCI target retries during chip intialization, providing the optimal behavior for live insertion in Hot Swap systems.

The PCI 9056, with its internal PCI arbiter, reset signal direction control, and Type 0/1 PCI configuration support, is ideal for CompactPCI system cards.

PCI Adapters

The PCI 9056 is also designed for traditional PCI adapter card applications requiring 32-bit, 66MHz PCI operation and bandwidth. Specific applications are high performance communications, networking, disk control, RAID, and data encryption adapters.

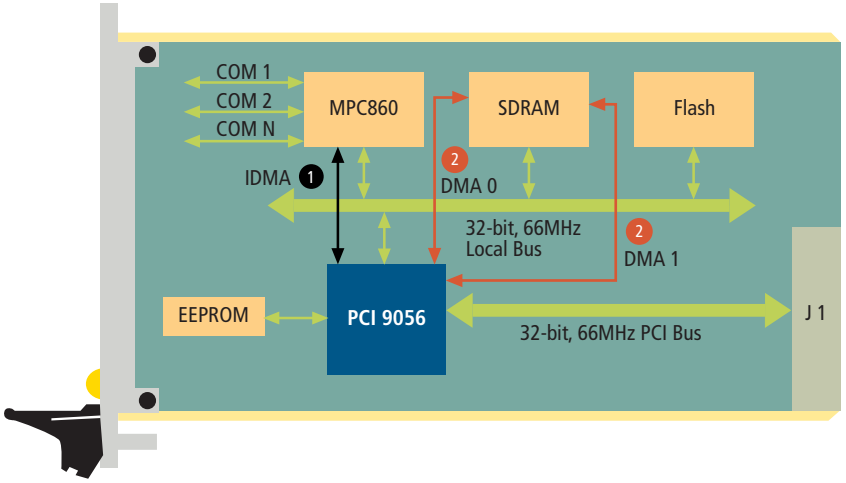
Today, Power Management and Green PCs are major initiatives in traditional PCI applications. The PCI 9056 supports PCI power management, including generation of PME in the $D3_{COLD}$ state. This is a requirement for modem and communications adapters in Windows 98 and 2000 systems.

Embedded Host Designs

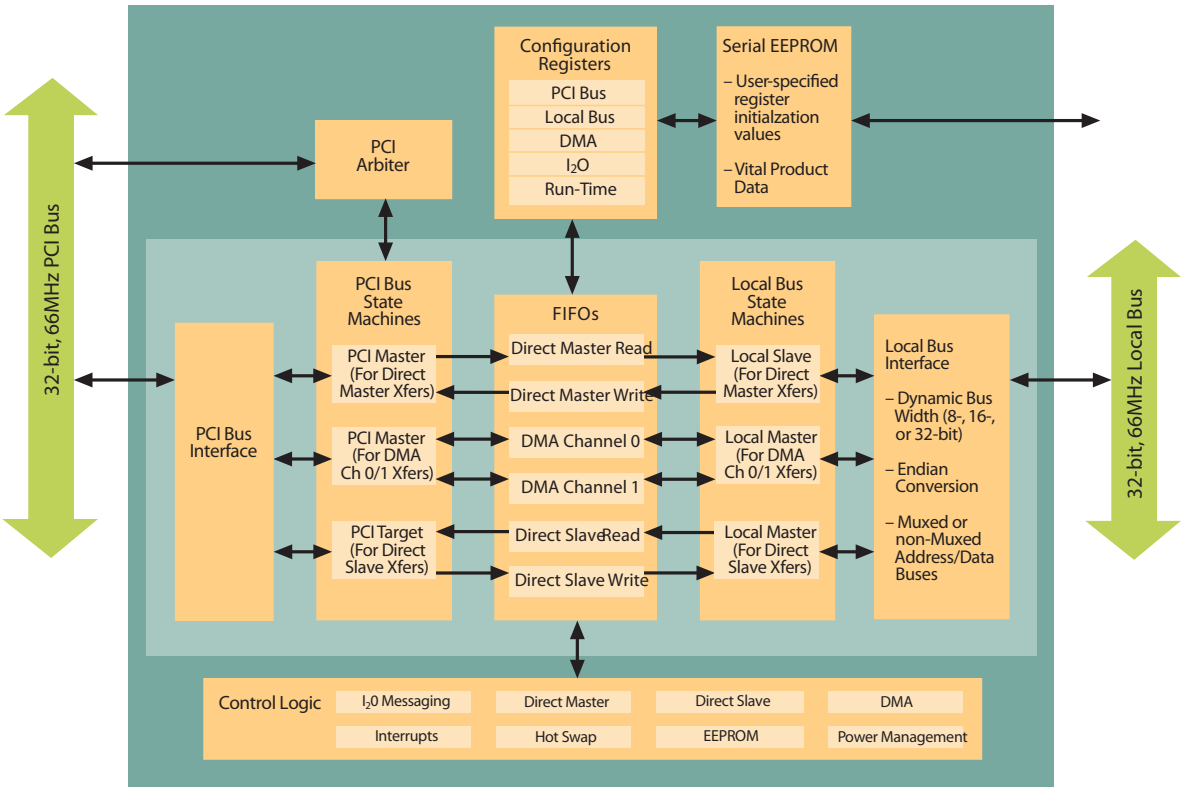
I/O intensive embedded host designs are another major application of the PCI 9056. These applications include network switches/routers, printer engines, set-top boxes, CompactPCI system cards, and industrial equipment.

While the support requirements of these embedded host designs share many similarities with peripheral card designs, there are three significant differences:

- A host must configure the PCI bus. The PCI 9056 supports PCI Type 0 and Type 1 configuration cycles.
- A host must provide a PCI bus arbiter. The PCI 9056 arbiter supports seven external PCI masters, enough for a CompactPCI backplane with 7 peripheral slots.
- For hosts, the directions of reset and interrupt signals reverse. The PCI 9056 includes a strapping option to accomplish this. In one setting, the directions are appropriate for a peripheral. In the other, they are appropriate for a host.



PCI 9056 PowerQUICC CompactPCI Adapter



PCI 9056 Internal Block Diagram

Product Ordering Information

Development Tools Support

To minimize risk and lower your product development costs, PLX offers Software Development Kits (SDKs) and Rapid Development Kits (RDKs) that support the PCI 9056. These kits enable designers to quickly bring new designs to production.

PLX recognizes that software often represents the largest investment in development. The PCI 9056 is fully compliant with PLX's SDK-LITE and SDK-PRO that enable quick and easy development of high performance local processor and host PCI software through standard APIs, I $_2$O messaging protocols, PCI debug tools, and sample drivers.

The PCI 9056 design support is provided through RDKs that include a robust PCI development platform, complete with OrCAD schematics, documentation, a PCI 9056 chip sample, and software.

Product Ordering Information

Part Number	Description
PCI 9056-BA66BI	32-bit, 66 MHz PCI Bus Mastering I/O Accelerator for Motorola PowerQUICC and Generic 32-bit, 66MHz Local Bus Designs
PCI 9056-BA66BI G	32-bit, 66 MHz PCI Bus Mastering I/O Accelerator for Motorola PowerQUICC and Generic 32-bit, 66MHz Local Bus Designs (Lead-Free)
CompactPCI 9056RDK-860	CompactPCI 9056 Rapid Development Kit with Motorola MPC860 PowerQUICC CPU and communications channels
PCI 9056RDK-LITE	PCI 9056 Rapid Development Kit with prototyping area for C, J, & M mode Local Bus designs
SDK-LITE	Windows Host-Side Software Development Kit for PLX I/O Accelerators and I/O Processors
SDK-PRO	Windows Host-Side and Local-Side Software Development Kit for PLX I/O Accelerators and I/O Processors

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for pricing and samples.

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