19-0971; Rev 0; 9/07

EVALUATION KIT AVAILABLE

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

General Description

The MAX8798 includes a high-performance, step-up regulator; a high-speed operational amplifier; a digitally adjustable VCOM calibration device with nonvolatile memory and an I²C interface; and a high-voltage, level-shifting scan driver. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The step-up DC-DC converter provides the regulated supply voltage for panel source driver ICs. The high switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode control architecture provides fast transient response to pulsed loads typical of source driver loads. The step-up regulator features soft-start and current limit.

The high-current operational amplifier is designed to drive the LCD backplane (VCOM). The amplifier features high output current (±150mA), fast slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail inputs and outputs.

The programmable VCOM calibrator is externally attached to the VCOM amplifier's resistive voltage-divider and sinks a programmable current to adjust the VCOM output-voltage level. An internal 7-bit digital-to-analog converter (DAC) controls the sink current. The DAC is ratiometric relative to BOOST and is guaranteed to be monotonic over all operating conditions. The calibrator IC includes an EEPROM to store the desired VCOM voltage level. The 2-wire I²C interface between the LCD panel and the programming circuit minimizes panel connector pin count and simplifies production equipment.

The high-voltage, level-shifting scan driver is designed to drive the TFT panel gate drivers. Its three outputs swing from +35V (maximum) to -25V (minimum) and can swiftly drive capacitive loads. To save power, the two complementary outputs are designed to allow charge sharing during state changes.

The MAX8798 is available in a 36-pin, thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

Applications

Notebook Computer Displays

LCD Monitor Panels

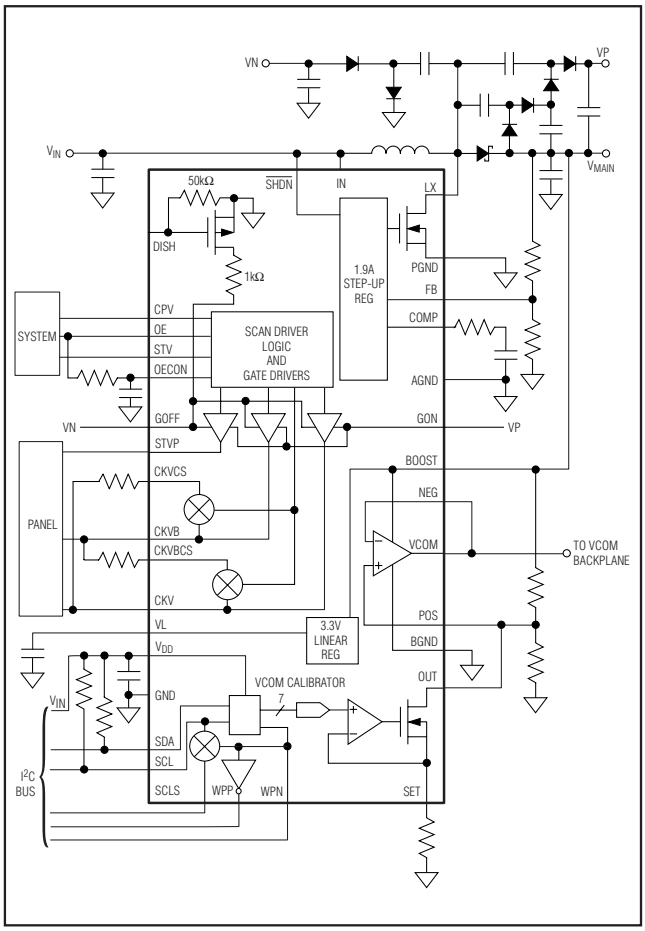
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8798ETX+	-40°C to +85°C	36 Thin QFN 6mm x 6 mm	T-3666M-1

Features

- ♦ **1.8V to 5.5V IN Supply Voltage Range**
- ♦ **1.8V to 4.0V V_{DD} Input Voltage Range**
- ♦ **1.2MHz Current-Mode Step-Up Regulator**
  - **Fast Transient Response**
  - **Built-In 20V, 1.9A, 150mΩ MOSFET**
- ♦ **High-Speed (20MHz) Operational Amplifier**
  - **±150mA Output Current**
- ♦ **High-Voltage Drivers with Scan Logic**
  - **+35V to -25V Outputs**
  - **Output Charge Sharing**
- ♦ **Programmable VCOM Calibrator**
  - **7-Bit Adjustable Current-Sink Output**
  - **I²C Interface**
  - **EEPROM Setting Memory**
- ♦ **Thermal-Overload Protection**

Simplified Operating Circuit



Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

IN, VL, $\overline{SHDN}$ to AGND .....-0.3V to +7.5V
V_{DD}, SDA, SCL, SCLS, WPN, WPP, SET to GND...-0.3V to +4.0V
OECON, CPV, OE, STV to AGND.....-0.3V to +4.0V
COMP, FB to AGND .....-0.3V to (V_L + 0.3V)
DISH to GND .....-6V to +0.3V
LX to PGND .....-0.3V to +20V
OUT, VCOM, NEG, POS to BGND.....-0.3V to (BOOST + 0.3V)
PGND, BGND, AGND to GND.....-0.3V to +0.3V
GON to AGND.....-0.3V to +40V
GOFF to AGND .....-30V to (V_{IN} + 0.3V)
BOOST to BGND.....-0.3V to +20V
CKV, CKVB, STVP, CKVCS,
CKVBCS to AGND.....(GOFF - 0.3V) to (GON + 0.3V)
LX, PGND RMS Current Rating.....2.4A
Continuous Power Dissipation (T_A = +70°C)
NiPd Lead Frame with Nonconductive Epoxy
36-Pin, 6mm x 6mm Thin QFN
(derate 27.2mW/°C above +70°C) 2179.8mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Input Voltage Range		1.8		4.0	V
V_{DD} Quiescent Current	V_{DD} = 3V		4	10	µA
V_{DD} Undervoltage Lockout	V_{DD} rising; typical hysteresis 100mV		1.3	1.75	V
IN Input Voltage Range	(Note 1)	1.8		6.0	V
IN Quiescent Current	V_{IN} = 3V, V_{FB} = 1.5V, not switching		0.04	0.1	mA
IN Undervoltage Lockout	IN rising; typical hysteresis 100mV		1.4	1.75	V
Thermal Shutdown	Rising edge, hysteresis = 15°C		160		°C
BOOTSTRAP LINEAR REGULATOR (VL)					
VL Output Voltage	I_{VL} = 100µA	3.15	3.3	3.45	V
VL Undervoltage Lockout	VL rising, typical hysteresis 200mV	2.4	2.7	3.0	V
VL Maximum Output Current	V_{FB} = 1.1V	10			mA
MAIN DC-DC CONVERTER					
BOOST Supply Current	LX not switching, no load on VL		1.5	2	mA
	LX switching, no load on VL		3	4	
Operating Frequency		990	1170	1350	kHz
Oscillator Maximum Duty Cycle		88	92	96	%
FB Regulation Voltage		1.216	1.235	1.254	V
FB Load Regulation	0 < I_{LOAD} < 200mA, transient only		-1		%
FB Line Regulation	V_{IN} = 1.8V to 5.5V, FB to COMP	-0.15	-0.08	+0.15	%/V
FB Input Bias Current	V_{FB} = 1.25V	50	125	200	nA
FB Transconductance	ΔI = 5µA at COMP	70	160	280	µS
FB Voltage Gain	FB to COMP		2400		V/V
FB Fault Timer Trip Threshold	Falling edge	0.96	1	1.04	V
LX On-Resistance	I_{LX} = 1.2A		150	300	mΩ
LX Leakage Current	V_{LX} = 18V		0.01	20	µA
LX Current Limit	Duty cycle = 65%	1.6	1.9	2.2	A
Current-Sense Transresistance		0.25	0.42	0.55	V/A
Soft-Start Period			3		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATIONAL AMPLIFIER					
BOOST Supply Range		5		18	V
BOOST Overvoltage Fault Threshold	(Note 2)	18.1	19	19.9	V
BOOST Undervoltage Fault Threshold	(Note 3)		1.0	1.4	V
Large-Signal Voltage Gain	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)		120		dB
Common-Mode Rejection Ratio	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)		75		dB
Input Offset Voltage	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)	-25	-5	+25	mV
	V_{BOOST}/2	+15	-2.5	+12	
Input Bias Current	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)	-50		+50	nA
Input Common-Mode Voltage Range	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)	0		V_{BOOST}	V
VCOM Output Voltage Swing High	I_{VCOM} = 5mA	V_{BOOST} - 100	V_{BOOST} - 50		mV
VCOM Output Voltage Swing Low	I_{VCOM} = -5mA		50	100	mV
VCOM Output-Current High	V_{VCOM} = V_{BOOST} - 1V		-75		mA
VCOM Output-Current Low	V_{VCOM} = 1V		+75		mA
Slew Rate	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)		40		V/µs
-3dB Bandwidth	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)		20		MHz
VCOM Short-Circuit Current	Short to V_{BOOST}/2, sourcing	50	150		mA
	Short to V_{BOOST}/2, sinking	50	150		
PROGRAMMABLE VCOM CALIBRATOR					
GON Input Range		16.1		35.0	V
GON Threshold to Enable Program	Rising edge, 60mV hysteresis		15.6	16.0	V
SET Voltage Resolution		7			Bits
SET Differential Nonlinearity	Monotonic overtemperature	-2		+2	LSB
SET Zero-Scale Error		-1	+1	+2	LSB
SET Full-Scale Error		-3		+3	LSB
SET Current				120	µA
SET External Resistance (Note 4)	To GND, V_{BOOST} = 18V	8.5		170.0	kΩ
	To GND, V_{BOOST} = 6V	2.5		50.0	
V_{SET}/V_{BOOST} Voltage Ratio	DAC full scale		0.05		V/V
OUT Leakage Current	When OUT is off		1		nA
OUT Settling Time	To ±0.5 LSB error band		20		µs
OUT Voltage Range		V_{SET} + 0.5V		18	V
EEPROM Write Cycles	(Note 5)	1000			Times

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE INTERFACE					
Logic-Input Low Voltage (V_{IL})	SDA, SCL, WPN, V_{DD} = 3V			0.3 x V_{DD}	V
Logic-Input High Voltage (V_{IH})	SDA, SCL, WPN, V_{DD} = 3V	0.7 x V_{DD}			V
WPP Logic-Output Low Voltage	I_{WPP} = 1mA			+0.1	V
WPP Logic-Output High Voltage	I_{WPP} = 1mA	V_{DD} - 0.1			V
SDA Logic-Output Low Sink Current	SDA forced to 3.3V	6			mA
Logic Input Current	SDA, SCL, SCL_S,WPN to VDD or GND	-1		+1	µA
Input Capacitance	SDA, SCL, SCL_S		5		pF
SCL Frequency (f_{CLK})		DC		500	kHz
SCL High Time (t_{CLH})		600			ns
SCL Low Time (t_{CLL})		1300			ns
SDA, SCL, SCLS Rise Time (t_R)	C_{BUS} = total capacitance of bus line in pF	20 + 10 x C_{BUS}		300	ns
SDA, SCL, SCLS Fall Time (t_F)	C_{BUS} = total capacitance of bus line in pF	20 + 10 x C_{BUS}		300	ns
START Condition Hold Time (t_{HDSTT})	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time (t_{SVSTT})		600			ns
Data Input Hold Time (t_{HDDAT})		0			ns
Data Input Setup Time (t_{SUDAT})		150			ns
STOP Condition Setup Time (t_{SVSTP})		600			ns
Bus Free Time (t_{UF})		1300			ns
Input Filter Spike Suppression (t_{SP})	SDA, SCL (Note 5)			250	ns
SCL-SCLS Switch Resistance	WPN = GND	1			MΩ
	WPN = VDD		20	50	Ω
HIGH-VOLTAGE SCAN DRIVER					
GON Input Voltage Range		12		35	V
GOFF Input Voltage Range		-25		-2	V
GON Supply Current	STV, CPV, OE, OECON = AGND		250	350	µA
GOFF Supply Current	STV, CPV, OE, OECON = AGND		100	200	µA
Output-Voltage Low	CKV, CKVB, STVP, -5mA output current	V_{GOFF} + 0.2	V_{GOFF} + 0.05		V
Output-Voltage High	CKV, CKVB, STVP, 5mA output current		V_{GON} - 0.05	V_{GON} - 0.2	V
Propagation Delay Between OE Rising Edge and CKV/CKVB Edge	CPV = 0, STV = 0, C_{LOAD} = 4.7nF, 50Ω		250	450	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate CKV, CKVB	Without charge sharing, STV = V_{DD}, C_{LOAD} = 4.7nF, 50Ω	20	40		V/µs
Propagation Delay Between STV and STVP	C_{LOAD} = 4.7nF		250	450	ns
STVP Output Slew Rate	C_{LOAD} = 4.7nF, 50Ω	20	40		V/µs
Charge-Sharing Discharge Path Resistance	CKV to CKVCS and CKVB to CKVBCS		250	400	Ω
DISH Discharge Path Resistance	GOFF to -3V, DISH = -3V		250	500	Ω
DISH Turn-On Threshold	Dish falling			-1.8	V
STV, CPV, OE Input Low Voltage				0.8	V
STV, CPV, OE Input High Voltage		1.6			V
OECON Input Low Voltage				1.5	V
OECON Input High Voltage		2.0			V
OECON Sink Current	OECON = 5W = V_{DD}	0.4	0.8		mA
STV, CPV, OE Input Current	V_{STV} = V_{DD} or GND, V_{CPV} = V_{DD} or GND, V_{OE} = V_{DD} or GND, V_{OECON} = V_{DD} or GND	-1		+1	µA
CKV, CKVB, STVP Output Three-State Current	V_{CKV} = GON or GOFF, three-state V_{CKVB} = GON or GOFF, three-state V_{CKVCS} = GON or GOFF, three-state V_{CKVBCS} = GON or GOFF, three-state V_{STVP} = GON or GOFF, three-state	-1		+1	µA
CONTROL INPUTS					
Input Low Voltage	$\overline{SHDN}$			0.6	V
Input High Voltage	$\overline{SHDN}$, 1.8V < V_{IN} < 3.0V	1.8			V
	$\overline{SHDN}$, 3.0V < V_{IN} < 5.5V	2.0			
$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 0V or 3V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Input Voltage Range		1.8		4.0	V
V_{DD} Quiescent Current	V_{DD} = 3V			10	µA
V_{DD} Undervoltage Lockout	V_{DD} rising; typical hysteresis 100mV			1.75	V
IN Input Voltage Range	(Note 1)	1.8		6.0	V
IN Quiescent Current	V_{IN} = 3V, V_{FB} = 1.5V, not switching			0.1	mA
IN Undervoltage Lockout	IN rising; typical hysteresis 100mV			1.75	V

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BOOTSTRAP LINEAR REGULATOR (VL)					
VL Output Voltage	I_{VL} = 100µA	3.15		3.45	V
VL Undervoltage Lockout	VL rising, typical hysteresis 100mV	2.4		3.0	V
MAIN DC-DC CONVERTER					
BOOST Supply Current	LX not switching, no load on VL			2	mA
	LX switching, no load on VL			4	
Operating Frequency		990		1350	kHz
Oscillator Maximum Duty Cycle		88		96	%
FB Regulation Voltage		1.216		1.254	V
FB Line Regulation	V_{IN} = 1.8V to 5.5V, FB to COMP	-0.15		+0.15	%/V
FB Transconductance	ΔI = 5µA at COMP	70		280	µS
FB Fault-Timer Trip Threshold	Falling edge	0.96		1.04	V
LX On-Resistance	I_{LX} = 1.2A			300	mΩ
LX Current Limit	Duty cycle = 65%	1.6		2.2	A
OPERATIONAL AMPLIFIER					
BOOST Supply Range		5		18	V
BOOST Overvoltage Fault Threshold	(Note 2)	18.1		19.9	V
BOOST Undervoltage Fault Threshold	(Note 3)			1.4	V
Input Offset Voltage	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)	-25		+25	mV
Input Common-Mode Voltage Range	1V < (V_{NEG}, V_{POS}) < (V_{BOOST} - 1V)	0		V_{BOOST}	V
VCOM Output-Voltage Swing High	I_{VCOM} = 5mA	V_{BOOST} - 100			mV
VCOM Output-Voltage Swing Low	I_{VCOM} = -5mA			100	mV
VCOM Short-Circuit Current	Short to V_{BOOST}/2, sourcing	50			mA
	Short to V_{BOOST}/2, sinking	50			
PROGRAMMABLE VCOM CALIBRATOR					
GON Input Range		16.1		35.0	V
GON Threshold to Enable Program	Rising edge, 60mV hysteresis			16.0	V
SET Voltage Resolution		7			Bits
SET Differential Nonlinearity	Monotonic overtemperature	-2		+2	LSB
SET Zero-Scale Error		-1		+2	LSB
SET Full-Scale Error		-3		+3	LSB
SET Current				120	µA
SET External Resistance (Note 4)	To GND, V_{BOOST} = 18V	8.5		170.0	kΩ
	To GND, V_{BOOST} = 6V	2.5		50.0	
OUT Voltage Range		V_{SET} + 0.5V		18	V
EEPROM Write Cycles	(Note 5)	1000			Times

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE INTERFACE					
Logic-Input Low Voltage (V_{IL})	SDA, SCL, WPN, V_{DD} = 3V			0.3 x V_{DD}	V
Logic-Input High Voltage (V_{IH})	SDA, SCL, WPN, V_{DD} = 3V	0.7 x V_{DD}			V
WPP Logic-Output Low Voltage	I_{WPP} = 1mA			+0.1	V
WPP Logic-Output High Voltage	I_{WPP} = -1mA	V_{DD} - 0.1			V
SDA Logic-Output Low Sink Current	SDA forced to 3.3V	6			mA
SCL Frequency (f_{CLK})		DC		500	kHz
SCL High Time (t_{CLH})		600			ns
SCL Low Time (t_{CLL})		1300			ns
SDA, SCLS, and SCL Rise Time (t_R)	C_{BUS} = total capacitance of bus line in pF	20 + 10 x C_{BUS}		300	ns
SDA, SCLS, and SCL Fall Time (t_F)	C_{BUS} = total capacitance of bus line in pF	20 + 10 x C_{BUS}		300	ns
START Condition Hold Time (t_{HDSTT})	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time (t_{SVSTT})		600			ns
Data Input Hold Time (t_{HDDAT})		0			ns
Data Input Setup Time (t_{SUDAT})		150			ns
STOP Condition Setup Time (t_{SVSTP})		600			ns
Bus Free Time (t_{UF})		1300			ns
Input Filter Spike Suppression (t_{SP})	SDA, SCL (Note 5)			250	ns
SCL-SCLS Switch Resistance	WPN = GND	1			MΩ
	WPN = V_{DD}			50	Ω
HIGH-VOLTAGE SCAN DRIVER					
GON Input Voltage Range		12		35	V
GOFF Input Voltage Range		-25		-2	V
GON Supply Current	STV, CPV, OE, OECON = AGND			350	µA
GOFF Supply Current	STV, CPV, OE, OECON = AGND			200	µA
Output-Voltage Low	CKV, CKVB, STVP, -5mA output current	V_{GOFF} + 0.2			V
Output-Voltage High	CKV, CKVB, STVP, 5mA output current			V_{GON} - 0.2	V

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, BOOST = 8V, GON = 23V, GOFF = -12V, V_{POS} = 0V, V_{NEG} = 1.5V, OE = CPV = STV = OECON = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Between OE Rising Edge and CKV/CKVB Edge	CPV = 0, STV = 0, C_{LOAD} = 4.7nF, 50Ω			450	ns
Output Slew Rate CKV, CKVB	Without charge sharing, STV = V_{DD}, C_{LOAD} = 4.7nF, 50Ω	20			V/µs
Propagation Delay Between STV and STVP	C_{LOAD} = 4.7nF			450	ns
STVP Output Slew Rate	C_{LOAD} = 4.7nF, 50Ω	20			V/µs
Charge-Sharing Discharge Path Resistance	CKV to CKVCS and CKVB to CKVBCS			400	Ω
DISH Switch Resistance	GOFF to -3V, DISH = -3V			500	Ω
DISH Turn-On Threshold	Dish falling			-1.8	V
STV, CPV, OE Input Low Voltage				0.8	V
STV, CPV, OE Input High Voltage		1.6			V
OECON Input Low Voltage				1.5	V
OECON Input High Voltage		2.0			V
OECON Sink Current	OECON = STV = V_{DD}	0.4			mA
CONTROL INPUTS					
Input Low Voltage	$\overline{SHDN}$			0.6	V
Input High Voltage	$\overline{SHDN}$, 1.8V < V_{IN} < 3.0V	1.8			V
	$\overline{SHDN}$, 3.0V < V_{IN} < 5.5V	2.0			

Note 1: For 5.5V < V_{IN} < 6.0V, use the MAX8798 for no longer than 1% of IC lifetime. For continuous operation, the input voltage should not exceed 5.5V.

Note 2: Inhibits boost switching if V_{BOOST} exceeds the threshold This fault is not latched.

Note 3: Step-up regulator switching is not enabled until BOOST is above undervoltage threshold.

Note 4: SET external resistor range is verified at DAC full scale.

Note 5: Guaranteed by design, not production tested.

Note 6: -40°C specs are guaranteed by design, not production tested.

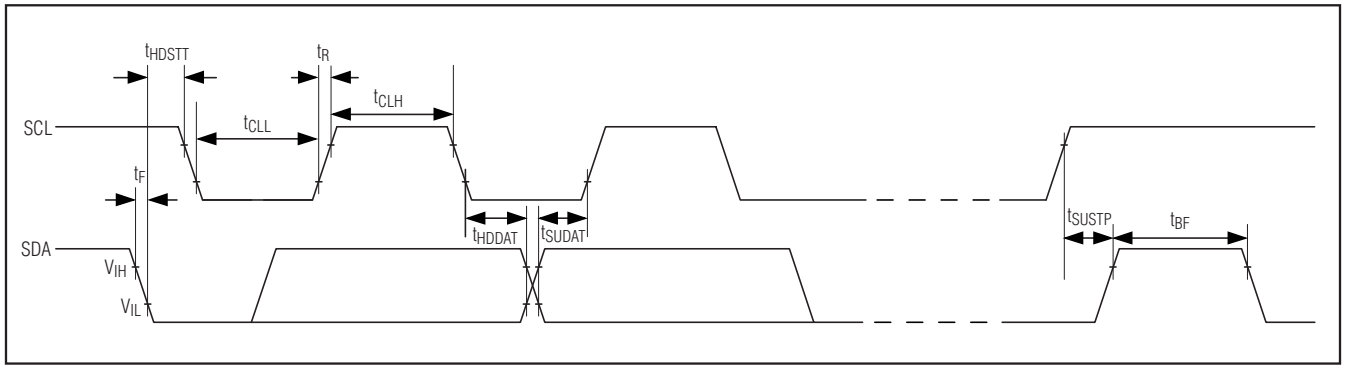


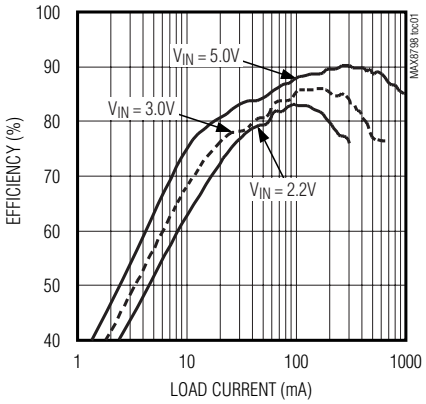
Figure 1. Timing Definitions Used in the Electrical Characteristics

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

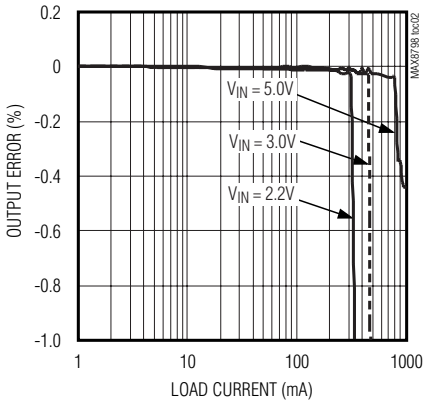
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 3V, T_A = +25°C, unless otherwise noted.)

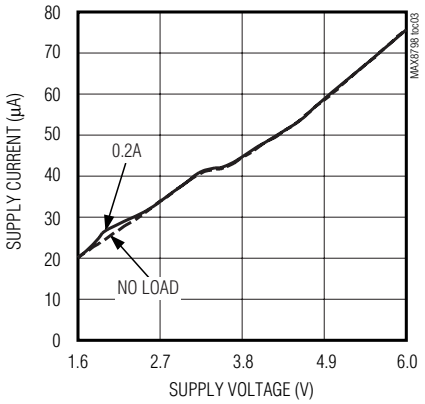
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



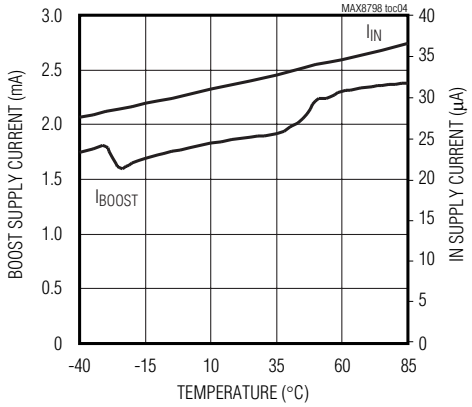
STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



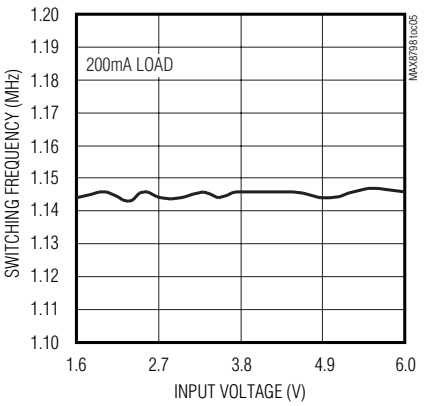
IN SUPPLY QUIESCENT CURRENT vs. IN SUPPLY VOLTAGE



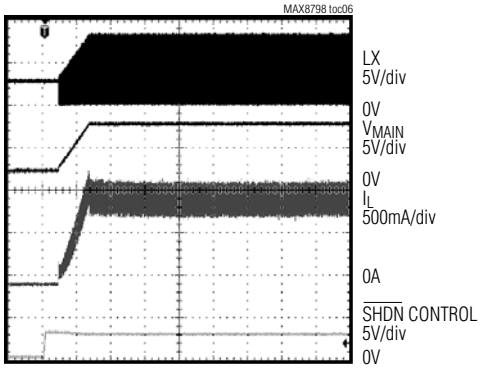
STEP-UP REGULATOR SUPPLY CURRENT vs. TEMPERATURE



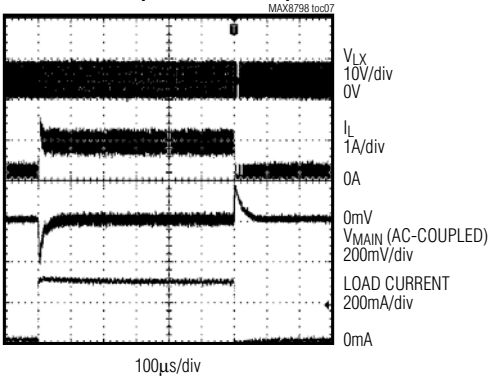
STEP-UP CONVERTER SWITCHING FREQUENCY vs. INPUT VOLTAGE



STEP-UP REGULATOR HEAVY-LOAD SOFT-START



STEP-UP REGULATOR LOAD TRANSIENT RESPONSE (20mA TO 300mA)



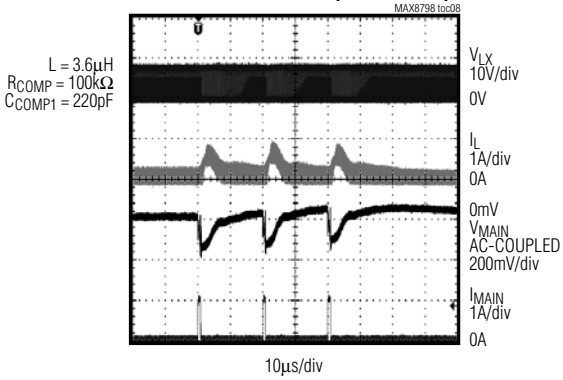
L = 3.6µH
R_{COMP} = 100kΩ
C_{COMP1} = 220pF

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

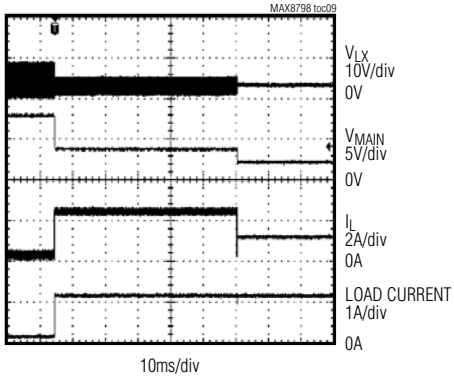
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 3V, T_A = +25°C, unless otherwise noted.)

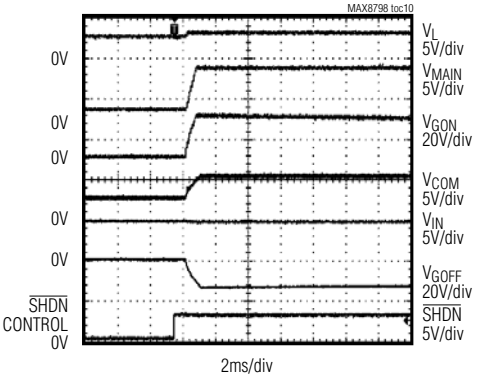
STEP-UP REGULATOR PULSED LOAD TRANSIENT RESPONSE (20mA TO 1A)



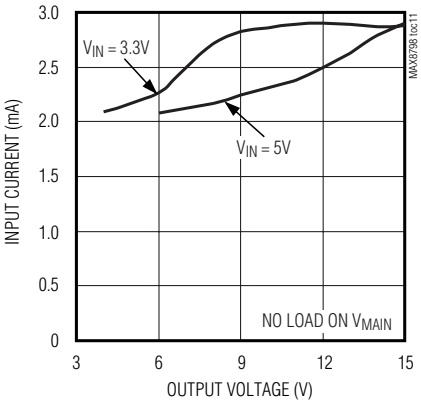
TIMER-DELAY LATCH RESPONSE TO OVERLOAD



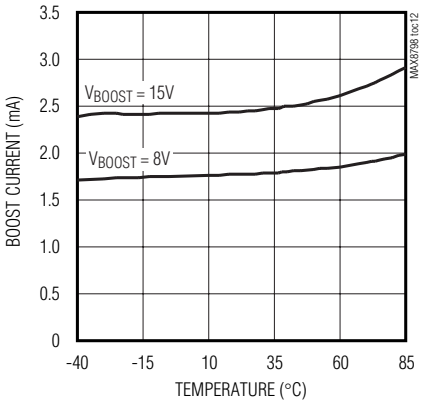
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



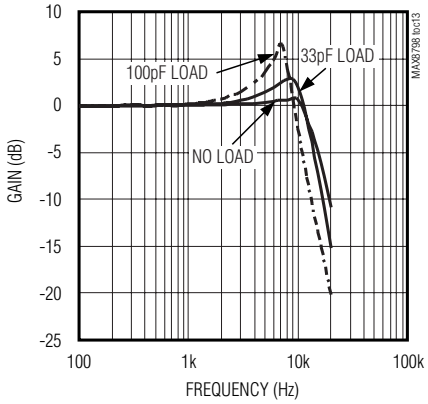
BOOST SUPPLY CURRENT vs. BOOST SUPPLY VOLTAGE



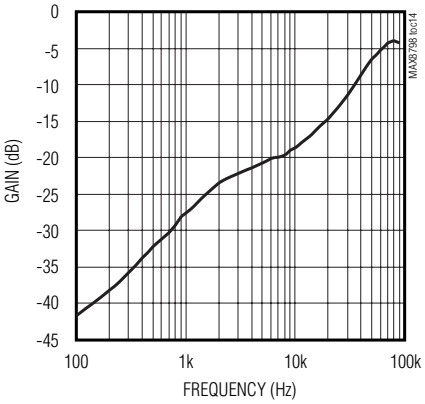
BOOST SUPPLY CURRENT vs. TEMPERATURE



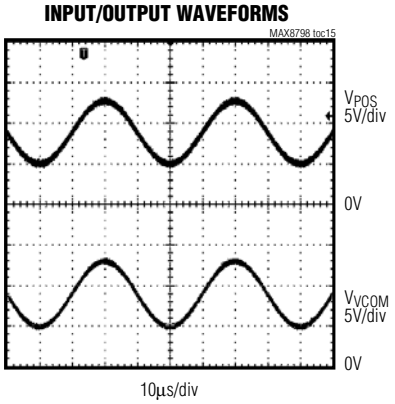
OPERATIONAL AMPLIFIER FREQUENCY RESPONSE



OPERATIONAL AMPLIFIER PSRR vs. FREQUENCY



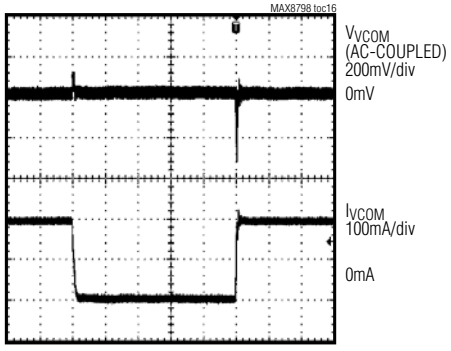
OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS



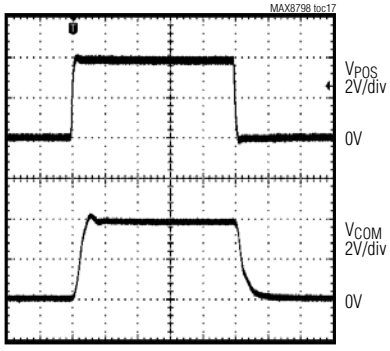
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 3V, T_A = +25°C, unless otherwise noted.)

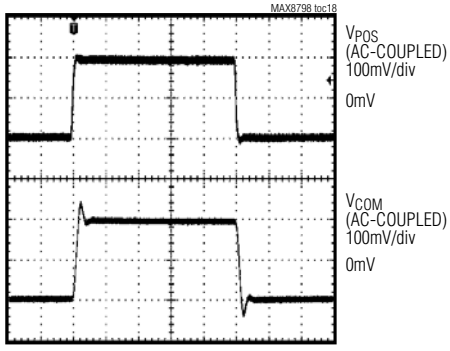
OPERATIONAL AMPLIFIER LOAD TRANSIENT RESPONSE



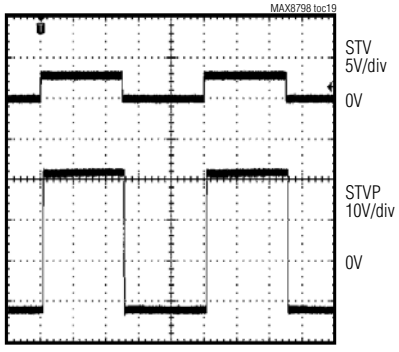
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



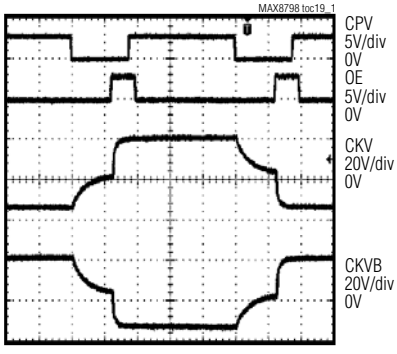
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



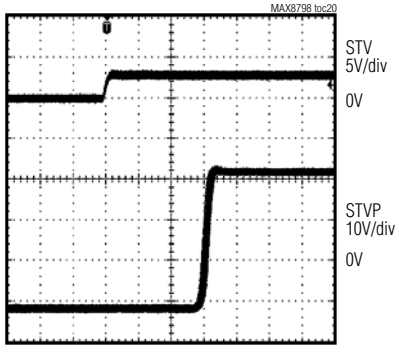
STV/STVP INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT



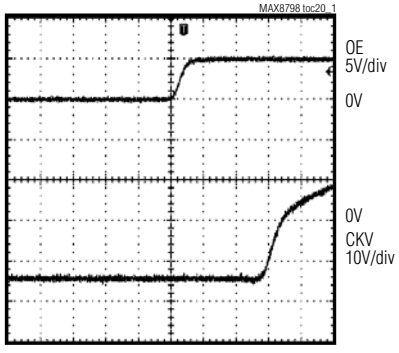
CPV AND OE/CKV AND CKVB INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT (STV = 0V, C_{LOAD} = 5.0nF AND 50Ω, R1, R2 = 200Ω)



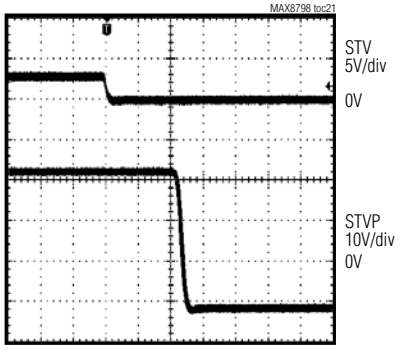
STV RISING EDGE PROPAGATION DELAY



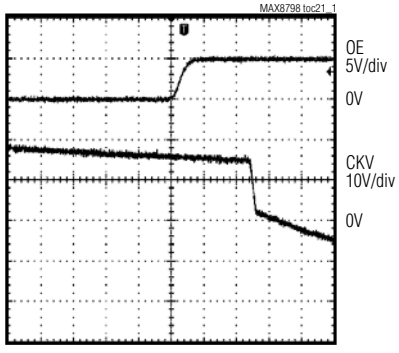
OE/CKV RISING EDGE PROPAGATION DELAY



STV FALLING EDGE PROPAGATION DELAY



OE/CKV FALLING EDGE PROPAGATION DELAY

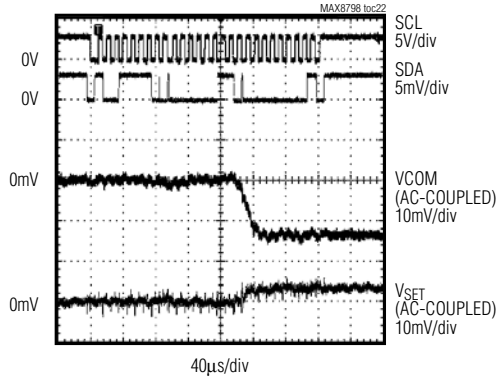


Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

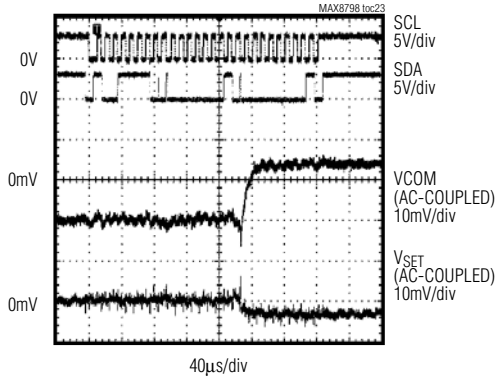
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 3V, T_A = +25°C, unless otherwise noted.)

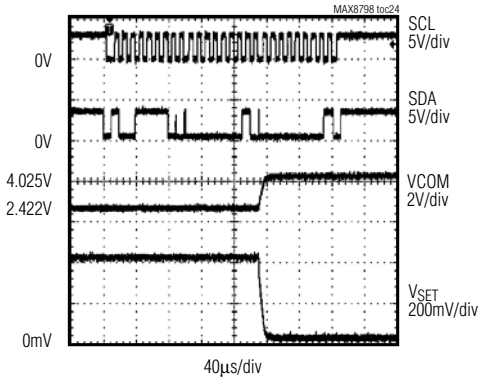
CALIBRATOR SIGNAL LSB DOWNWARD STEP RESPONSE



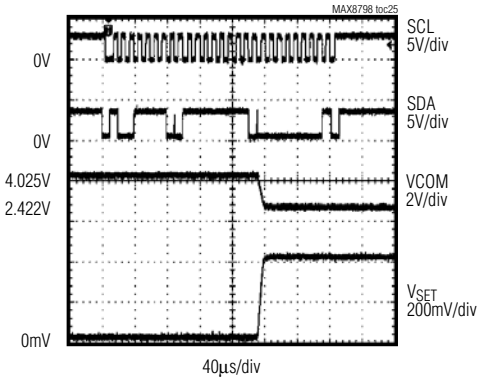
CALIBRATOR SIGNAL LSB UPWARD STEP RESPONSE



CALIBRATOR FULL-SCALE UPWARD STEP RESPONSE



CALIBRATOR FULL-SCALE DOWNWARD STEP RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	CKV	High-Voltage, Gate-Pulse Output. When enabled, CKV toggles between its high state (connected to GON) and its low state (connected to GOFF) on each falling edge of the CPV input. Further, CKV floats whenever CPV and OE are both low or whenever CPV is low and OECON is high.
2	CKVCS	CKV Charge-Sharing Connection. CKVCS connects to CKV whenever CKV floats to allow connection to CKVB, sharing charge between the capacitive loads on these two outputs.
3	CKVBCS	CKVB Charge-Sharing Connection. CKVBCS connects to CKVB whenever CKVB floats to allow connection to CKV, sharing charge between the capacitive loads on these two outputs.
4	CKVB	High-Voltage, Gate-Pulse Output. CKVB is the inverse of CKV during active states and floats whenever CKV floats.
5	STVP	High-Voltage, Start-Pulse Output. STVP is low (connected to GOFF) whenever STV is low and is high (connected to GON) only when STV is high and CPV and OE are both low. When STV is high and either CPV or OE is high, STVP floats.
6	STV	Vertical Sync Input. The rising edge of STV begins a frame of data. The STV input is used to generate the high-voltage STVP output.
7	OECON	Active-Low, Output-Enable Timing Input. OECON is driven by an RC-filtered version of the OE input signal. If OE remains high long enough for the resistor to charge the capacitor up to the OECON threshold, the OE signal is masked until OE goes low and the capacitor is discharged below the threshold through the resistor.
8	OE	Active-High, Gate-Pulse Output Enable. CKV and CKVB leave the floating charge-sharing state on the rising edge of OE.
9	CPV	Vertical Clock-Pulse Input. CPV controls the timing of the CKV and CKVB outputs, which change state (by first sharing charge) on its falling edge.
10	GND	Logic Ground
11	DISH	GOFF Discharge Input. Pulling DISH below ground activates an internal connection between GOFF and GND, rapidly discharging the GOFF supply. Typically, DISH is capacitively connected to IN, so that when V_{IN} falls GOFF is discharged.
12	V_{DD}	Supply Input. Logic supply input for the VCOM calibrator. Bypass to GND through a minimum 0.1µF capacitor.
13	WPN	Active-Low, Write-Protect Input. When WPN is low, I^2C commands are ignored and the VCOM calibrator settings cannot be modified.
14	SCLS	Alternate I^2C-Compatible Clock Input. When WPN is high, SCLS connects to SCL to drive SCL from an alternate clock source.
15	SCL	I^2C-Compatible Clock Input and Output
16	SDA	I^2C-Compatible Serial Bidirectional Data Line
17	WPP	Write-Protect Output. WPP is the inverse of WPN. It can be used to control active-high, write-protect inputs on other devices.
18	SET	Full-Scale, Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from SET to GND to set the full-scale adjustable sink current, which is V_{BOOST} / (20 x R_{SET}). I_{OUT} is equal to the current through R_{SET}.
19	VL	3.3V On-Chip Regulator Output. This regulator powers internal analog circuitry for the step-up regulator, op amp, and VCOM calibrator. External loads up to 10mA can be powered. Bypass VL to GND with a 0.22µF or greater ceramic capacitor.

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Pin Description (continued)

PIN	NAME	FUNCTION
20	BGND	Amplifier Ground
21	BOOST	Operational Amplifier Supply Input. Connect to V_{MAIN} and bypass to BGND with a 1µF or greater ceramic capacitor.
22	OUT	Adjustable Sink-Current Output. OUT connects to the resistive voltage-divider at the op amp input POS (between BOOST and GND) that determines the VCOM output voltage. I_{OUT} lowers the divider voltage by a programmable amount.
23	POS	Operational Amplifier Noninverting Input
24	NEG	Operational Amplifier Inverting Input
25	VCOM	Operational Amplifier Output
26	$\overline{SHDN}$	Shutdown Control Input. Pull $\overline{SHDN}$ low to disable the step-up regulator. The VCOM calibrator, op amp, and scan driver functions remain enabled.
27	IN	Step-Up Regulator Supply Pin. Bypass IN to AGND (pin 34) with a 1µF or greater ceramic capacitor.
28, 29	LX	Switching Node. Connect inductor/catch diode here and minimize trace area for lowest EMI.
30, 31	PGND	Power Ground. Source connection of the internal step-up regulator power switch.
32	FB	Feedback Pin. Reference voltage is 1.24V nominal. Connect external resistor-divider midpoint here and minimize trace area. Set V_{OUT} according to: V_{OUT} = 1.24V (1 + R1/R2).
33	COMP	Compensation Pin for Error Amplifier. Connect a series RC from this pin to AGND. Typical values are 180kΩ and 470pF.
34	AGND	Ground
35	GOFF	Gate-Off Supply. GOFF is the negative supply voltage for the CKV, CKVB, and STVP high-voltage driver outputs. Bypass to PGND with a minimum of 0.1µF ceramic capacitor.
36	GON	Gate-On Supply. GON is the positive supply voltage for the CKV, CKVB, and STVP high-voltage driver outputs. Bypass to V_{MAIN} or PGND with a minimum of 0.1µF ceramic capacitor.
—	EP	Exposed Backside Paddle

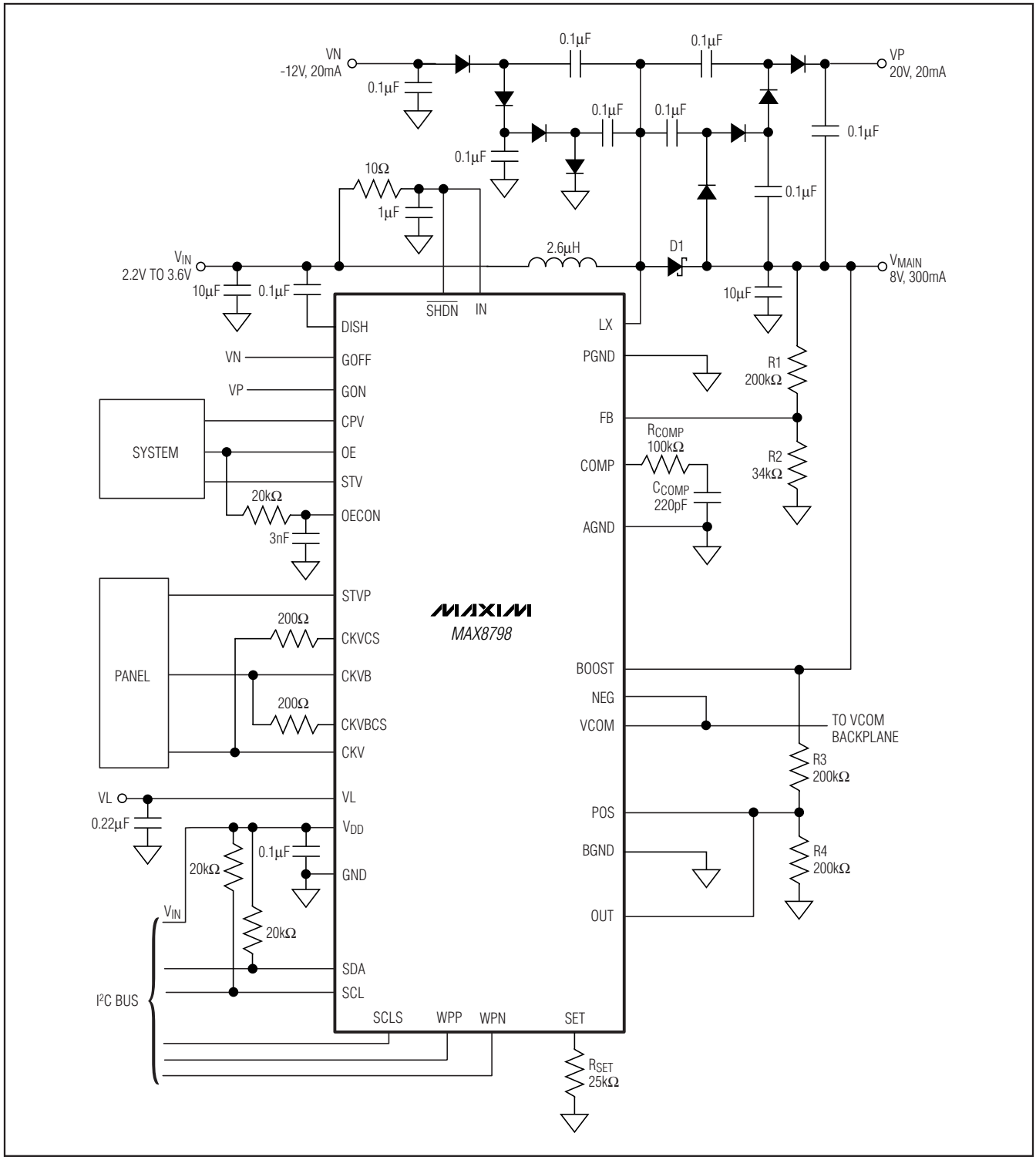


Figure 2. MAX8798 Typical Operating Circuit

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

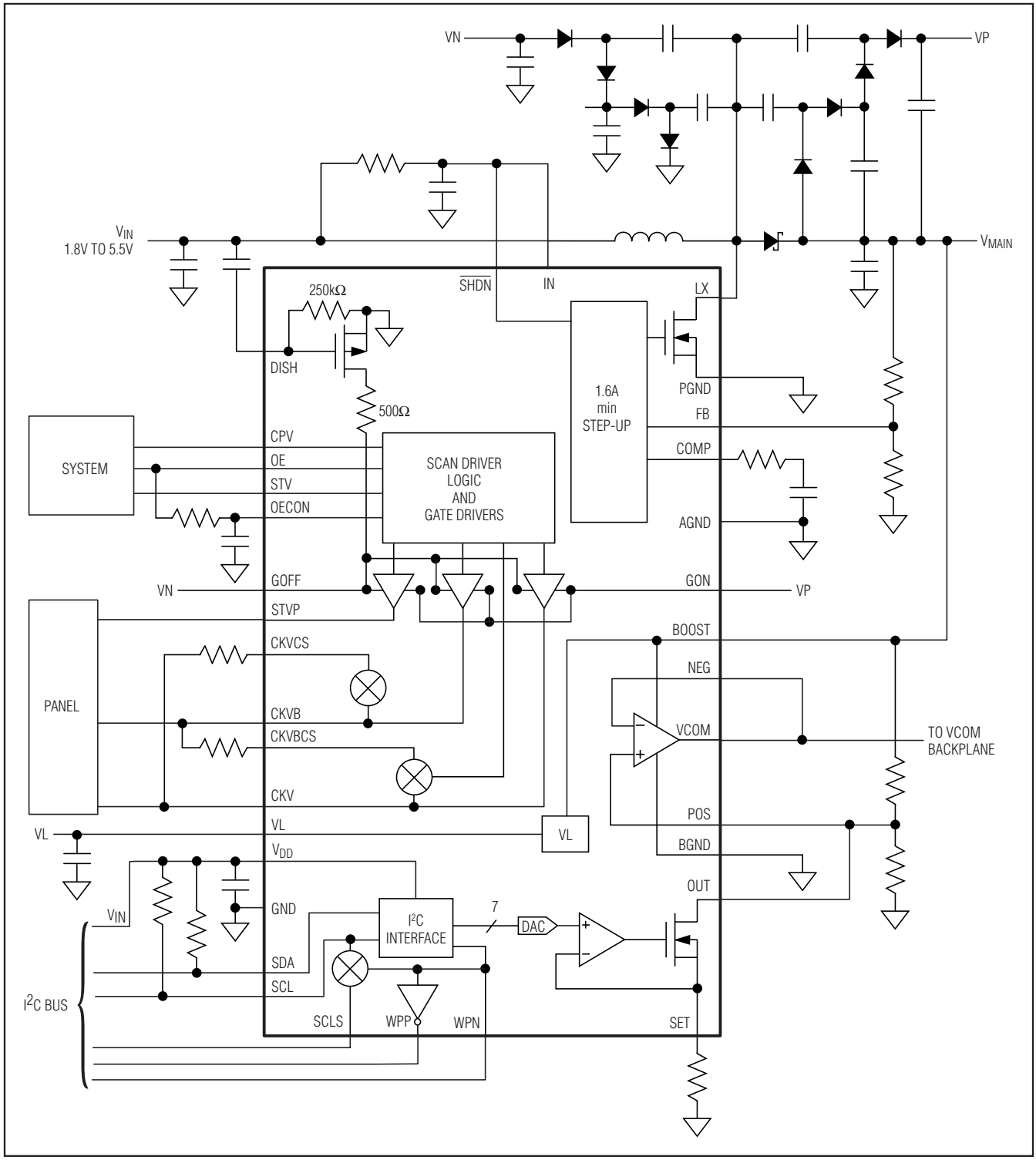


Figure 3. MAX8798 Functional Diagram

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Typical Application Circuit

The MAX8798 typical application circuit (Figure 2) generates a +8V source-driver supply and approximately +20V and -12V gate-driver supplies for TFT displays. The input-voltage range for the IC is from +1.8V to +5.5V, but the Figure 2 circuit is designed to run from 2.2V to 3.6V. Table 1 lists recommended components and Table 2 lists contact information of component suppliers.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1	10µF, 6.3V X5R ceramic capacitor (1206) TDK C3216X5ROJ106M
C21, C22	4.7µF, 10V X5R ceramic capacitors (1206) TDK C3216X5R1A475M
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02
D2–D5	200mA, 100V, dual, ultra-fast diodes (SOT23) Fairchild MMBD4148SE
L1	3.6µH, 1.8A inductor Sumida CM0611BHPNP-3R6MC

Detailed Description

The MAX8798 contains a high-performance step-up switching regulator; one high-speed operational amplifier; one three-channel, high-voltage level-shifting scan driver for active-matrix TFT LCDs; and an I^2C-controlled VCOM calibrator. Figure 3 shows the MAX8798 functional diagram.

Step-Up Regulator

The step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads found in source drivers of TFT LCD panels. The high switching frequency (1.2MHz) allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start functions reduce the number of external components required while controlling inrush current. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Figure 4 shows the block diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.24V and changes the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit compares the input voltage at IN with the UVLO threshold (1.3V rising and 1.2V falling) to ensure that the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and the linear regulator, disables the switch-control block, and the operational amplifier output becomes high impedance.

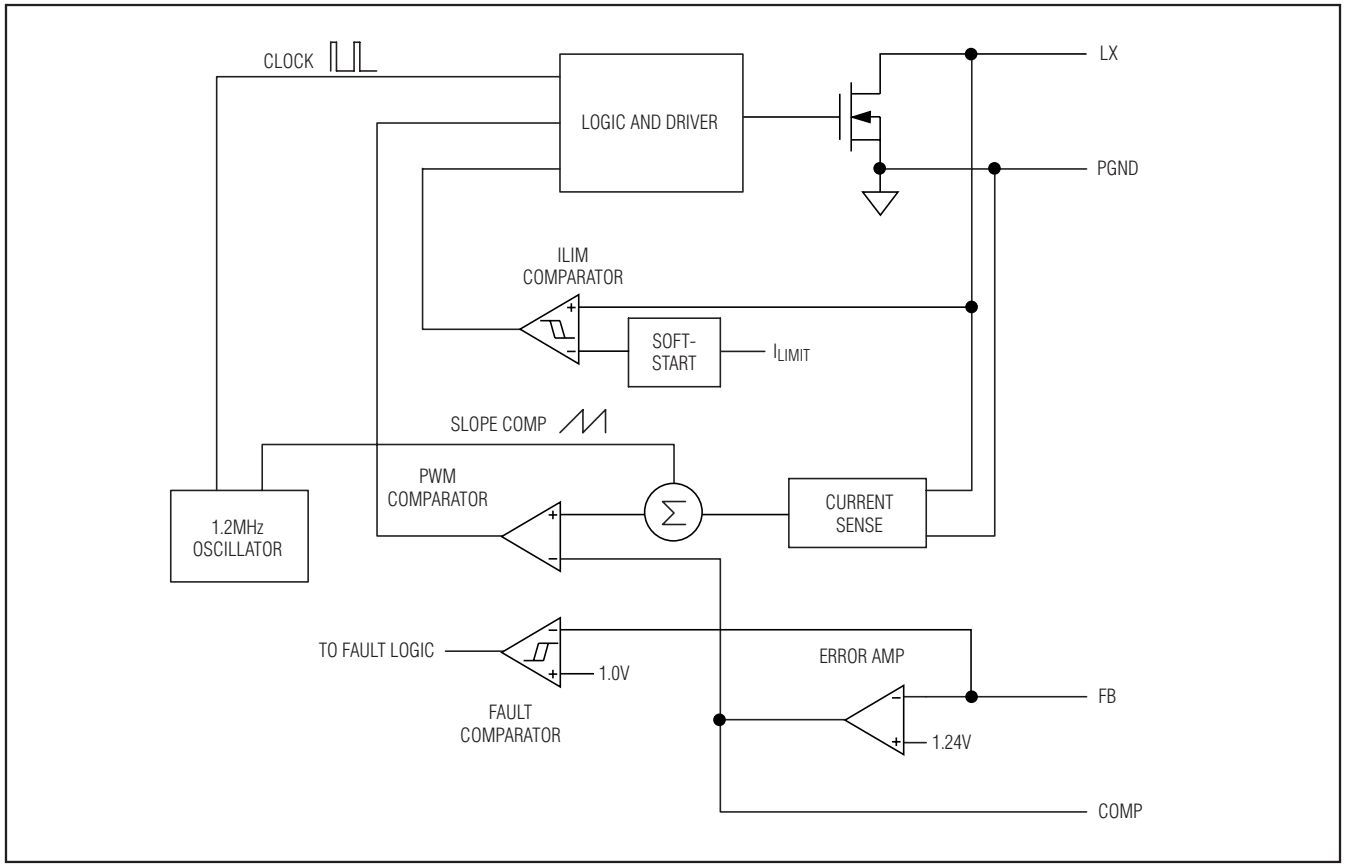


Figure 4. Step-Up Regulator Block Diagram

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Linear Regulator (VL)

The MAX8798 includes an internal 3.3V linear regulator. BOOST is the input of the linear regulator. The input voltage range is between 5V and 18V. The regulator powers all the internal circuitry including the MOSFET gate driver. Bypass the VL pin to AGND with a 0.22µF or greater ceramic capacitor. BOOST should be directly connected to the output of the step-up regulator. This feature significantly improves the efficiency at low input voltages.

Bootstrapping and Soft-Start

The MAX8798 features bootstrapping operation. In normal operation, the internal linear regulator supplies power to the internal circuitry. The input of the linear regulator (BOOST) should be directly connected to the output of the step-up regulator. The MAX8798 is enabled when the voltages at IN and BOOST are above their UVLO thresholds and the fault latch is not set. After being enabled, the regulator starts open-loop switching to generate the supply voltage for the linear regulator. The internal reference block turns on when the VL voltage exceeds its 2.7V (typ). When the reference voltage reaches regulation, the PWM controller and the current-limit circuit are enabled and the step-up regulator enters soft-start. During soft-start, the main step-up regulator directly limits the peak inductor current, allowing from zero up to the full current-limit value in 128 equal current steps. The maximum load current is available after the output voltage reaches regulation (which terminates soft-start), or after the soft-start timer expires in approximately 3ms. The soft-start routine minimizes the inrush current and voltage overshoot and ensures a well-defined startup behavior.

Fault Protection

During steady-state operation, the MAX8798 monitors the FB voltage. If the FB voltage does not exceed 1V (typ), the MAX8798 activates an internal fault timer. If there is a continuous fault for the fault-timer duration, the MAX8798 sets the fault latch, turning off the main step-up regulator and the linear regulator, disabling the switch-control block and the operational amplifier. Once the fault condition is removed, cycle the input voltage to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

The MAX8798 monitors BOOST for undervoltage and overvoltage conditions. If the BOOST voltage is below 1.4V (typ) or above 19V (typ), the MAX8798 disables the gate driver of the step-up regulator and prevents the internal MOSFET from switching. The BOOST undervoltage and overvoltage conditions do not set the fault latch.

Operational Amplifier

The MAX8798 has an operational amplifier that is typically used to drive the LCD backplane (VCOM) or the gamma-correction-divider string. The operational amplifier features ±150mA output short-circuit current, 40V/µs slew rate, and 20MHz bandwidth. While the op amp is a rail-to-rail input and output design, its accuracy is significantly degraded for input voltages within 1V of its supply rails (BOOST and BGND).

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately ±150mA if the output is directly shorted to BOOST or to AGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal-fault latch, shutting off the main step-up regulator, the linear regulator, the switch-control block, and the operational amplifier. Those portions of the device remain inactive until the input voltage is cycled.

Driving Pure Capacitive Loads

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction-divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between VCOM and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω and the typical value of the capacitor is 10pF.

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

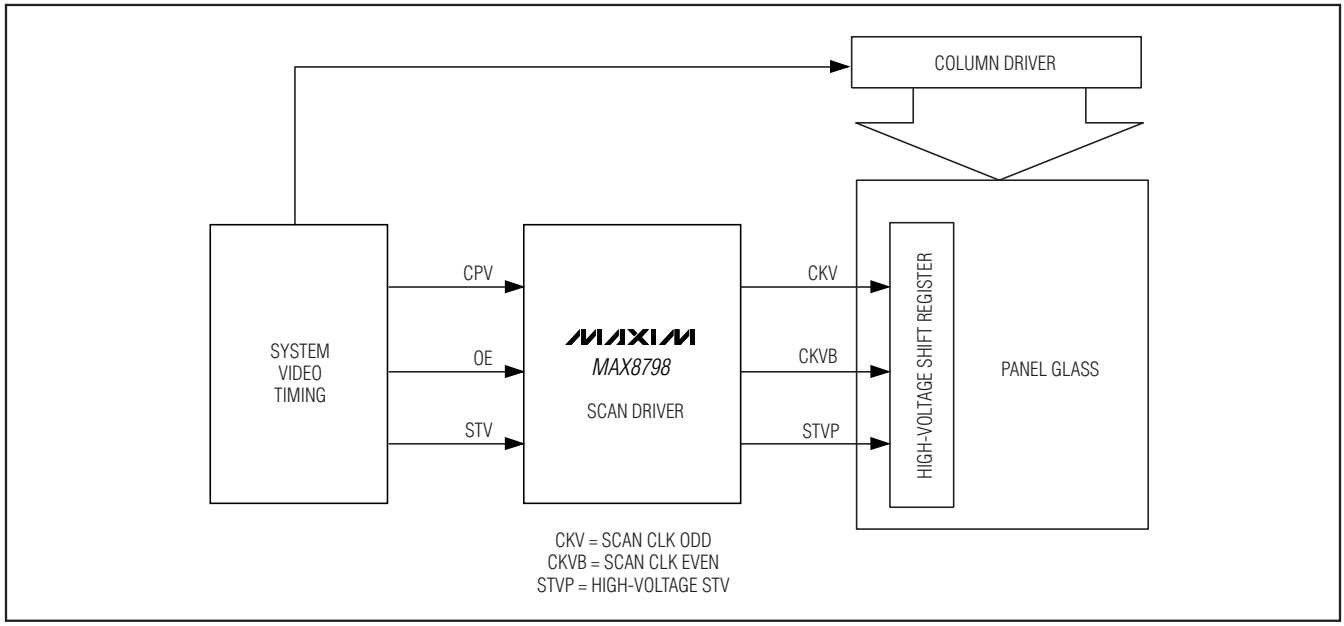


Figure 5. Scan Driver System Diagram

High-Voltage Level-Shifting Scan Driver

The MAX8798 includes a 3-channel high-voltage (60V) level-shifting scan driver, which includes logic functions necessary to drive row driver functions on the panel glass (Figure 5). The driver outputs (CKV, CKVB, STVP) swing between their power-supply rails (GON and GOFF) according to the input logic levels on the block's inputs (STV, CPV, OE, and OECON) and the internal logic of the block (Tables 3, 4). STV is the vertical sync signal. CPV is the horizontal sync signal. OE is the output enable signal. OECON is a timing signal derived from OE that blanks OE if it stays high too long. These signals have CMOS input logic levels set by the IN supply voltage. CKV and CKVB are complementary scan clock outputs. STVP is the output scan start signal. These output signals swing from GON to GOFF, which have a maximum range of +35V and -25V. Their 10Ω (typ) output impedance enables them to swiftly drive capacitive loads. The complementary CKV and CKVB outputs feature power-saving, charge-sharing inputs (CKVCS, CKVBCS) that can be used to save power by shorting each output to its complement during transitions, making a portion of the transition "lossless."

Table 3. STVP Logic

SIGNAL	LOGIC STATE			
STV	H	H	H	L
OECON	X	X	X	X
CPV	L	H	X	X
OE	L	X	H	X
STVP	H	Hi-Z	Hi-Z	L

X = *Don't care.*

Table 4. CKV, CKVB Logic

SIGNAL	LOGIC STATE							
STV	H	H	H	L	L	L	L	L
OECON	X	X	X	L	L	L	H	H
CPV	L	H	X	L	—	X	L	—
OE	L	X	H	L	X	—	X	X
CKV	L	H	H	CS	Toggle	Toggle	CS	Toggle
CKVB	H	L	L	CS	Toggle	Toggle	CS	Toggle

X = *Don't care. CS = Charge share state.*

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GOFF Rapid Discharge Function (DISH Input)

The DISH input controls a switch between GOFF and PGND. When DISH is pulled below ground by at least 1V, GOFF is rapidly discharged to GND. Typically, DISH is capacitively coupled to IN so that if IN falls suddenly, GOFF is discharged to blank the display (Figure 3).

VCOM Calibrator

The VCOM calibrator is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. OUT attaches to the external resistive voltage-divider at POS and sinks a programmable current (I_{OUT}), which sets the VCOM level (Figure 6). An internal 7-bit DAC controls the sink current and allows the user to increase or decrease the VCOM level. The DAC is ratiometrically relative to V_{BOOST} and is monotonic over all operating conditions. The user can store the DAC setting in an internal EEPROM. On power-up, the EEPROM presets the DAC to the last stored setting. The 2-wire I^2C interface between the system controller and the programming circuit adjusts the DAC and programs the EEPROM when WPN is high.

The resistive voltage-divider and the BOOST supply set the maximum value of VCOM. OUT sinks current from the voltage-divider to reduce the POS voltage level and VCOM output. The external resistor at SET (R_{SET}) sets the full-scale sink current and the minimum value of VCOM.

The GON input provides the high voltage required to program the EEPROM. To allow programming, GON is connected to the TFT LCD VGON supply. VGON should be between 16.1V and 35V. EEPROM programming is disabled when GON is below 15.5V (typ). Bypass GON to GND or BOOST (which is bypassed to GND) with a 0.1µF or greater capacitor.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection, which shuts down the step-up regulator, switch control block, operational amplifier, and the internal linear regulator, allowing the device to cool down. Once the device cools down by approximately 15°C, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

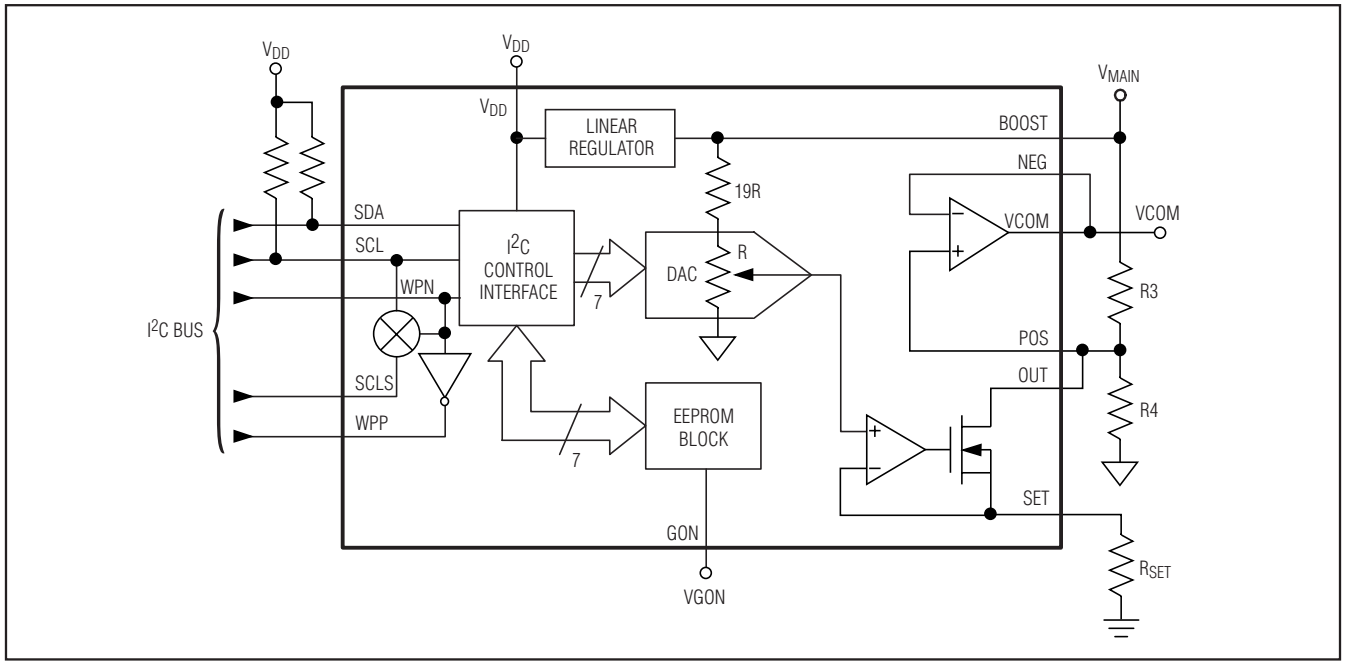

Figure 6. VCOM Calibrator Functional Diagram

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Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 2, the LCD's gate-on and gate-off supply voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance and current calculations. The effective maximum output current, $I_{MAIN(EFF)}$ becomes the sum of the maximum load current of the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{NEG} \times I_{NEG} + (n_{POS} + 1) \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, n_{NEG} is the number of negative charge-pump stages, n_{POS} is the number of positive charge-pump stages, I_{NEG} is the negative charge-pump output current, and I_{POS} is the positive charge-pump output current, assuming the initial pump source for I_{POS} is V_{MAIN}.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX8798's LX current limit (I_{LIM}) should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering Figure 2, the maximum load current ($I_{MAIN(MAX)}$) is 300mA, with an 8V output and a typical input voltage of 3.3V. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 300mA + 2 \times 20mA + (2 + 1) \times 20mA = 400mA$$

Choosing an LIR of 0.5 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{3.3V}{8V}\right)^2 \left(\frac{8V - 3.3V}{0.4A \times 1.2MHz}\right)\left(\frac{0.85}{0.5}\right) \approx 2.8\mu H$$

A 2.6µH inductor is chosen. Then, using the circuit's minimum input voltage (3.0V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.4A \times 8V}{3V \times 0.8} \approx 1.33A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{3V \times (8V - 3V)}{2.6\mu H \times 8V \times 1.2MHz} \approx 0.6A$$

$$I_{PEAK} = 1.33A + \frac{0.6A}{2} = 1.53A$$

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in Figure 2 because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in Figure 2. Ensure a low noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (seen in Figure 2).

Rectifier Diode

The MAX8798's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output Voltage Selection

The output voltage of the main step-up regulator is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 2). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{REF}} - 1\right)$$

where V_{REF}, the step-up regulator's feedback set point, is 1.235V (typ). Place R1 and R2 close to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{1000 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

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Setting the VCOM Adjustment Range

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{SET} sets the full-scale sink current, I_{OUT}, which determines the minimum value of the VCOM adjustment range. Large R_{SET} values increase resolution, but decrease the VCOM adjustment range. Calculate R3, R4, and R_{SET} using the following procedure:

1) Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the V_{MAIN} supply voltage.
2) Select R3 between 10kΩ and 500kΩ based on the acceptable power loss from the V_{MAIN} supply rail connected to BOOST.
3) Calculate R4:

$$R4 \cong \frac{V_{MAX}}{(V_{BOOST} - V_{MAX})} \times R3$$

4) Calculate R_{SET}:

$$R_{SET} = \frac{V_{MAX}}{20 \times (V_{MAX} - V_{MIN})} \times R3$$

5) Verify that I_{SET} does not exceed 120µA:

$$I_{SET} = \frac{V_{BOOST}}{20 \times R_{SET}}$$

6) If I_{SET} exceeds 120µA, return to step 2 and choose a larger value for R1.
7) The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

V_{MAX} = 4V, V_{MIN} = 2.4V, V_{BOOST} = 8V

If R3 = 200kΩ, then R4 = 200kΩ and R_{SET} = 24.9kΩ.

Resolution = 12.5mV

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX8798, with its exposed backside paddle soldered to 1in² of PCB copper and a large internal ground plane layer, can dissipate about 2.18W into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifiers.

The MAX8798's largest on-chip power dissipation occurs in the step-up switch, the VCOM amplifier, and the high-voltage scan-driver outputs.

Step-Up Regulator

The largest portions of the power dissipated by the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator with 3.3V input and 300mA output has about 85% efficiency, about 5% of the power is lost in the internal MOSFET, about 3% in the inductor, and about 5% in the output diode. The remaining few percent are distributed among the input and output capacitors and the PCB traces. If the input power is about 3W, the power lost in the internal MOSFET is about 150mW.

Operational Amplifier

The power dissipated in the operational amplifier depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{VCOM\_SOURCE} \times (V_{BOOST} - V_{VCOM})$$

$$PD_{SINK} = I_{VCOM\_SINK} \times V_{VCOM}$$

where I_{VCOM_SOURCE} is the output current sourced by the operational amplifier, and I_{VCOM_SINK} is the output current that the operational amplifier sinks.

In a typical case where the supply voltage is 8V and the output voltage is 4V with an output source current of 30mA, the power dissipated is 120mW.

Scan-Driver Outputs

The power dissipated by the scan-driver outputs (CKV, CKVB, and STVP) depends on the scan frequency, the capacitive load, and the difference between the GON and GOFF supply voltages:

$$PD_{SCAN} = 3 \times f_{SCAN} \times C_{PANEL} \times (V_{GON} - V_{GOFF})^2$$

If the scan frequency is 50kHz, the load of the three outputs is 5nF, and the supply voltage difference is 30V, then the power dissipated is 675mW.

VCOM Calibrator Interface

The MAX8798 is a slave-only device with an I²C address of 9Eh. The 2-wire I²C-bus-like serial interface (pins SCL and SDA) is designed to attach to a 1.8V to 4V I²C bus. Connect both SCL and SDA lines to the V_{DD} supply through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time in the *Electrical Characteristics* table, and C_{BUS} is the total capacitance on the bus.

The MAX8798 uses a nonstandard I²C interface protocol with mostly standard voltage and timing parameters, as defined in the following subsections.

Bus Free

Both data and clock lines remain HIGH. Data transfers can be initiated only when the bus is not busy (Figure 7).

START Condition (S)

Starting from an idle bus state (both SDA and SCL are high), a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition from a master device on the bus.

STOP Condition (P)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition from the master device.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. The master generates one clock pulse per bit of data during write operations and the slave device outputs 1 data bit per clock pulse during read operations. Each data transfer is initiated with a START condition and terminated with a STOP condition. Two bytes are transferred between the START and STOP conditions.

Slave Address

After generating a START condition, the bus master transmits the slave address consisting of the 7-bit device code (0b1001110 or 9Eh) for the MAX8798 (Figure 8). For a read operation the 8th bit is 1 and for write operations it is 0. The MAX8798 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if it recognizes its slave address and it is not busy programming the EEPROM.

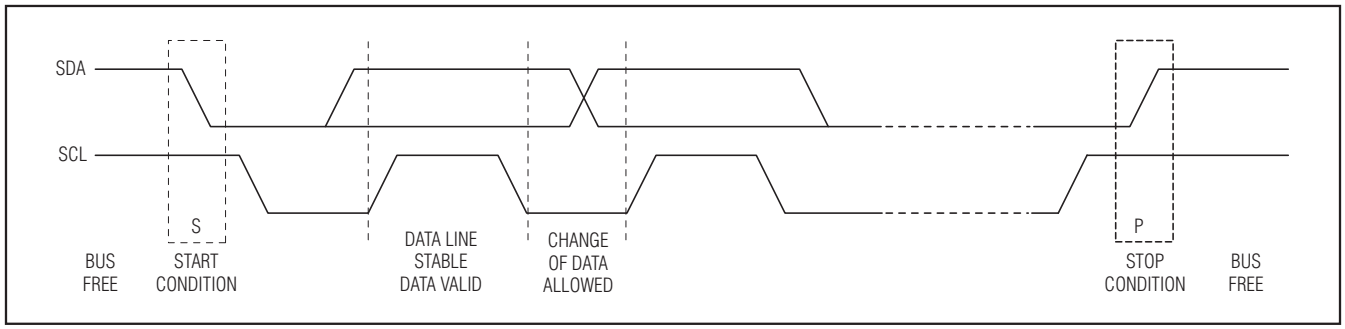

Figure 7. I²C Bus Start, Stop, and Data Change Conditions

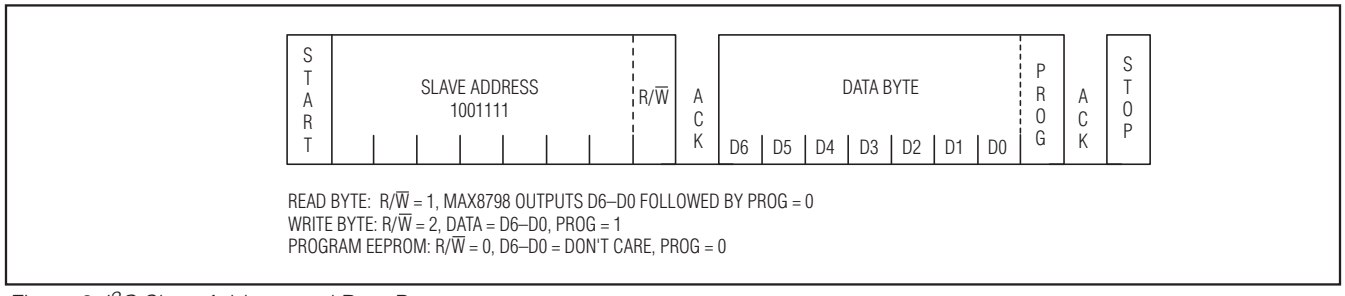

Figure 8. I²C Slave Address and Data Byte

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Data Byte

The data byte follows successful transmission of the MAX8798's slave address (Figure 8). For a read operation, the MAX8798 outputs the 7 bits corresponding to the current DAC setting followed by a 0 bit. For a write operation, the bus master must provide the 7-bit data corresponding to the desired DAC setting followed by a 1 bit. To program the IC's EEPROM, the master must make the last bit a zero, in which case the other 7 bits of data are ignored. For programming, GON must exceed its programming threshold. Otherwise, programming does not occur and the MAX8798 does not acknowledge the programming command.

DAC Values

Table 5 lists the DAC values and the corresponding I_{SET}, V_{SET}, and V_{OUT} values.

Table 5. DAC Settings

7-BIT DATA BYTE	I_{SET}	V_{SET} (V)	V_{OUT} (V)
0000000	$I_{SET(MAX)}$	$V_{SET(MAX)}$	V_{MIN}
0000001	$I_{SET(MAX)}$ - 1-LSB	$V_{SET(MAX)}$ - 1-LSB	V_{MIN} + 1-LSB
. . .	. . .	. . .	. . .
1111110	$I_{SET(MIN)}$ + 1-LSB	$V_{SET(MIN)}$ + 1-LSB	V_{MAX} - 1-LSB
1111111	$I_{SET(MIN)}$	$V_{SET(MIN)}$	V_{MAX}

Acknowledge/Polling

The MAX8798, when addressed, generates an acknowledge pulse after the reception of each byte (Figure 9). The master device must generate an extra clock pulse, which is associated with this acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. The master signals an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave leaves the data line HIGH to enable the master to generate the STOP condition.

The MAX8798 does not generate an acknowledge while an internal programming cycle is in progress. Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a START condition followed by the device address byte. Only if the internal write cycle has completed does the MAX8798 respond with an acknowledge pulse, allowing the read or write sequence to continue.

The MAX8798 does not acknowledge a command to program the EEPROM if V_{GON} is not high enough to properly program the device. Also, a program command must be preceded by a write command. The IC does not acknowledge a program command or program the EEPROM unless the DAC data has been modified since the most recent program command.

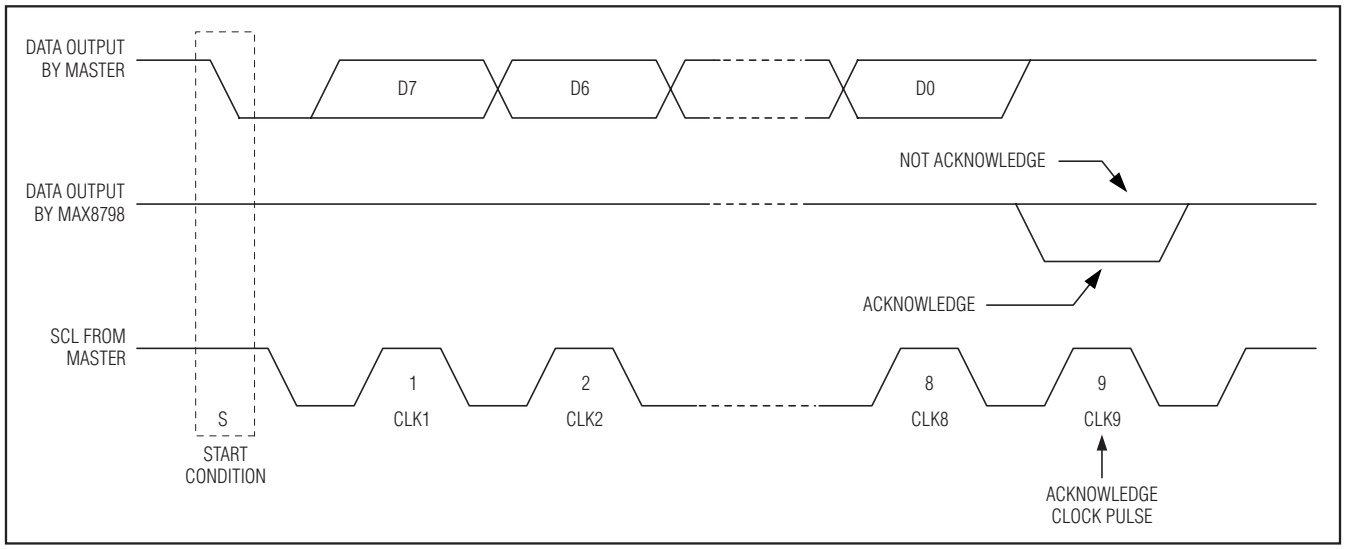


Figure 9. I^2C Bus Acknowledge

PCB Layout and Grounding

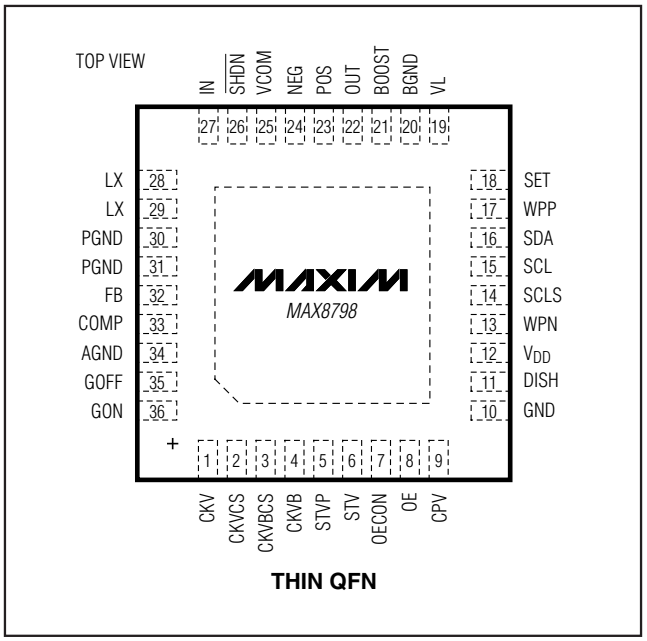
Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier-divider ground connections, the COMP capacitor ground connection, the BOOST and VL bypass capacitor ground connections, and the device's exposed backside paddle. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside paddle. Make no other connections between these separate ground planes.
- Place the feedback-voltage-divider resistors as close as possible to the feedback pin. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX or the switching nodes in the charge pumps.
- Place the IN pin and VL pin bypass capacitors as close as possible to the device. The ground connections of the IN and VL bypass capacitors should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as shield if necessary.

Refer to the MAX8798 evaluation kit for an example of proper board layout.

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Pin Configuration



THIN QFN

Chip Information

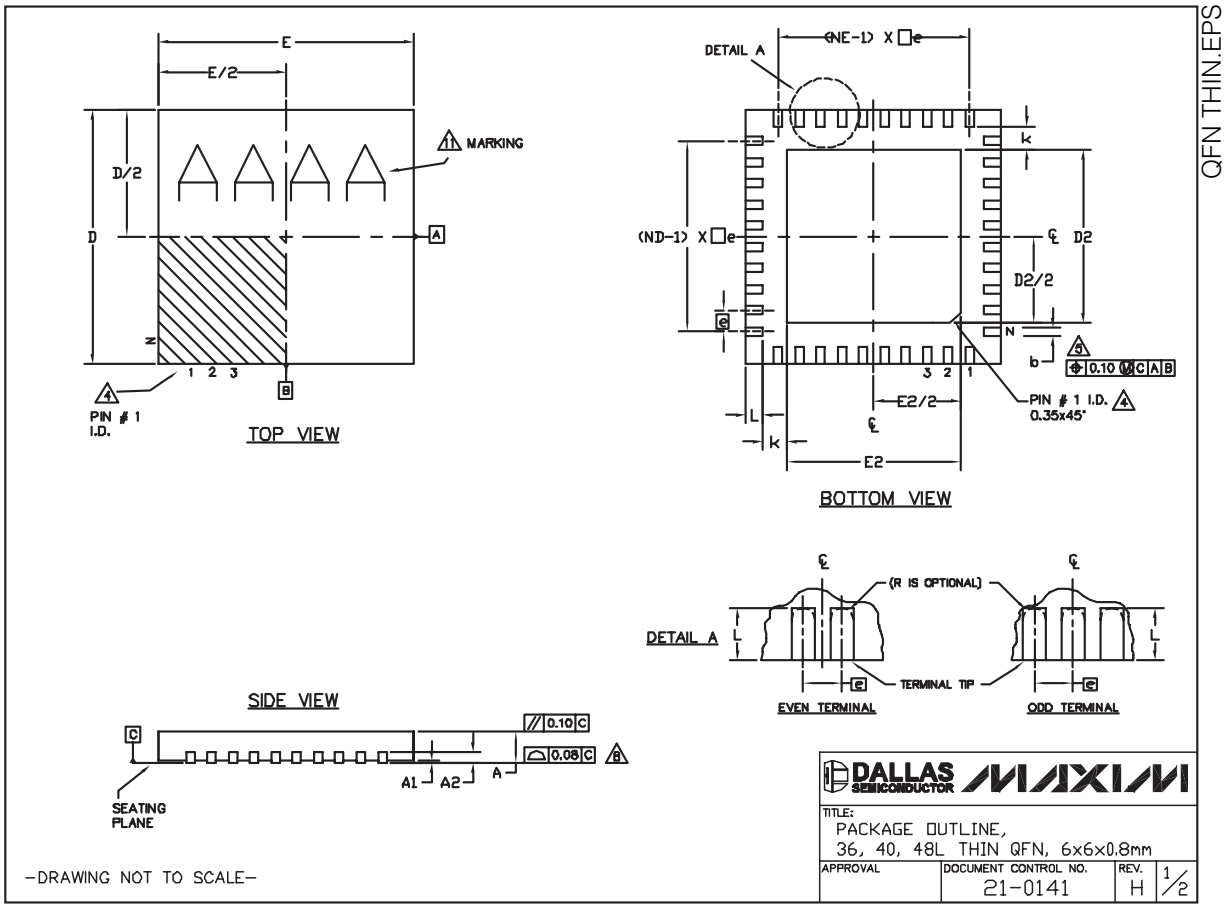
TRANSISTOR COUNT: 15,227

PROCESS: BiCMOS

Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Internal-Switch Boost Regulator with Integrated 3-Channel Scan Driver for TFT LCDs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	H	2/2