MAXIM

Temperature-Controlled, NV, I2C, Logarithmic Resistor
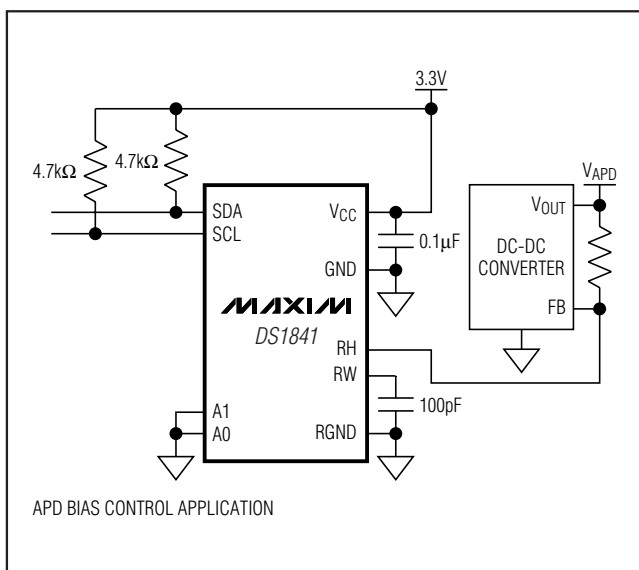
DS1841

General Description

The DS1841 is a 7-bit, logarithmic, nonvolatile (NV) digital resistor that features an on-chip temperature sensor and associated analog-to-digital converter (ADC). The integrated temperature sensor indexes a 72-byte NV lookup table (LUT) encompassing a temperature range from -40°C to +100°C. The LUT output can drive the resistor directly or be added to an NV initial-value register (IVR) to drive the resistor. This flexible LUT-based architecture allows the DS1841 to provide a temperature-compensated resistor output with arbitrary slope. Programming is accomplished by an I2C-compatible interface, which can operate at speeds of up to 400kHz.

Applications

Optical Transceivers

Linear and Nonlinear Compensation

Instrumentation and Industrial Controls

Mechanical Potentiometer Replacement

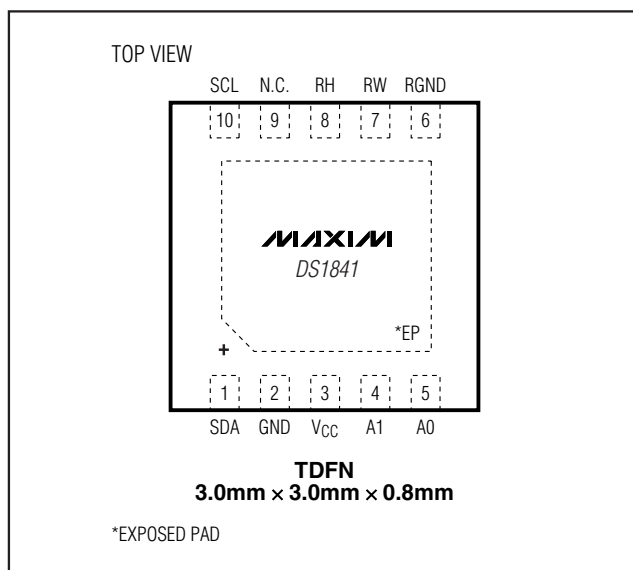*Registers and Modes are capitalized for clarity.*

Features

♦ **22kΩ to 3.7kΩ Adjustable Logarithmic Resistor with a 3.6kΩ Fixed Resistor**

♦ **128 Wiper Tap Points**

♦ **On-Chip Temperature Sensor and ADC**

♦ **72-Byte Lookup Table (LUT)**

♦ **I2C-Compatible Serial Interface**

♦ **Address Pins Allow Up to Four DS1841s to Share the Same I2C Bus**

♦ **Digital Supply of 2.7V to 5.5V**

♦ **-40°C to +100°C Operating Range**

♦ **3mm x 3mm, 10-Pin TDFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1841T+	-40°C to +100°C	10 TDFN
DS1841T+T&R	-40°C to +100°C	10 TDFN

+Denotes a lead-free package.
T&R = Tape and reel.

Typical Operating Circuit

APD BIAS CONTROL APPLICATION

Pin Configuration

TDFN
3.0mm × 3.0mm × 0.8mm

*EXPOSED PAD

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on SDA, SCL, and
   V_{CC} Relative to GND ....-0.5V to +6.0V
Voltage Range on RH, RW, A0, and
   A1 Relative to GND ....-0.5V to (V_{CC} + 0.5V)
Operating Temperature Range ....-40°C to +100°C

Programming Temperature Range ....0°C to +70°C
Storage Temperature Range ....-55°C to +125°C
Soldering Temperature ....See IPC/JEDEC J-STD-020
RW Current..3mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +100°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
Input Logic 1 (SCL, SDA, A0, A1)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, A1)	V_{IL}		-0.3		0.3 x V_{CC}	V
Resistor Inputs (RW, RH)	V_{RES}		-0.3		V_{CC} + 0.5	V
Wiper Current	I_{WIPER}				2	mA

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (SDA, SCL, A0, A1)	I_L		-1		+1	µA
V_{CC} Supply Current	I_{CC2}	(Note 2)			350	µA
Low-Level Output Voltage (SDA)	V_{OL}	3mA sink current	0		0.4	V
I/O Capacitance	$C_{I/O}$			5	10	pF
Power-On Recall Voltage	V_{POR}	(Note 3)	1.6		2.6	V
Power-Up Recall Delay	t_D	(Note 4)			5	ms
Series Resistance	R_S			3.6		kΩ
Minimum Resistance (GND to RW)	R_{MIN}	(Note 5)		370		Ω
End-to-End Resistance (GND to RW)	R_{TOTAL}			22		kΩ
R_{TOTAL} Tolerance		T_A= +25°C	-20		+20	%
Temp Coefficient	T_{CV}	WR set to 40h		±250		ppm/°C
RH, RW Capacitance	C_{POT}			10		pF

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TEMPERATURE SENSOR CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Error					±5	°C
Update Rate (Temperature and Supply Conversion Time)	t_{FRAME}			16		ms

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Resolution	LSB	Full-scale voltage of 6.5536V		25.6		mV
Input/Supply Accuracy	A_{CC}	At factory setting		0.25	1.0	% FS (Full Scale)
Update Rate (Temperature and Supply Conversion Time)	t_{FRAME}			16		ms

I2C AC ELECTRICAL CHARACTERISTICS (See Figure 3)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Conditions	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 7)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 7)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 7)			400	pF

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I²C AC ELECTRICAL CHARACTERISTICS (See Figure 3) (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Time	t_W	(Note 8)		10	20	ms
A0, A1 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0, A1 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
Input Capacitance on A0, A1, SDA, or SCL	C_I			5	10	pF
Startup Time	t_{ST}				2	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		T_A = +85°C	50,000			Writes
EEPROM Write Cycles		T_A = +25°C (Note 9)	200,000			Writes

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.

Note 2: I_{CC} is specified with the following conditions: SCL and SDA = V_{CC}, RW and RH floating with Update Mode bit = 1.

Note 3: This is the minimum V_{CC} voltage that causes NV memory to be recalled.

Note 4: This is the time from V_{CC} > V_{POR} until initial memory recall is complete.

Note 5: Guaranteed by design.

Note 6: I²C interface timing shown is for Fast-Mode (400kHz) operation. This device is also backward-compatible with I²C-Standard Mode timing.

Note 7: C_B—total capacitance of one bus line in picofarads.

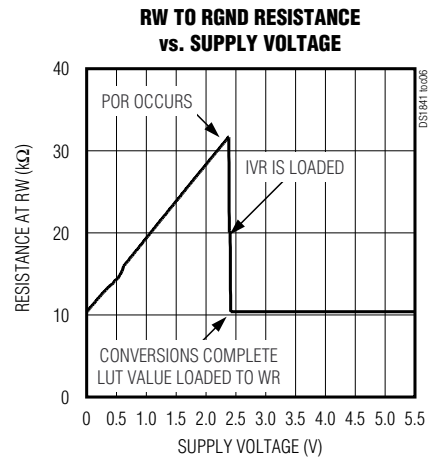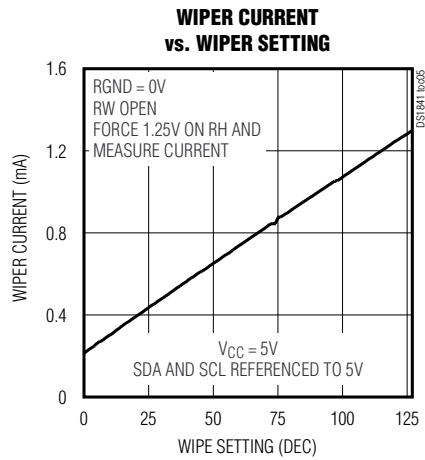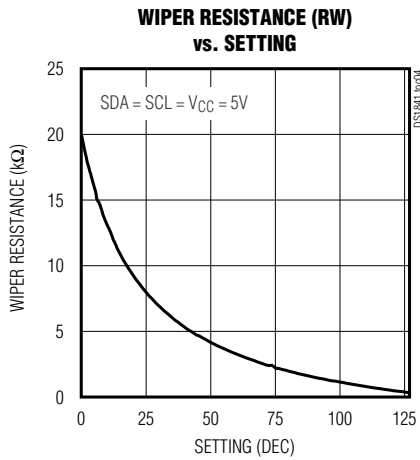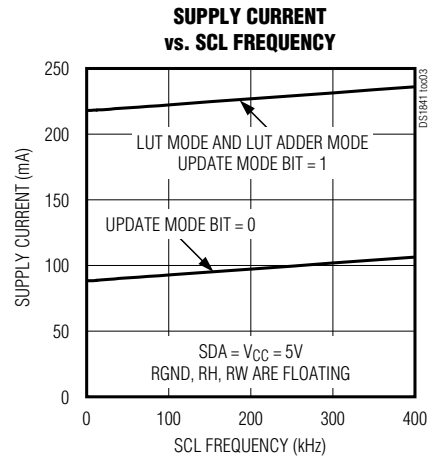**Note 8:** EEPROM write time begins after a STOP condition occurs.

Note 9: Guaranteed by characterization.

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Typical Operating Characteristics

(V_{CC} = +2.7V to +5.5V, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE

SUPPLY CURRENT vs. TEMPERATURE

SUPPLY CURRENT vs. SCL FREQUENCY

WIPER RESISTANCE (RW) vs. SETTING

WIPER CURRENT vs. WIPER SETTING

RW TO RGND RESISTANCE vs. SUPPLY VOLTAGE
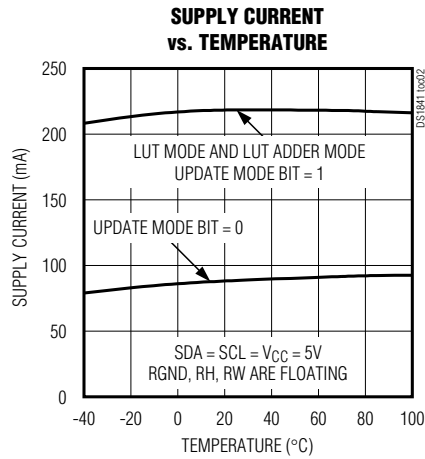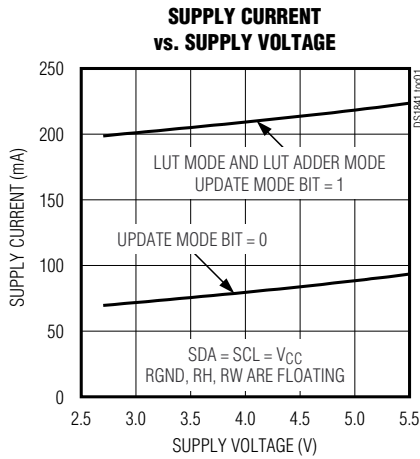
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PIN	NAME	FUNCTION
1	SDA	I^{2}C Serial Data. Input/output for I^{2}C data.
2	GND	Ground
3	V$_{CC}$	Power Supply
4	A1	Address Select Inputs. Determines I^{2}C slave address. Device address is 01010A$_1$A$_0$X (see the
5	A0	*Slave Address Byte and Address Pins* sections for more details).
6	RGND	Low Terminal of Resistor. **Must be connected to GND.**
7	RW	Wiper Terminal
8	RH	Terminal with Fixed Resistor Added in Series with Digital Resistor
9	N.C.	No Connection
10	SCL	I^{2}C Serial Clock. Input for I^{2}C clock.
—	EP	Exposed Paddle. Must be connected to ground.

Detailed Description

The DS1841 operates in one of two modes: LUT Mode and LUT Adder Mode. In LUT Mode and LUT Adder Mode, the resistor's wiper position is controlled as a function of the temperature measured by the DS1841's internal temperature sensor. The difference between the two LUT modes is the way the resistor's wiper position is calculated. Detailed descriptions of these two modes, as well as additional features of the DS1841, are discussed in subsequent sections.

Digital Resistor Description

The DS1841's resistor consists of 128 resistive steps between RW and RGND with a series resistor, R$_S$, between RH and RW. The wiper position and the output seen on RW are decoded based on the value in the wiper register (WR). The step size of each position is optimized to produce a linear response when used in the feedback network of a DC-DC converter.

Mode Selection

The DS1841 mode of operation is determined by the Update Mode bit (Control Register 1, address 03h, bit 0) and the Adder Mode bit (Control Register 1, address 03h, bit 1). Table 1 illustrates how the two control bits are used to select the operating mode. When shipped from the factory, the DS1841 is programmed with the Update Mode and Adder Mode bits set to 1, hence configuring the DS1841 in LUT Adder Mode. See Appendix A for a detailed table of the control logic bit functions.

Table 1. Operating Modes

UPDATE MODE BIT	ADDER MODE BIT	MODE
1	0	LUT Mode
1	1	LUT Adder Mode (Default)

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LUT Adder Mode (Default)

LUT Adder Mode is selected by setting the Update Mode bit to 1 and the Adder Mode bit to 1. This mode operates similar to LUT Mode with one major difference (see the *LUT Mode and LUT Adder Mode Block Diagram*). The WR is loaded with the sum of the values of LUTVAL (the value pointed to by the address stored in LUTAR) and IVR. Furthermore, in this mode, the values programmed into the LUT are signed two's complement. This allows convenient positive or negative offsetting of the nominal IVR value. WR resistance values clamp at 00h and 7Fh (the MSB is ignored).

LUT Mode

LUT Mode is selected by setting the Update Mode bit (Control Register 1, address 03h, bit 0) to a 1 and the Adder Mode bit (Control Register 1, address 03h, bit 1) to a 0. An overview of the DS1841 in this mode is illustrated in the *LUT Mode and LUT Adder Mode Block Diagram*. The memory map for the LUT Mode and the LUT Adder Mode is shown in Table 2. The major difference between the two LUT modes is whether the value

in the IVR is added to the values stored in the LUT. The dashed line/arrow shown in the *LUT Drive Mode Block Diagram* is not active in LUT Mode. When in LUT Mode, on power-up the IVR value is recalled into the WR. This value remains there until completion of the first temperature conversion following power-up. The temperature is measured every t_{FRAME}. The temperature value is used to calculate an index that points to the corresponding value in the LUT. This index is referred to as the LUT Address Register (LUTAR) and is located at address 08h. The value stored in the LUT at the location pointed to by LUTAR is called LUTVAL, and this value is stored as the WR value (WR) at address 09h when Update Mode bit = 1. The process then repeats itself, continuously updating the wiper setting in a closed-loop fashion. In this mode the 72-byte LUT is populated with wiper settings for each two-degree temperature window. Valid wiper settings are 00h to 7Fh (the MSB is ignored). Table 3 shows the memory addresses of the LUT as well as the corresponding temperature range for each byte in the LUT.

Table 2. LUT Mode and LUT Adder Mode Memory Map

REGISTER	NAME	ADDRESS (HEX)	VOLATILE/NV	FACTORY/POWER-UP DEFAULT
IVR	Initial Value Register	00h	NV (Shadowed)	00h
CR0	Control Register 0	02h	Volatile	00h
CR1	Control Register 1	03h	NV (Shadowed)	03h
LUTAR	LUT Address Register	08h	Volatile	00h
WR	LUT Value Register	09h*	Volatile	00h
CR2	Control Register 2	0Ah	Volatile	00h
TEMP	Temperature Result	0Ch	Volatile (Read Only)	N/A
VOLTAGE	Supply Voltage Result	0Eh	Volatile	N/A
LUT	Temperature Lookup Registers	80h–C7h	NV	00h

*In LUT Mode and LUT Adder Mode, WR is accessed through memory address 09h, while IVR remains at memory address 00h.

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___LUT Mode and LUT Adder Mode Block Diagram (Update Mode Bit = 1)

*NOTE THAT WHEN IN LUT OR LUT ADDER MODE, WR IS ACCESSED THROUGH 09h WHILE IVR REMAINS AT 00h.
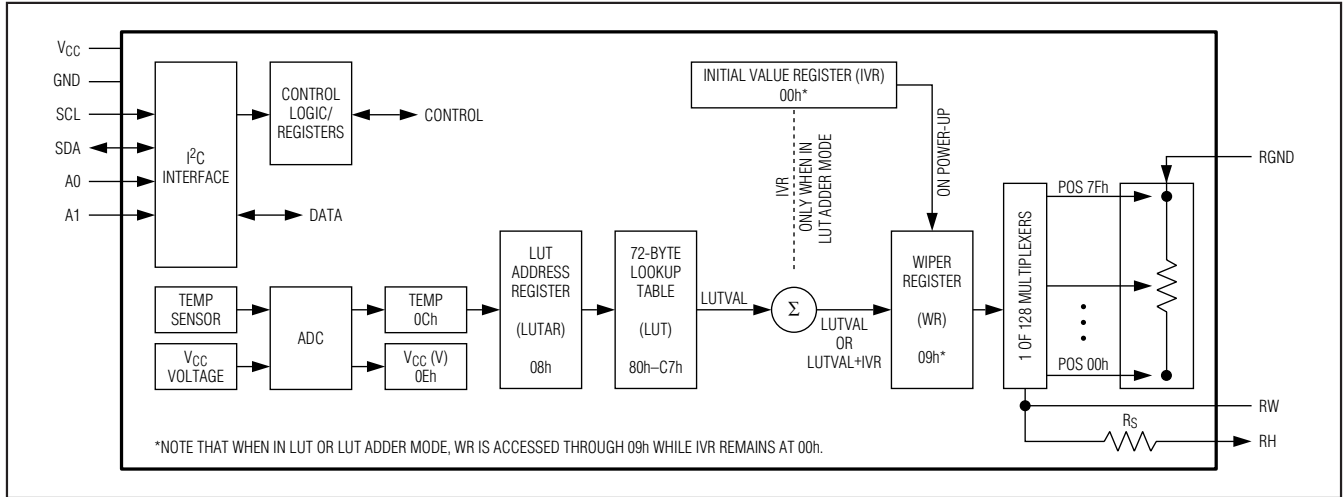
Temperature Conversion and Supply Voltage Monitoring

Temperature Conversion

The DS1841 features an internal 8-bit temperature sensor that can drive the LUT and provide a measurement of the ambient temperature over I²C by reading the value stored in address 0Ch. The sensor is functional over the entire operating temperature range and is stored in signed two's complement format with a resolution of 1°C/bit. See Table 2, Register 0Ch description for the temperature sensor's bit weights. To calculate the temperature, treat the two's complement binary value as an unsigned binary number, then convert it to decimal. If the result is greater than or equal to 128, subtract 256 from the result.

LUT

The DS1841 monitors the internal temperature by repeatedly polling the sensor's result with update rate tFRAME. During each cycle, the DS1841 reads the internal temperature, and, based on that temperature, points to the corresponding LUT address. Every two degrees of temperature will convert into one temperature address slot. See Table 3 for a list of temperatures and their corresponding LUT addresses.

The LUT features one-degree hysteresis to prevent chattering if the measured temperature falls on the boundary between two windows (see Figure 1).

Table 3. LUT Registers and Temperature Ranges

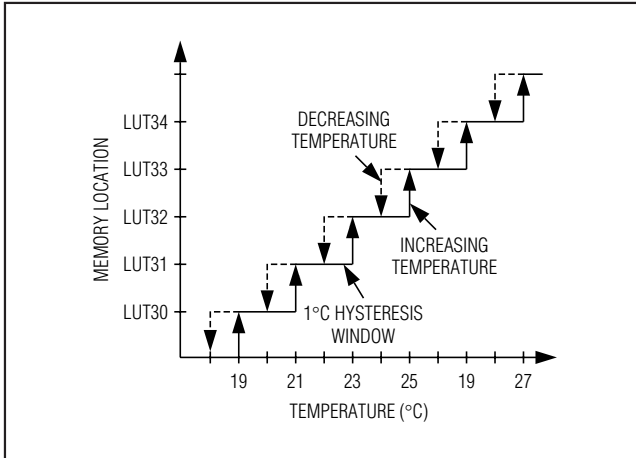| TEMPERATURE (°C)	TEMPERATURE VALUE FOR GIVEN TEMPERATURE (HEX)	CORRESPONDING LUT ADDRESS (HEX)
-40 or less	D8	80
-39 to -38	D9 to DA	81
-37 to -36	DB to DC	82
-35 to -34	DD to DE	83
—	—	—
+95 to +96	5F to 60	C4
+97 to +98	61 to 62	C5
+99 to +100	63 to 64	C6
+101 or more	65	C7

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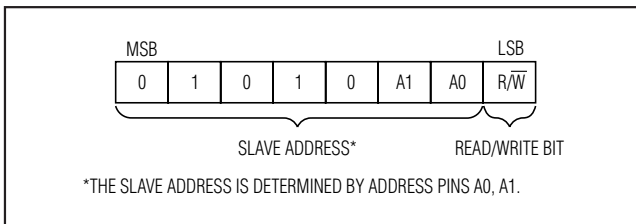
Figure 1. LUT Hysteresis

Figure 2. Slave Address Byte

Supply Voltage Monitoring

The DS1841 also features an internal 8-bit supply voltage (V_{CC}) monitor. A value of the supply voltage measurement can be read over I2C at the address 0Eh.

To calculate the supply voltage, simply convert the hexadecimal result into decimal and then multiply it by the LSB as shown in *the Analog Voltage Monitoring Characteristics* electrical table.

Supply Current (I_{CC})

The DS1841 has two supply current levels of power supply consumption. First, active current during I2C communications while in the LUT-Driven Mode is the "worst case" supply current, I_{CC}. All functionality including I2C communication is operating simultaneously. Second, active current without I2C while in the LUT-Driven Mode is quantified by the supply current, I_{CC2}. SDA and SCL are held statically in the high logic level.

Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 2). The DS1841's slave address is determined by the state of the A0 and A1 address pins. These pins allow up to four devices to reside on the same I2C bus. Address pins tied to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a 1 in the corresponding bit positions. For example, the DS1841's slave address byte is 50h when A0 and A1 pins are grounded. I2C communication is described in detail in the *I2C Serial Interface Description* section.

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Memory Description

The DS1841's internal memory consists of both volatile and NV registers that are organized into eight byte rows. Three control registers as well as specialized data registers are used to control the wiper and drive the LUT.

Register Descriptions
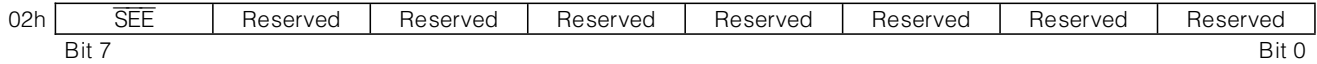
Register 00h: Initial Value Register (IVR)

FACTORY DEFAULT (IVR) 00h
MEMORY TYPE   NV
MEMORY TYPE   Volatile

00h	IVR
Bit 7	Bit 0
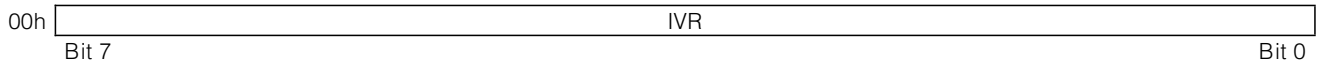
If $\overline{SEE}$ bit = 0, an I²C READ retrieves the IVR value and an I²C WRITE sets the wiper position in volatile memory and updates IVR in NV memory with this new value. If $\overline{SEE}$ bit = 1, an I²C READ retrieves the WR value and an I²C WRITE sets the wiper position (volatile) and the IVR value is not modified. During power-up, IVR's value is used to set the wiper position.

Register 02h: Control Register 0 (CR0)

FACTORY DEFAULT   00h
MEMORY TYPE   Volatile

02h	$\overline{SEE}$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit 7								Bit 0

Bit 7	**$\overline{SEE}$** Controls IVR and WR functionality, as well as the memory type for Control Register 1. **0** = (Default) Issuing an I²C READ of the value in address 00h retrieves the IVR value. Issuing an I²C WRITE to address 00h sets both the wiper's position (volatile) and the IVR value (nonvolatile) to the same value. Writes to Control Register 1 (03h) are stored in shadowed SRAM and EEPROM. **1** = Issuing an I²C READ of the value in address 00h retrieves the WR value. Issuing an I²C WRITE to address 00h only sets the wiper's position (volatile). The IVR value is not modified. Writes to Control Register 1 (03h) are stored in shadowed SRAM only.
Bits 6 to 0	Reserved.

Control Register 0 determines how the wiper position values (volatile and NV versions) are set, as well as how writes to Control Register 1 are stored.

The IVR is located at memory address 00h and is implemented as EEPROM shadowed SRAM. This register can be visualized as an SRAM byte (the WR portion) in parallel with an EEPROM byte (the IVR portion). The operation of the register is controlled by the Shadow EEPROM ($\overline{SEE}$) bit in Control Register 0, address 02h, bit 7. When the $\overline{SEE}$ bit = 0 (default), data written to memory address 00h by I²C actually gets stored in both SRAM (WR) and EEPROM (IVR). When $\overline{SEE}$ = 1, only the SRAM (WR) is written to the new value. The EEPROM byte (IVR) continues to store the last value written to it when $\overline{SEE}$ was 0. Reading memory address 00h reads the value stored in WR. The $\overline{SEE}$ bit is volatile and its power-up default state is 0.

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Register 03h: Control Register 1 (CR1)

FACTORY DEFAULT	00h
MEMORY TYPE	Shadowed NV

03h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Adder Mode	Update Mode
	Bit 7							Bit 0

Bits 7 to 2	Reserved.
Bit 1	**Adder Mode** *This bit is valid only if the Update Mode bit = 1.* **0** = (Default) The LUTVAL or IVR value is directly loaded to WR though the mux. **1** = The LUTVAL is summed with the IVR value and is directly loaded to WR though the mux.
Bit 0	**Update Mode** **0** = (Default) CR0 is enabled. During power-up the IVR value is loaded into the WR to set the wiper position. Updates to Temperature Result (0Ch) and Supply Voltage Result (0Eh) are halted. **1** = The WR is controlled directly by I²C communication though registers 08h or 09h, or the WR is controlled by the temperature-compensation/LUT circuitry. If temperature compensation is enabled, one of the 72 temperature slots is selected (by the LUTAR) and this slot value is copied into the LUTVAL, which in turn sets the WR. Updates to Temperature Result (0Ch) and Supply Voltage Result (0Eh) are enabled.

Control Register 1 controls how the wiper position is determined. The $\overline{SEE}$ bit controls whether the values of this register are stored in EEPROM or in Shadowed SRAM. On power-up, the EEPROM value is recalled to this register, regardless of the state of $\overline{SEE}$.

While the registers other than 00h through 0Ah can be read, they are not updated by the ADC as the ADC is disabled with the Update Mode bit = 0.

Register 08h: LUT Address Register (LUTAR)

FACTORY DEFAULT	00h
POR DEFAULT	00h until t_{FRAME}
MEMORY TYPE	Volatile

08h	LUTAR
Bit 7	Bit 0

The LUTAR register serves as the index pointer to choose the corresponding temperature slot in the LUT based on the internal temperature sensor result. The LUTAR can be directly read by acessing address 08h; however, to write an new value to LUTAR (to control WR manually), the LUTAR Mode bit must be set to a 1.

Register 09h: LUT Value Register (WR*)

FACTORY DEFAULT	00h
MEMORY TYPE	Volatile

09h	WR*
Bit 7	Bit 0

WR serves as an intermediate location, which is populated automatically with the results of the temperature-indexed lookup. The WR can be directly read by acessing address 09h; however to write an new value to WR (to control it manually), the wiper access control bit must be set to a 1. WR is an unsigned 7-bit value.

*WR is updated every t_{FRAME} if Update Mode bit = 1. If Update Mode bit = 0, WR holds the value stored in register 00h.

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Register 0Ah: Control Register 2 (CR2)

FACTORY DEFAULT   00h
MEMORY TYPE   Volatile

0Ah	Reserved	Reserved	Reserved	Reserved	Reserved	Wiper Access Control	LUTAR Mode	Reserved
	Bit 7							Bit 0

Bits 7 to 3	Reserved.
Bit 2	**Wiper Access Control** *This bit is valid only in LUT Mode and in LUT Adder Mode.* **0** = (Default) WR is loaded with the value from IVR summed with LUTVAL, or just the value of LUTVAL based on the state of the Adder Mode bit. **1** = The DS1841 is placed in a manual mode, allowing WR (address 09h) to be programmed using I²C commands.
Bit 1	**LUTAR Mode** *This bit is valid only in LUT Mode and in LUT Adder Mode.* **0** = (Default) The LUTAR value, located in at address 08h, is calculated following each temperature conversion that points to the corresponding location in the LUT. **1** = Automatic updates of LUTAR are disabled, allowing the LUTAR register to be programmed using I²C commands.
Bit 0	**Reserved. This bit must be set to a 0.**

Control Register 2 controls how the wiper position is determined.

Register 0Ch: Temperature Result (TEMP)

FACTORY DEFAULT   None
MEMORY TYPE   Volatile

0Ch	Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Bit 7							Bit 0

This register holds the current temperature result. It is updated every conversion time, t_{FRAME}. To calculate the temperature, treat the two's complement binary value as an unsigned binary number, then convert it to decimal. If the result is greater than or equal to 128, subtract 256 from the result. This register is only updated when the Update Mode bit = 1. When the Update Mode bit = 0, no ADC updates are made to this register.

Register 0Eh: Supply Voltage Result (VOLTAGE)

FACTORY DEFAULT   None
MEMORY TYPE   Volatile

0Eh	Supply Voltage
Bit 7	Bit 0

This register holds the current supply voltage result. It is updated every conversion time, t_{FRAME}. See the *Supply Voltage Monitoring* section. This register is only updated when the Update Mode bit = 1. When the Update Mode bit = 0, no ADC updates are made to this register.

MAXIM

Registers 80h to C7h: Temperature Lookup Register (LUT)

FACTORY DEFAULT	00h
MEMORY TYPE	NV

80h to C7h	(See Table 3 for settings.)

Bit 7   Bit 0
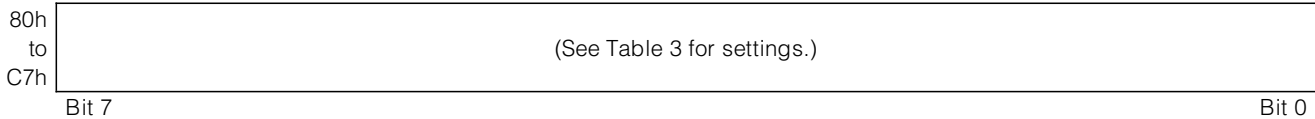
These registers at location 80h to C7h are NV and serve to temperature compensate RW over the operating temperature range of the DS1841.

The LUT entries are unsigned 8-bit values if the Adder Mode bit = 0. If the Adder Mode bit = 1, LUT entries are two's complement, signed 7-bit values.

___I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 3 and I²C AC Electrical Table for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.
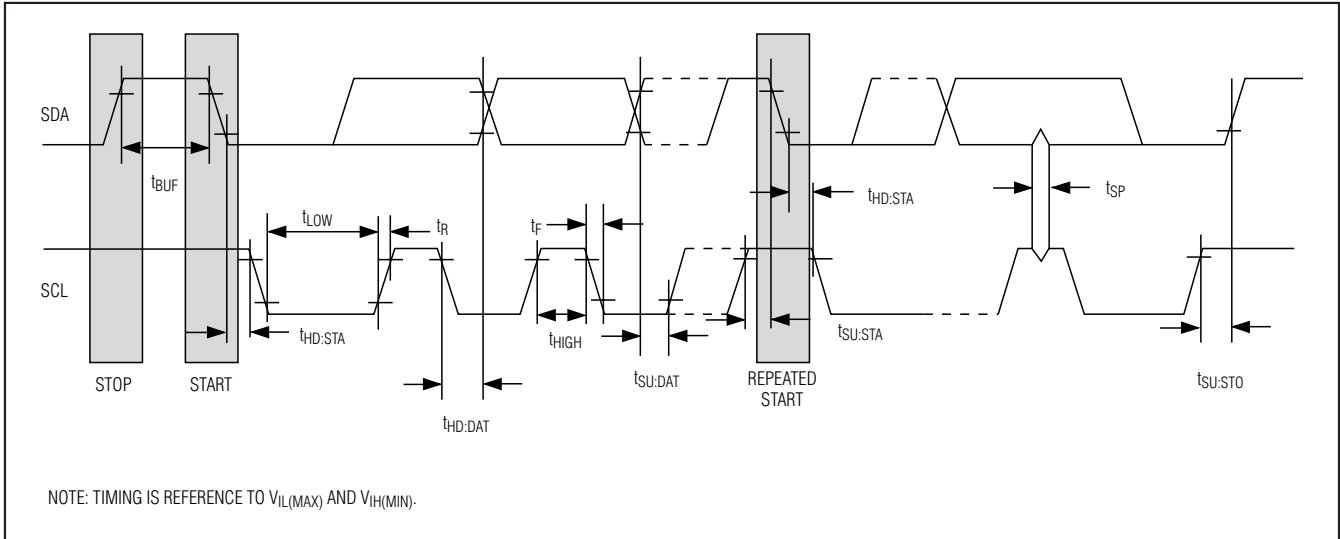
Figure 3. I2C Timing Diagram

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave address byte: Each slave on the I2C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1841's slave address is determined by the state of the A0 and A1 address pins as shown in Figure 2. Address pins tied to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a 1 in the corresponding bit positions.

When the R/$\overline{W}$ bit is 0 (such as in 50h), the master is indicating that it will write data to the slave. If R/$\overline{W}$ = 1 (51h in this case), the master is indicating that it wants to read from the slave.

If an incorrect slave address is written, the DS1841 assumes the master is communicating with another I2C device and ignores the communication until the next START condition is sent.

Memory address: During an I2C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I2C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

When writing to the DS1841, the potentiometer adjusts to the new setting once it has acknowledged the new data that is being written, and the EEPROM is written following the STOP condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated START condition before the next STOP condition occurs. Using a repeated START condition prevents the t_W delay required for the EEPROM write cycle to finish.

Writing multiple bytes to a slave: I²C write operations of multiple bytes can also be performed. During a single write sequence, up to 8 bytes in one page can be written at one time. If more than eight bytes are transmitted in the sequence, then only the last eight transmitted bytes are stored. After the last physical memory location in a particular page (8-byte page write), the address counter automatically wraps back to the first location in the same page for subsequent byte write operations.

Acknowledge polling: Any time a EEPROM byte is written, the DS1841 requires the EEPROM write time (t$_W$) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS1841, which allows communication to continue as soon as the DS1841 is ready. The alternative to acknowledge polling is to wait for a maximum period of t$_W$ to elapse before attempting to access the device.

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Reading multiple bytes from a slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a STOP condition. During a single read sequence of multiple bytes, after the last address counter position of FFh is accessed, the address counter automatically wraps back to the first location, 00h. Read operations can continue indefinitely.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condi-
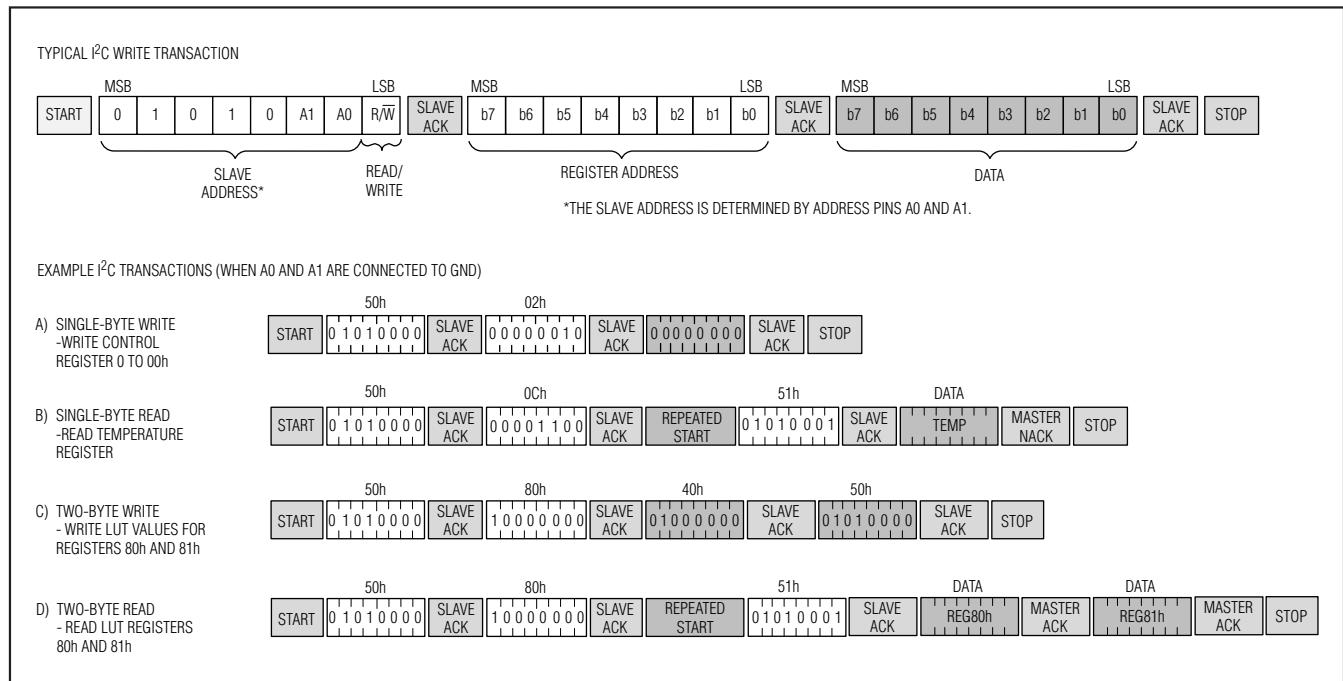

Figure 4. I²C Communication Examples

DS1841

tion, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. See Figure 4 for I2C Communication Examples.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS1841, decouple both the power-supply pin and the wiper-bias voltage pin with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead induc-

tance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

SDA and SCL Pullup Resistors

SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the AC electrical characteristics are within specification. A typical value for the pullup resistors is 4.7kΩ.

Appendix A: Control Bits Logic Table

LUTAR MODE BIT	WIPER ACCESS CONTROL BIT	ADDER MODE BIT	UPDATE MODE BIT	CONTROL OF WR AND REGISTER FUNCTIONALITY
X	X	X	0	IVR is loaded to WR on power-up. Subsequent writes to 00h set the value of WR.
0	0	0	1	Temperature conversion references the LUT, determining LUTAR value, the LUTAR determines the LUTVAL value, the unsigned LUTVAL value is then automatically loaded into WR.
0	0	1	1	Temperature conversion references the LUT, determining LUTAR value, the LUTAR sets the LUTVAL value, the signed LUTVAL value is then summed with IVR, and the result is loaded into WR.
X	1	0	1	I2C Write (to 09h): The unsigned value written to WR, register 09h, is loaded into WR.
X	1	1	1	I2C Write (to 09h): The signed value of LUTVAL is summed with IVR, then loaded into WR, register 09h.
1	0	0	1	I2C Write (to 08h): LUTAR references LUT address, value at LUT address location is loaded into LUTVAL, the unsigned LUTVAL value is loaded into WR.
1	0	1	1	I2C Write (to 08h): LUTAR references LUT address, the signed value at LUT address location is loaded into LUTVAL, the signed LUTVAL value is summed with IVR value, and the result is loaded into WR.

Package Information

(For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

PACKAGE TYPE	DOCUMENT NO.
10 TDFN	**21-0137**

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