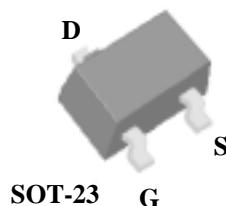




- ▼ Simple Drive Requirement
- ▼ Small Package Outline
- ▼ Surface Mount Device
- ▼ RoHS Compliant

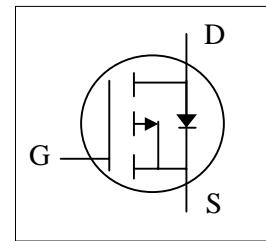


BV_{DSS}	-60V
$R_{DS(ON)}$	250m Ω
I_D	- 1.8A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The SOT-23 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current ³	- 1.8	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current ³	- 1.4	A
I_{DM}	Pulsed Drain Current ^{1,2}	-10	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1.38	W
	Linear Derating Factor	0.01	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Thermal Resistance Junction-ambient ³	Max. 90	$^\circ\text{C}/\text{W}$



Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

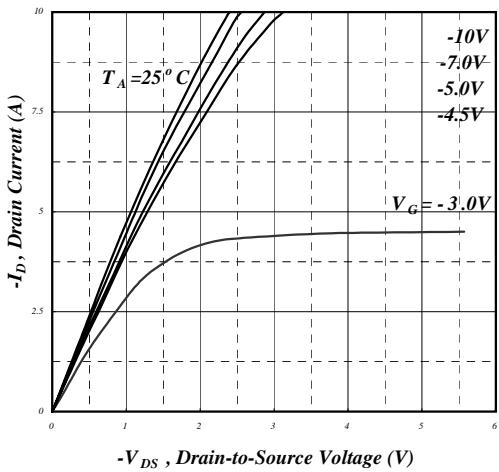
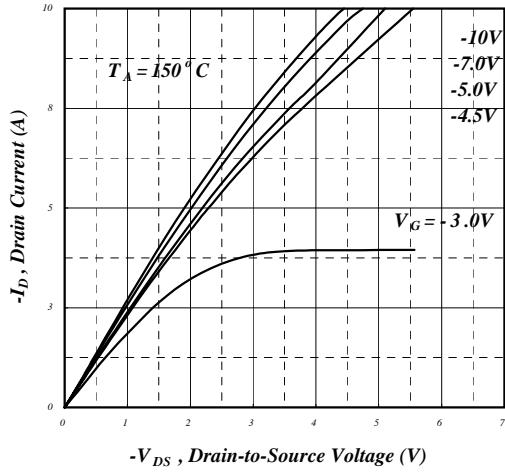
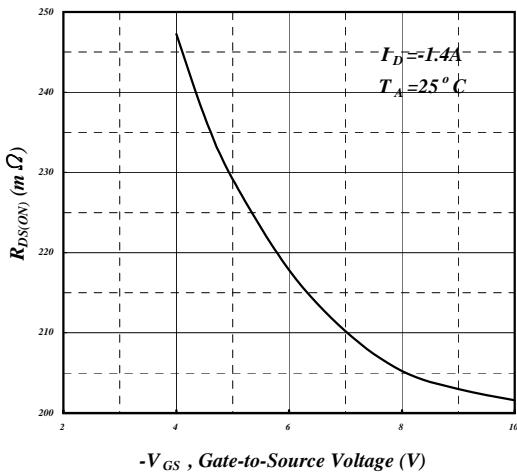
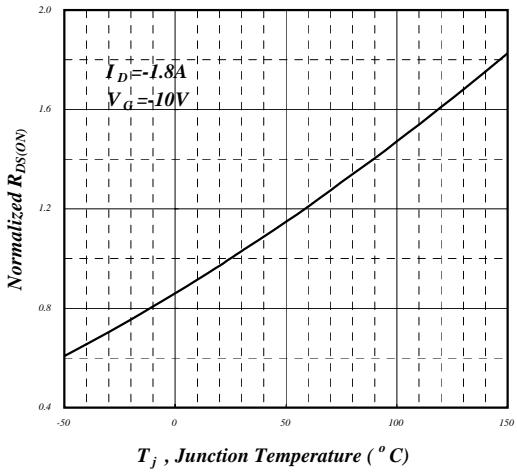
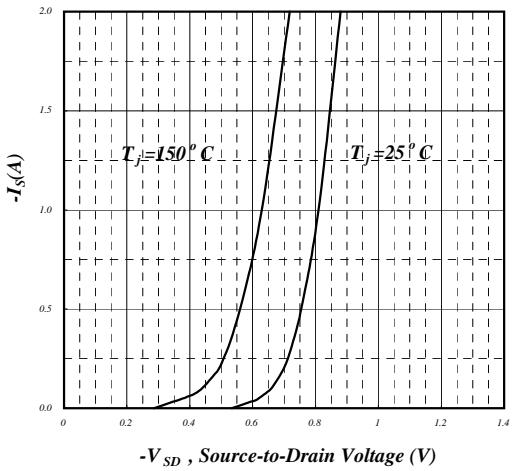
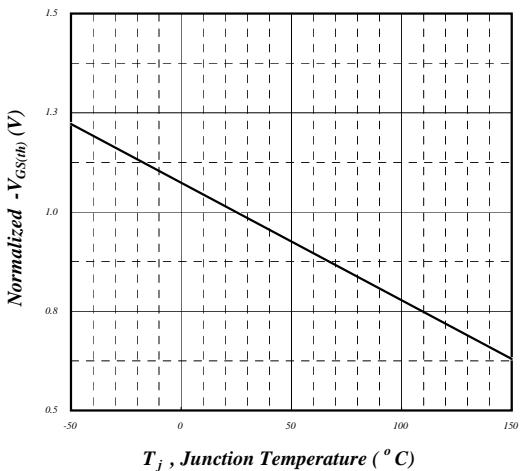
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=-250\mu\text{A}$	-60	-	-	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_{\text{D}}=-1\text{mA}$	-	-0.04	-	$\text{V}/^\circ\text{C}$
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=-10\text{V}$, $I_{\text{D}}=-1.8\text{A}$	-	200	250	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}$, $I_{\text{D}}=-1.4\text{A}$	-	240	300	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=-250\mu\text{A}$	-1	-	-3	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=-10\text{V}$, $I_{\text{D}}=-1\text{A}$	-	2	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{\text{DS}}=-60\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	-10	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{\text{DS}}=-48\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 20\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_{\text{D}}=-1\text{A}$	-	6	10	nC
Q_{gs}	Gate-Source Charge		-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	3	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time ²	$V_{\text{DS}}=-30\text{V}$	-	8	-	ns
t_r	Rise Time	$I_{\text{D}}=-1\text{A}$	-	5	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_G=3.3\Omega$, $V_{\text{GS}}=-10\text{V}$	-	22	-	ns
t_f	Fall Time	$R_D=30\Omega$	-	3	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	510	810	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=-25\text{V}$	-	50	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	40	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	6.4	9.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-1.2\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=-1\text{A}$, $V_{\text{GS}}=0\text{V}$,	-	30	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100\text{A}/\mu\text{s}$	-	38	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; $270^\circ\text{C}/\text{W}$ when mounted on Min. copper pad.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. On-Resistance v.s. Gate Voltage

Fig 4. Normalized On-Resistance v.s. Junction Temperature

Fig 5. Forward Characteristic of

Fig 6. Gate Threshold Voltage v.s.

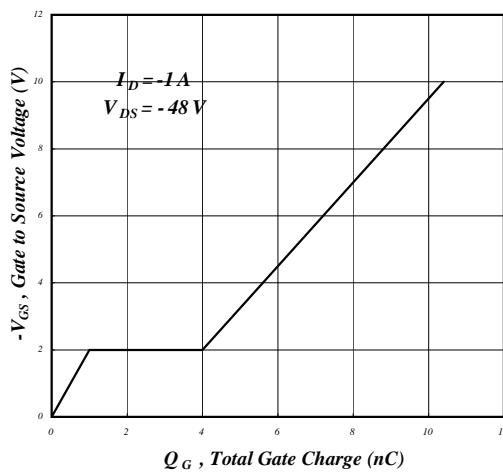


Fig 7. Gate Charge Characteristics

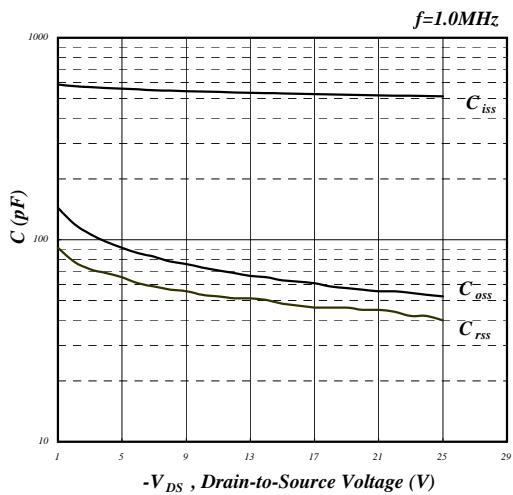


Fig 8. Typical Capacitance Characteristics

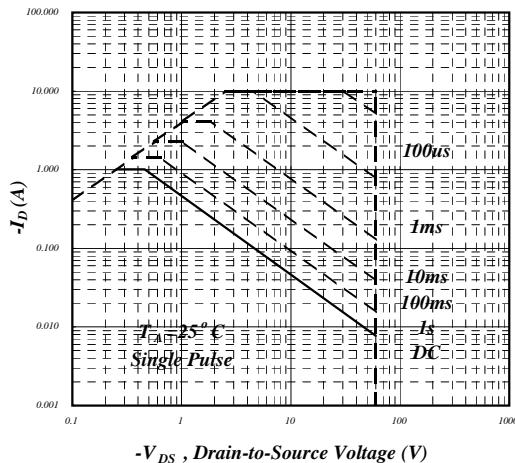


Fig 9. Maximum Safe Operating Area

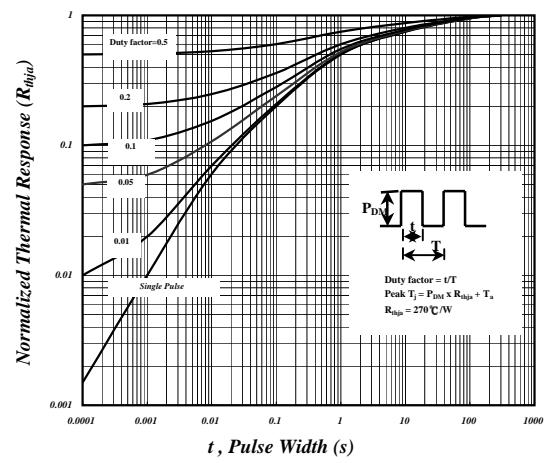


Fig 10. Effective Transient Thermal Impedance

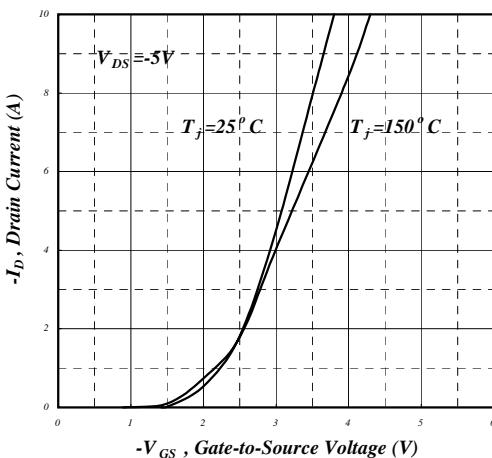


Fig 11. Transfer Characteristics

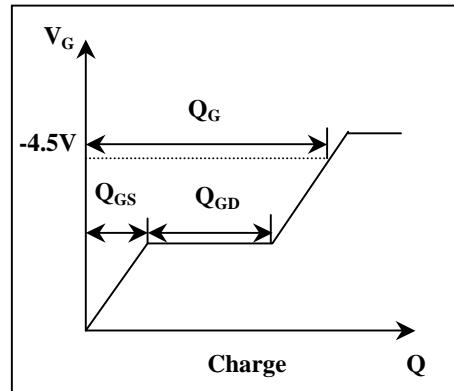


Fig 12. Gate Charge Circuit