AK4641EN

16-Bit ΔΣ CODEC with Bluetooth Interface

GENERAL DESCRIPTION

The AK4641EN is targeted at PDA and other low-power, small size applications. It features a 16bit Stereo CODEC with a built-in Microphone-Amplifier and 16bit Mono CODEC for Bluetooth Interface. Input circuits include Microphone-Amplifier and ALC (Auto Level Control) circuit. The AK4641EN is available in a 36pin QFN, utilizing less board space than competitive offerings.

FEATURES

1. Recording Function of 16bit Stereo CODEC
- **Mono Input**
- **2 to 1 Selector (Internal and External MIC)**
- **1st MIC Amplifier: +20dB or 0dB**
- **2nd Amplifier with ALC: +27.5dB ~ –8dB, 0.5dB Step**
- **ADC Performance: S/(N+D): 81dB, S/N: 86dB**
- **Sampling Rate: 7kHz ~ 48kHz**
- **Audio Interface Format: I2S, 16bit MSB justified**

2. Playback Function of 16bit Stereo CODEC
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital Volume (0dB ~ –127dB, 0.5dB Step, Mute)**
- **5 Band Equalizer**
- **Stereo Line Output**
  - **Performance: S/(N+D): 86dB, S/N: 90dB**
- **Mono Line Output**
  - **Differential Output**
  - **Performance: S/(N+D): 86dB, S/N: 93dB**
- **AUX Input**
  - **Differential Input**
  - **+24dB ~ –21dB, 3dB step**
- **Sampling Rate: 7kHz ~ 48kHz**
- **Audio Interface Format: I2S, 16bit MSB justified, 16bit LSB justified**

3. 16bit Mono CODEC
- **Analog Mix Path for Bluetooth Interface**
- **Sample Rate: 8kHz ~ 16kHz**
- **Audio Interface Format: Short/Long Frame, I2S, 16bit MSB justified**

4. Power Management

5. Master Clock: 1.792MHz ~ 12.288MHz

6. Control mode: I2C Bus

7. Ta = –20 ~ 85°C

8. Power Supply: 2.6V~ 3.6V (typ. 3.3V)

9. Power Supply Current: 17mA

10. Package: 36pin QFN (0.5mm pitch)

■ Block Diagram

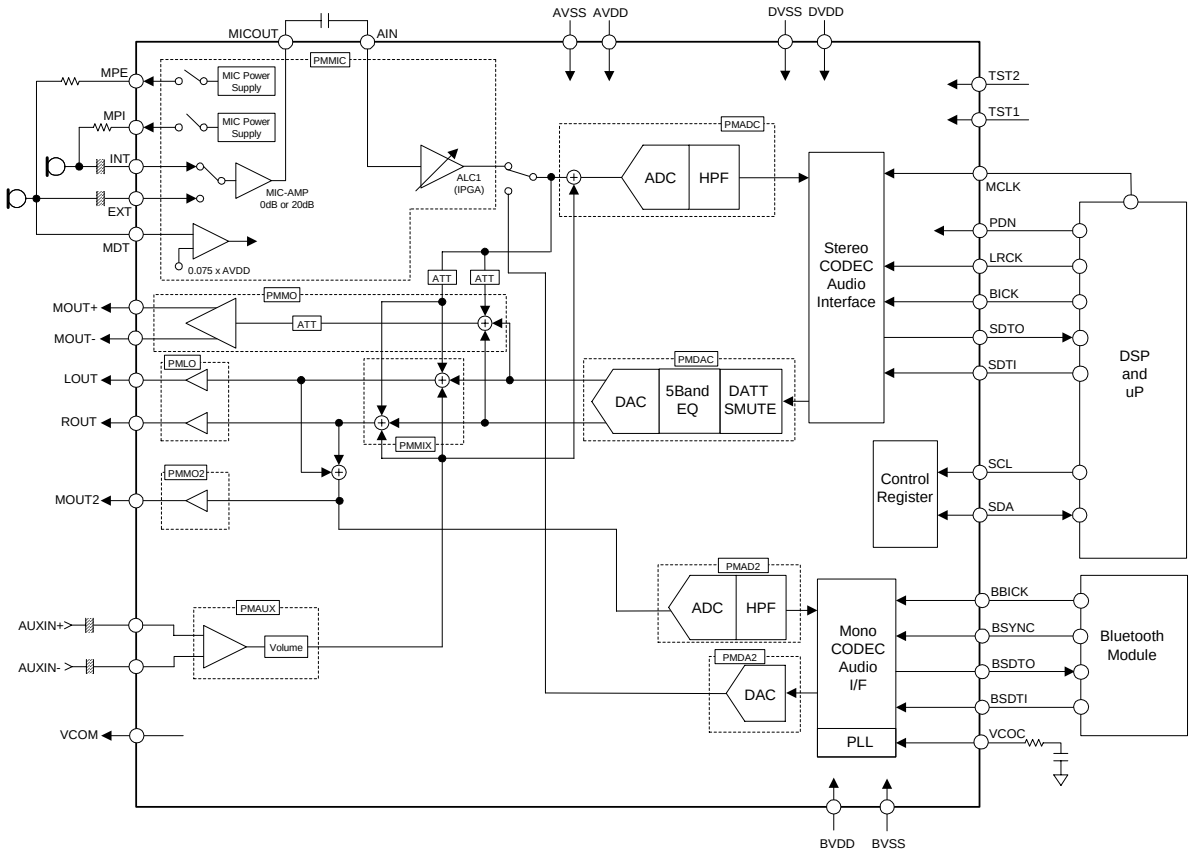
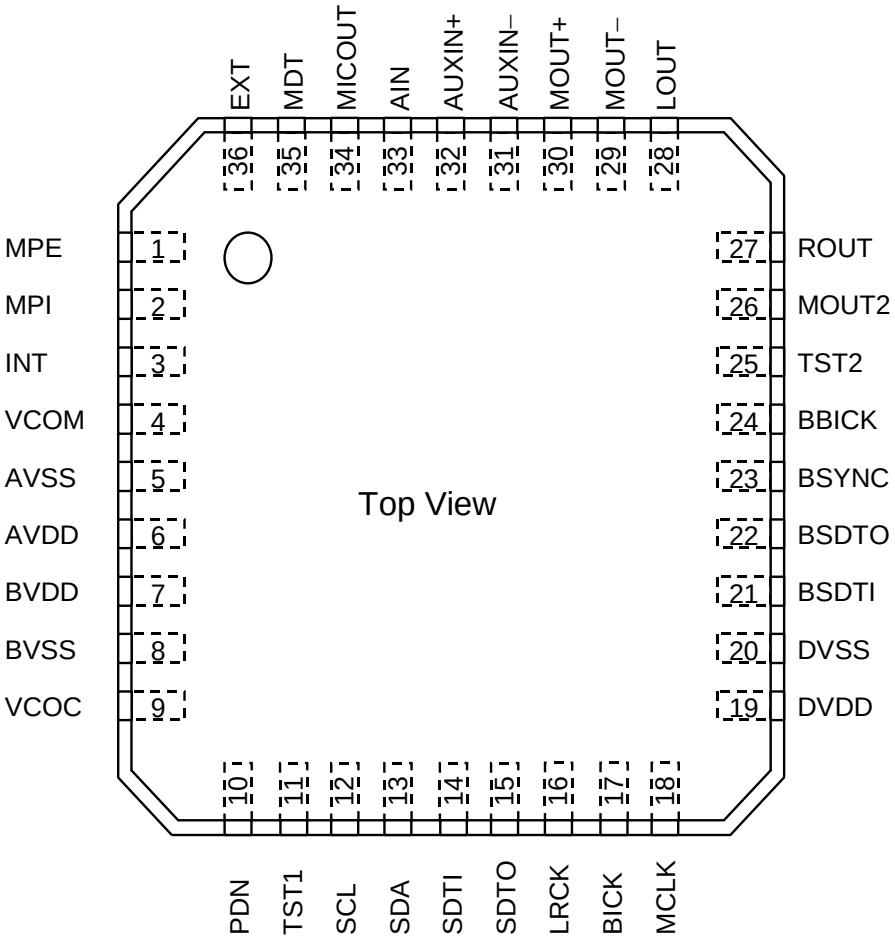


Figure 1. Block Diagram

■ Ordering Guide

AK4641EN	–20 ~ +85°C	36pin QFN (0.5mm pitch)
AKD4641EN	Evaluation board for AK4641EN	

■ Pin Layout (36pin QFN)



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MPE	O	MIC Power Supply Pin for External Microphone
2	MPI	O	MIC Power Supply Pin for Internal Microphone
3	INT	I	Internal Microphone Input Pin (Mono Input)
4	VCOM	O	Common Voltage Output Pin, 0.45*AVDD Bias voltage of ADC inputs and DAC outputs.
5	AVSS	-	Analog Ground Pin
6	AVDD	-	Analog Power Supply Pin
7	BVDD	-	Power Supply Pin for 16bit Mono CODEC of Bluetooth I/F
8	BVSS	-	Ground Pin for 16bit Mono CODEC of Bluetooth I/F
9	VCOC	O	PLL Loop Filter Pin for 16bit Mono CODEC of Bluetooth I/F
10	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register.
11	TST1	I	Test Pin. Connect to DVSS.
12	SCL	I	Control Data Clock Pin
13	SDA	I/O	Control Data Input Pin
14	SDTI	I	Audio Serial Data Input Pin
15	SDTO	O	Audio Serial Data Output Pin
16	LRCK	I	Input/Output Channel Clock Pin
17	BICK	I	Audio Serial Data Clock Pin
18	MCLK	I	External Master Clock Input Pin
19	DVDD	-	Digital Power Supply Pin
20	DVSS	-	Digital Ground Pin
21	BSDTI	I	Serial Data Input Pin for 16bit Mono CODEC of Bluetooth I/F
22	BSDTO	O	Serial Data Output Pin for 16bit Mono CODEC of Bluetooth I/F
23	BSYNC	I	Sync Signal Pin for 16bit Mono CODEC of Bluetooth I/F
24	BBICK	I	Serial Data Clock Pin for 16bit Mono CODEC of Bluetooth I/F
25	TST2	I	Test Pin. Connect to AVSS.
26	MOUT2	O	Mono Line Output 2 Pin
27	ROUT	O	Rch Stereo Line Output Pin
28	LOUT	O	Lch Stereo Line Output Pin
29	MOUT–	O	Mono Line Negative Output Pin
30	MOUT+	O	Mono Line Positive Output Pin
31	AUX IN–	I	Mono AUX Negative Input Pin
32	AUX IN+	I	Mono AUX Positive Input Pin
33	AIN	I	Analog Input Pin
34	MICOUT	O	Microphone Analog Output Pin
35	MDT	I	Microphone Detect Pin (Internal pull down by 500kΩ)
36	EXT	I	External Microphone Input Pin (Mono Input)

Note: All input pins except analog input pins (INT, EXT, AIN, AUXIN+, AUXIN–, MDT) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog Input	INT, AUXIN+, AUXIN–, AIN, MDT, EXT	These pins should be open.
Analog Output	MPE, MPI, MOUT2, ROUT, LOUT, MOUT–, MOUT+, MICOUT	These pins should be open.
Digital Input	BSDTI, BSYNC, BBICK	These pins should be connected to DVSS.
Digital Output	BSDTO	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, BVSS =0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	16bit Mono CODEC	BVDD	–0.3	4.6	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – BVSS| (Note 2)	ΔGND2	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–20	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and BVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, BVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	2.6	3.3	3.6	V
(Note 3)	Digital	DVDD	2.6	3.3	3.6	V
	16bit Mono CODEC	BVDD	2.6	3.3	3.6	V
	Differences	AVDD–BVDD	–0.1	0	+0.1	V
		AVDD–DVDD	–0.3	0	+0.3	V
		BVDD–DVDD	–0.3	0	+0.3	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, DVDD and BVDD is not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=BVDD=3.3V; AVSS=DVSS=BVSS=0V; Signal Frequency=1kHz; 16bit Data;
Stereo CODEC: fs=44.1kHz, BICK=64fs; Measurement frequency=20Hz ~ 20kHz;
Mono CODEC: Bfs=8kHz; BBICK=32Bfs; Measurement frequency=20Hz ~ 3.4kHz; unless otherwise specified)

Parameter		Min	typ	max	Units
MIC Amplifier					
Input Resistance		20	30	40	kΩ
Gain	MGAIN bit = "0"	-	0	-	dB
	MGAIN bit = "1"	-	+20	-	dB
MIC Power Supply					
Output Voltage (Note 4)		2.22	2.47	2.72	V
Load Resistance		2	-	-	kΩ
Load Capacitance		-	-	30	pF
MIC Detection					
Comparator Voltage Level (Note 5)		0.165	-	0.257	V
Internal pull down Resistance		250	500	750	kΩ
Input PGA Characteristics:					
Input Resistance (Note 6)		5	10	15	kΩ
Step Size		0.1	0.5	0.9	dB
Gain Control Range	Max (IPGA6-0 bits = "47H")	-	+27.5	-	dB
	Min (IPGA6-0 bits = "00H")	-	–8	-	dB
ADC Analog Input Characteristics of Stereo CODEC: MIC Gain=+20dB, IPGA=0dB, ALC1=OFF, MIC → IPGA → ADC of Stereo CODEC					
Resolution		-	-	16	Bits
Input Voltage (MIC Gain=+20dB, Note 7)		0.168	0.198	0.228	Vpp
S/(N+D) (–1dBFS)		71	81	-	dB
D-Range (–60dBFS, A-weighted)		78	86	-	dB
S/N	MIC Gain=+20dB, A-weighted	78	86	-	dB
	MIC Gain=0dB, A-weighted	-	92	-	dB
DAC Characteristics of Stereo CODEC:					
Resolution		-	-	16	Bits
Stereo Line Output Characteristics: R_L=10kΩ, DAC of Stereo CODEC → LOUT/ROUT pins					
Output Voltage (Note 8)		1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS)		76	86	-	dBFS
S/N (A-weighted)		82	90	-	dB
Interchannel Isolation		-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.5	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF

Note 4. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ).
Note 5. Comparator Voltage Level is proportional to AVDD voltage. Vout = 0.05 x AVDD (min), 0.078 x AVDD (max).
Note 6. When IPGA Gain is changed, this typical value changes between 8kΩ and 11kΩ.
Note 7. Input voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD (typ).
Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

Parameter		Min	Typ	max	Units
Mono Line Output Characteristics: R_L=20kΩ, DAC of Stereo CODEC → MOUT+/MOUT– pins					
Output Voltage (Note 9)	MOGN bit = "1", –17dB	-	0.305	-	Vpp
	MOGN bit = "0", +6dB	3.56	3.96	4.36	Vpp
S/(N+D) (0dBFS)	MOGN bit = "1", –17dB	-	74	-	dBFS
	MOGN bit = "0", +6dB	76	86	-	dBFS
S/N (A-weighted)	MOGN bit = "1", –17dB	-	77	-	dB
	MOGN bit = "0", +6dB	83	93	-	dB
Load Resistance	MOGN bit = "1", –17dB	2	-	-	kΩ
	MOGN bit = "0", +6dB	20	-	-	kΩ
Load Capacitance		-	-	30	pF
AUX Input: AUXIN+, AUXIN– pins: AUXSI bit = "0"					
Maximum Input Voltage (Note 10)		-	1.98	-	Vpp
Input Resistance		25	40	55	kΩ
Step Size		1	3	5	dB
Gain Control Range	Max (GN3-0 bits = "FH")	-	+24	-	dB
	Min (GN3-0 bits = "0H")	-	–21	-	dB
Mono Output: R_L=10kΩ, DAC of Stereo CODEC → MIX → MOUT2 pin					
Output Voltage (Note 11)		1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS)		76	86	-	dB
S/N (A-weighted)		83	93	-	dB
Load Resistance		10	-	-	kΩ
Load Capacitance (Note 12)		-	-	30	pF
16bit Mono ADC Analog Input Characteristics: AUXIN pin → MIX → ADC of Mono CODEC: AUX Volume = 0dB					
Resolution		-	-	16	Bits
Input Voltage (Note 13)		1.68	1.98	2.28	Vpp
S/(N+D) (–1dBFS)		65	75	-	dB
S/N		79	89	-	dB
16bit Mono DAC Analog Output Characteristics: DAC of Mono CODEC → MOUT+/– pins: MOGN = +6dB					
Resolution		-	-	16	Bits
Output Voltage (Note 14)		3.56	3.96	4.36	Vpp
S/(N+D)		68	78	-	dB
S/N		82	92	-	dB
Power Supplies					
Power Up (PDN pin = "H")					
AVDD+DVDD+ BVDD		-	17	27	mA
Power Down (PDN pin = "L") (Note 15)					
AVDD+DVDD+BVDD		-	-	100	μA

Note 9. Output voltage is proportional to AVDD voltage.
Vout = 1.2 x AVDD (typ) @MOGN bit = "0", 0.092 x AVDD (typ) @MOGN bit = "1" at differential Output.

Note 10. Maximum Input Voltage is proportional to AVDD voltage.
Vin = (AUXIN+) – (AUXIN–) = 0.6 x AVDD (typ) at AUXSI bit = "0",
Vin = AUXIN+ = 0.6 x AVDD (typ) at AUXSI bit = "1".

Note 11. Output Voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

Note 12. When the output pin drives a capacitive load, a resistor should be added in series between the output pin and capacitive load.

Note 13. Input voltage is proportional to AVDD voltage. Vin = 0.6 x AVDD (typ).

Note 14. Output Voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

Note 15. All digital input pins are fixed to DVSS. When the voltage difference among DVDD, BVDD and AVDD is larger than 0.3V, the power supply current at power down mode increases.

FILTER CHARACTERISTICS (Stereo CODEC)

(Ta=−20 ~ 85°C; AVDD, DVDD, BVDD=2.6 ~ 3.6V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	±0.1dB	PB	0	-	17.4	kHz
	−1.0dB		-	20.0	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 17)		GD	-	17.0	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response	−3.0dB	FR	-	3.4	-	Hz
(Note 16)	−0.5dB		-	10	-	Hz
	−0.1dB		-	22	-	Hz
DAC Digital Filter:						
Passband (Note 16)	±0.1dB	PB	0	-	19.6	kHz
	−0.7dB		-	20.0	-	kHz
	−6.0dB		-	22.05	-	
Stopband		SB	25.2	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	59	-	-	dB
Group Delay (Note 17)		GD	-	17.9	-	1/fs
DAC Digital Filter + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 16. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*fs (@-1.0dB), DAC is PB=0.454*fs (@-0.01dB).

Note 17. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16bit data of both channels from the input register to the output of analog signal.

FILTER CHARACTERISTICS (16bit Mono CODEC)

(Ta=−20 ~ 85°C; AVDD, DVDD, BVDD=2.6 ~ 3.6V; Bfs=8kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 16)	±0.1dB	PB	0	-	3.1	kHz
	−1.0dB		-	3.6	-	kHz
	−3.0dB		-	3.8	-	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 17)		GD	-	17.0	-	1/Bfs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response	−3.0dB	FR	-	0.62	-	Hz
(Note 16)	−0.5dB		-	1.81	-	Hz
	−0.1dB		-	3.99	-	Hz
DAC Digital Filter:						
Passband (Note 16)	±0.1dB	PB	0	-	3.6	kHz
	−0.7dB		-	3.6	-	kHz
	−6.0dB		-	4.0	-	
Stopband		SB	4.6	-	-	kHz
Passband Ripple		PR	-	-	±0.01	dB
Stopband Attenuation		SA	59	-	-	dB
Group Delay (Note 17)		GD	-	15.8	-	1/Bfs
DAC Digital Filter + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 16. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*Bfs (@-1.0dB), DAC is PB=0.454*Bfs (@-0.01dB).

Note 17. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16bit data of both channels from the input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=–20 ~ 85°C; AVDD, DVDD, BVDD=2.6 ~ 3.6V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (Note 18)	VAC	50%DVDD	-	-	V
High-Level Output Voltage (Iout=–200μA)	VOH	DVDD–0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout=200μA)	VOL	-	-	0.2	V
(SDA pin: Iout=3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

Note 18. The external clock is input to MCLK pin via AC coupled capacitor.

SWITCHING CHARACTERISTICS

(Ta=–20 ~ 85°C; AVDD, DVDD, BVDD=2.6 ~ 3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
16bit Stereo CODEC Interface Timing:					
Master Clock Timing (MCLK pin)					
Frequency	fCLK	1.792	-	12.288	MHz
Pulse Width Low	tCLKL	0.3/fCLK	-	-	ns
Pulse Width High	tCLKH	0.3/fCLK	-	-	ns
AC Pulse Width (Note 19)	tACW	0.4/fCLK	-	-	ns
LRCK Timing					
Frequency	fs	7	-	48	kHz
Duty Cycle	Duty	45	-	55	%
Audio Interface Timing					
BICK Period	tBCK	312.5	-	-	ns
BICK Pulse Width Low	tBCKL	130	-	-	ns
Pulse Width High	tBCKH	130	-	-	ns
LRCK Edge to BICK "↑" (Note 20)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 20)	tBLR	50	-	-	ns
LRCK to SDTO (MSB) (Except I^2S mode)	tLRS	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 19. Refer to Figure 3.
Note 20. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
16bit Mono CODEC Interface Timing:					
SYNC Timing					
Frequency (PLL Lock Range)	Bfs	8	-	16	kHz
Serial Interface Timing at Short/long Frame Sync					
BBICK Frequency	fBBCK	128		2048	kHz
BBICK Period	tBBCK	488			ns
BBICK duty cycle	tBDUT		50		%
BBICK Pulse Width Low	tBBCKL	200			ns
Pulse Width High	tBBCKH	200			ns
BSYNC Edge to BBICK "↓"	tBSYB	50			ns
BBICK "↓" to BSYNC Edge	tBBSY	50			ns
BSYNC to BSDTO (MSB) (Except Short Frame)	tBSYD			80	ns
BBICK "↑" to BSDTO	tBBSD			80	ns
BSDTI Hold Time	tBSDH	50			ns
BSDTI Setup Time	tBSDS	50			ns
BSYNC Pulse Width Low	tBBSL	3300			ns
Pulse Width High	tBBSH	440			ns
Serial Interface Timing at MSB justified and I^2S					
BBICK Frequency	fBBCK	256		2048	kHz
BBICK Period	tBBCK	488			ns
BBICK duty cycle	tBDUT		50		%
BBICK Pulse Width Low	tBBCKL	200			ns
Pulse Width High	tBBCKH	200			ns
BSYNC Edge to BBICK "↑"	tBSYB2	50			ns
BBICK "↑" to BSYNC Edge	tBBSY2	50			ns
BSYNC to BSDTO (MSB) (Except I^2S mode)	tBSYD2			80	ns
BBICK "↓" to BSDTO	tBBSD2			80	ns
BSDTI Hold Time	tBSDH2	50			ns
BSDTI Setup Time	tBSDH2	50			ns
BSYNC Duty Cycle	BDuty2	45	50	55	%
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	μs
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note 21)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	TSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Reset Timing					
PDN Pulse Width (Note 22)	tPD	150			ns
PMADC "↑" to SDTO valid (Note 23)	tPDV		2081		1/fs
PMAD2 "↑" to BSDTO valid (Note 24)	tBPDV		1057		1/Bfs

Note 21. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 22. The AK4641EN can be reset by the PDN pin = "L".
Note 23. This is the count of LRCK "↑" from the PMADC bit = "1".
Note 24. This is the count of BSYNC "↑" from the PMAD2 bit = "1".

Purchase of Asahi Kasei Microsystems Co., Ltd I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conform to the I^2C specifications defined by Philips.

■ **Timing Diagram**

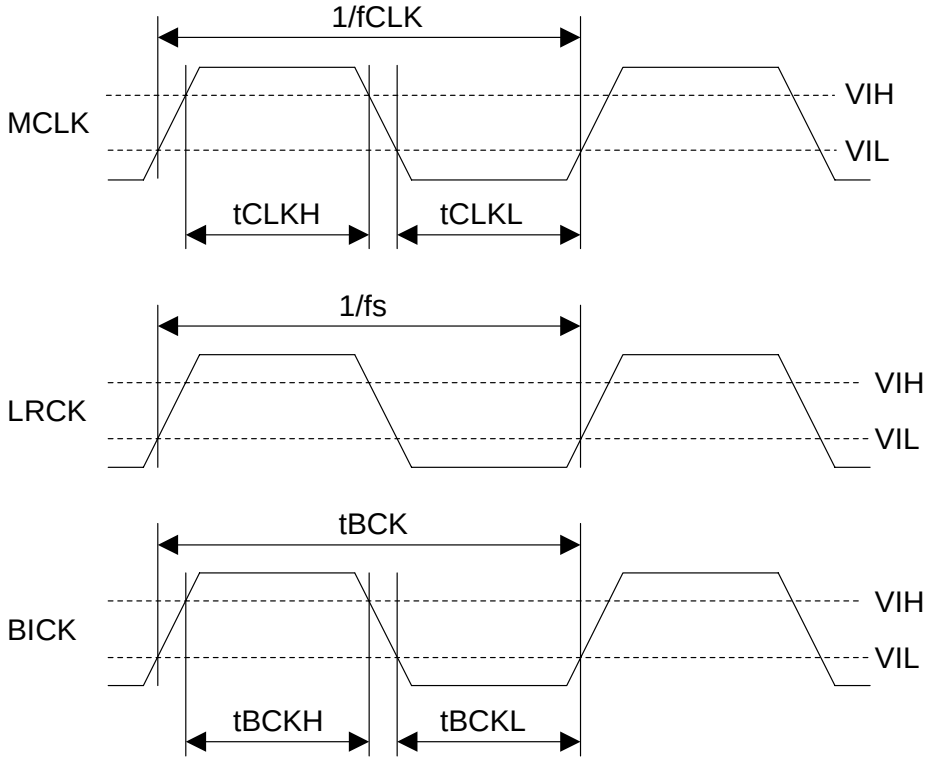
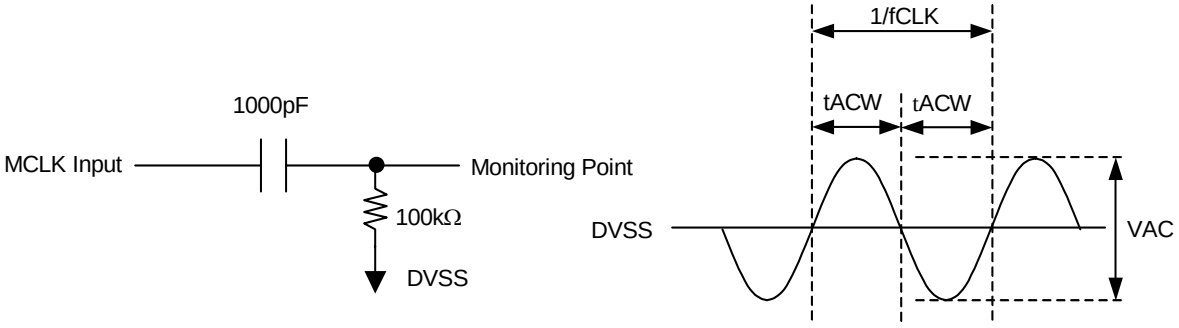


Figure 2. Clock Timing of Stereo CODEC



Note. This circuit shows how to monitor MCLK AC Coupling Timing. This circuit is not used in actual system.
Figure 3. MCLK AC Coupling Timing

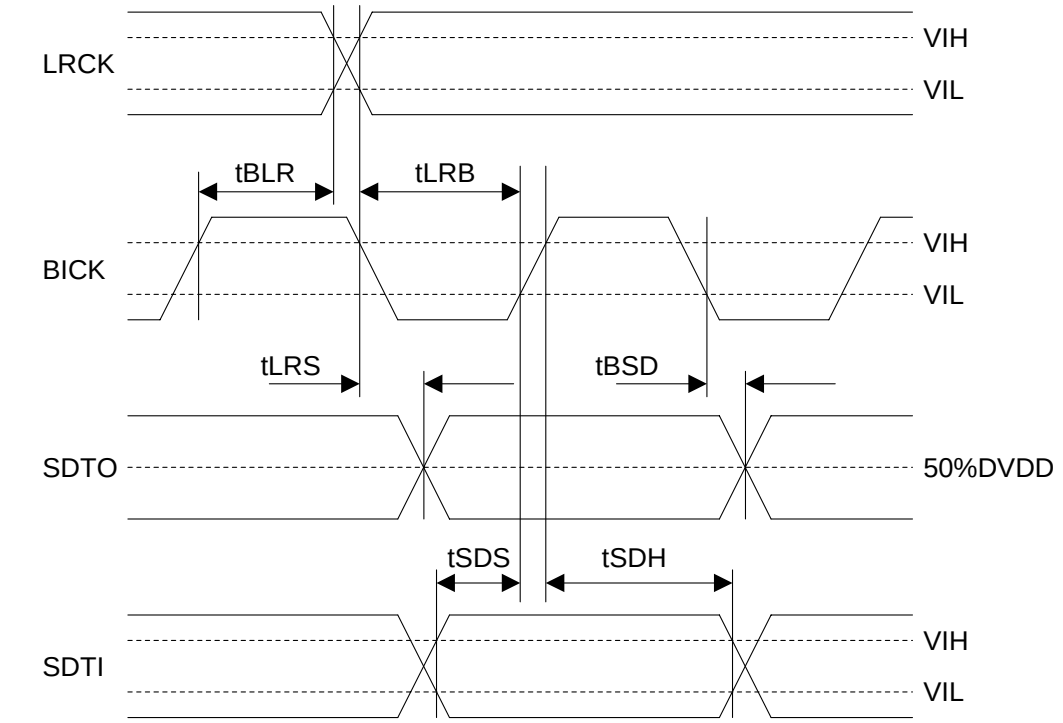


Figure 4. Audio Interface Timing of Stereo CODEC

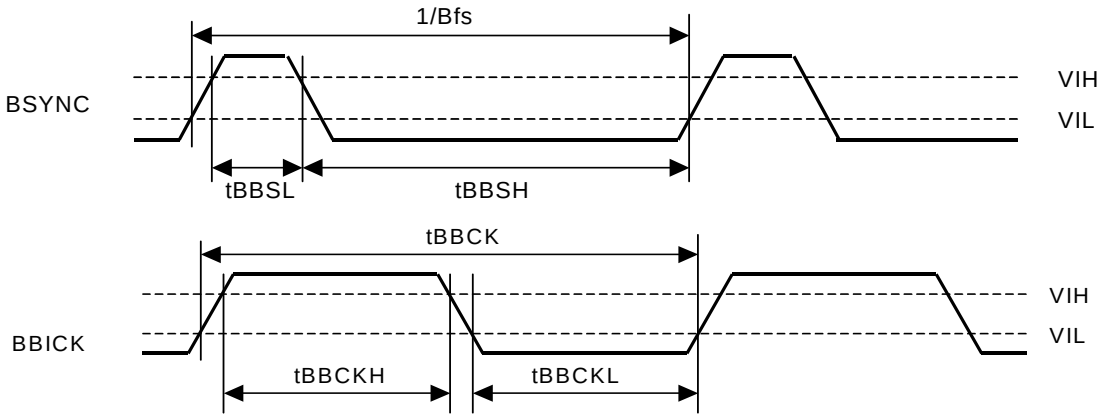


Figure 5. Clock Timing of 16bit Mono CODEC

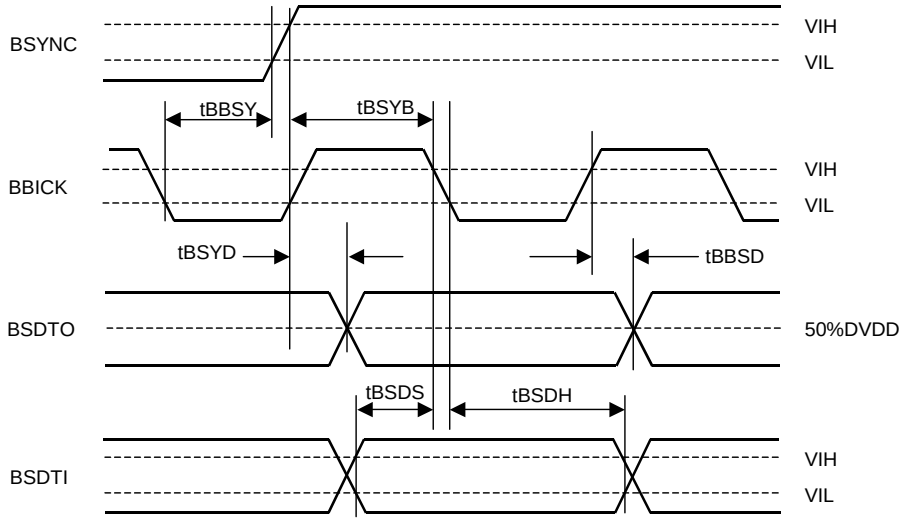


Figure 6. 16bit Mono CODEC Interface Timing at short and long frame sync

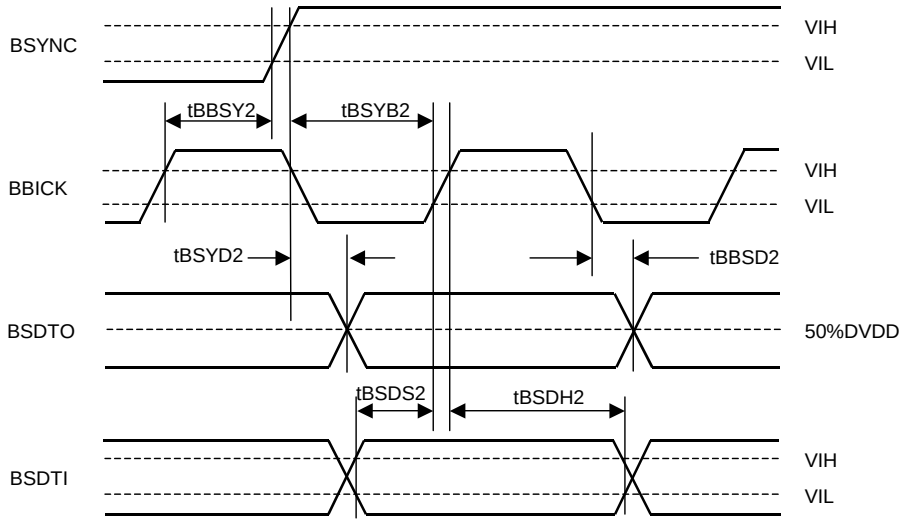


Figure 7. 16bit Mono CODEC Interface Timing at MSB justified and I^2S

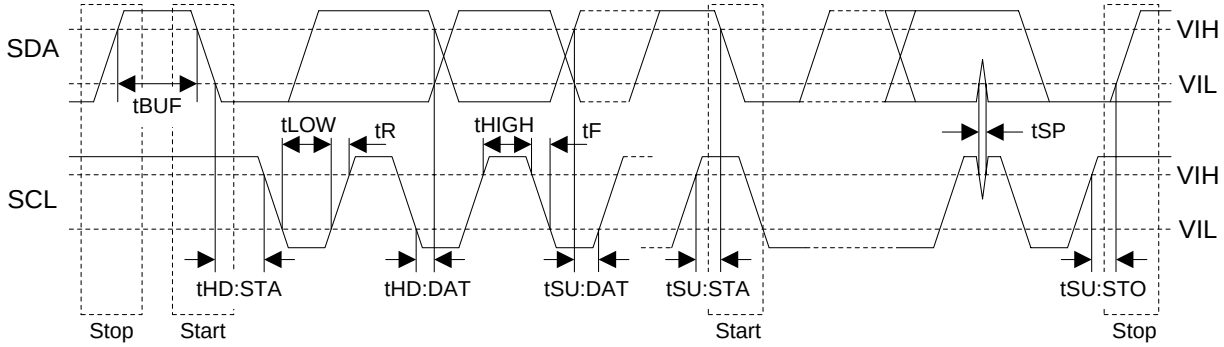


Figure 8. I^{2}C Bus Mode Timing

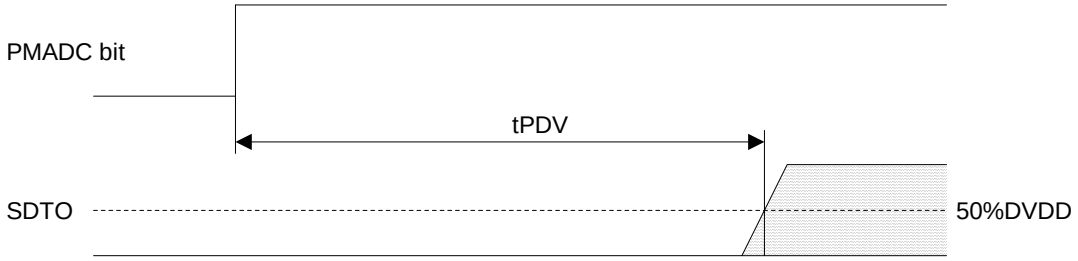


Figure 9. Power Down & Reset Timing 1

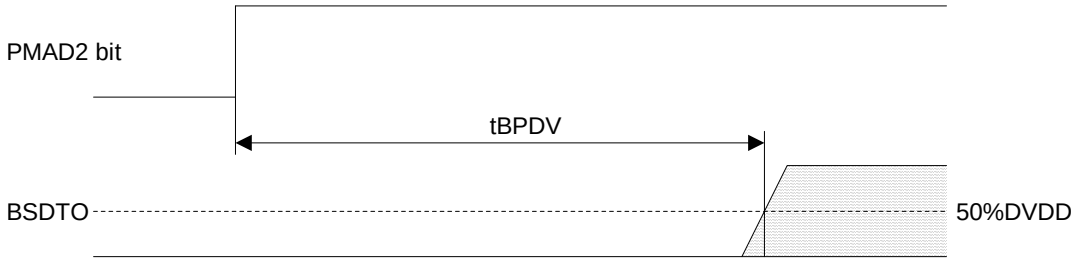


Figure 10. Power Down & Reset Timing 2

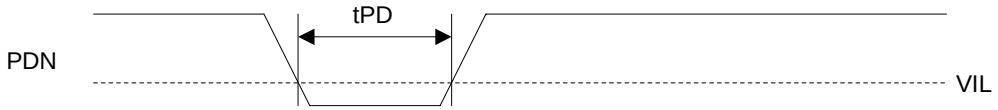


Figure 11. Power Down & Reset Timing 3

OPERATION OVERVIEW

■ System Clock Input

The AK4641EN requires a master clock (MCLK). This master clock is input to the AK4641EN by inputting an external CMOS-level clock to the MCLK pin or by inputting an external clock that is greater than 50% of the DVDD level to the MCLK pin through a capacitor. MCKPD and MCKAC bits should be set as shown in Table 1. ADC and DAC of 16bit Stereo CODEC are powered-down at MCKPD bit = "1".

Master Clock	Status	MCKAC bit	MCKPD bit
External Clock Direct Input (Figure 12)	Clock is input to MCLK pin.	0	0
	Clock is not input to MCLK pin.	0	1
AC Coupling Input (Figure 13)	Clock is input to MCLK pin.	1	0
	Clock is not input to MCLK pin.	1	1

Table 1. MCKPD and MCKAC bits Setting for Master Clock Status

(1) External Clock Direct Input

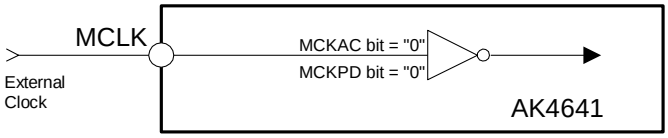


Figure 12. External Master Clock Input Block

(2) AC Coupling Input

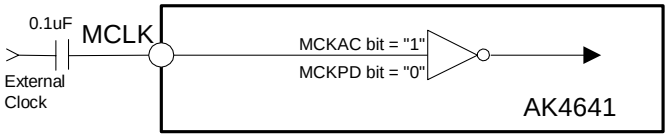


Figure 13. External Clock mode (Input: ≥ 50%DVDD)

The clock required to operate are MCLK, LRCK (fs) and BICK (≥ 32fs). Then the master clock (MCLK) should be synchronized with LRCK. The phase between these clocks does not matter.

The S/N of the DAC of Stereo CODEC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output of Stereo CODEC through Headphone amp at fs=8kHz is shown in Table 3.

MCK1	MCK0	Sampling Frequency (fs)	MCLK	
0	0	7kHz~48kHz	256fs	Default
0	1	7kHz~24kHz	512fs	
1	0	7kHz~12kHz	1024fs	
1	1	-	N/A	

Table 2. Select Master Clock Frequency

MCLK	S/N (fs=8kHz, A-weighted)
256fs	82dB
512fs	90dB
1024fs	90dB

Table 3. Relationship between MCLK and S/N of Line Out

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4641EN may occur pop noise.

All external clocks (MCLK, BICK and LRCK) should always be present when either ADC or DAC of Stereo CODEC is power-up. If these clocks are not provided, the AK4641EN may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4641EN should be in the power-down mode.

	Power up	Power down
BICK pin	Input	Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally

Table 4. Clock Operation

■ System Reset

Upon power-up, reset the AK4641EN by bringing the PDN pin = “L”. This ensures that all internal registers are reset to their initial values.

The ADC of Stereo CODEC enters an initialization cycle that starts when the PMADC bit is changed from “0” to “1”. The initialization cycle time is 2081/fs, or 47.2ms@fs=44.1kHz. During the initialization cycle, the ADC digital data output of Stereo CODEC is forced to a 2's compliment, “0”. The ADC output of Stereo CODEC reflects the analog input signal after the initialization cycle is complete. The DAC of Stereo CODEC does not require an initialization cycle.

The ADC of Mono CODEC enters an initialization cycle that starts when the PMAD2 bit is changed from “0” to “1”. The initialization cycle time is 1057/Bfs, or 132ms@Bfs=8kHz. During the initialization cycle, the ADC digital data output of Mono CODEC is forced to a 2's compliment, “0”. The ADC output of Mono CODEC reflects the analog input signal after the initialization cycle is complete. The DAC of Mono CODEC does not require an initialization cycle.

■ Audio Interface Format of Stereo CODEC

Three types of data formats are available and are selected by setting the DIF1-0 bits. In all modes, the serial data is MSB first, 2's complement format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. LRCK and BICK must be input to the AK4641EN in slave mode. If 16bit data that ADC of Stereo CODEC outputs is converted to 8bit data by removing LSB 8bit, "−1" at 16bit data is converted to "−1" at 8bit data. And when the DAC of Stereo CODEC playbacks this 8bit data, "−1" at 8bit data will be converted to "−256" at 16bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16bit data before converting to 8bit data.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 14	
1	0	1	MSB justified	MSB justified	≥ 32fs	Figure 15	
2	1	0	I^2S	I^2S	≥ 32fs	Figure 16	Default
3	1	1	N/A	N/A	N/A	-	

Table 5. Audio Interface Format of Stereo CODEC

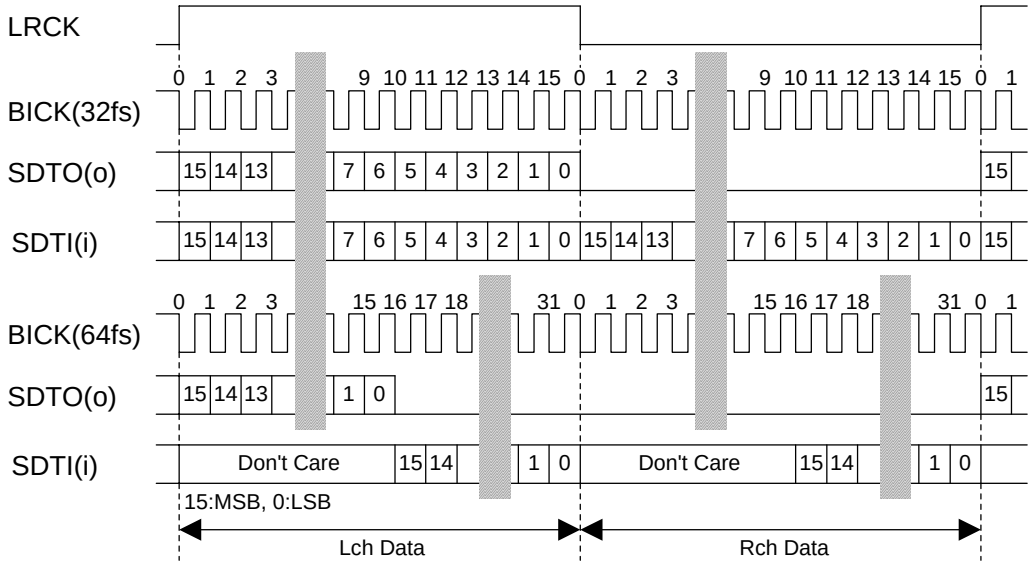


Figure 14. Mode 0 Timing

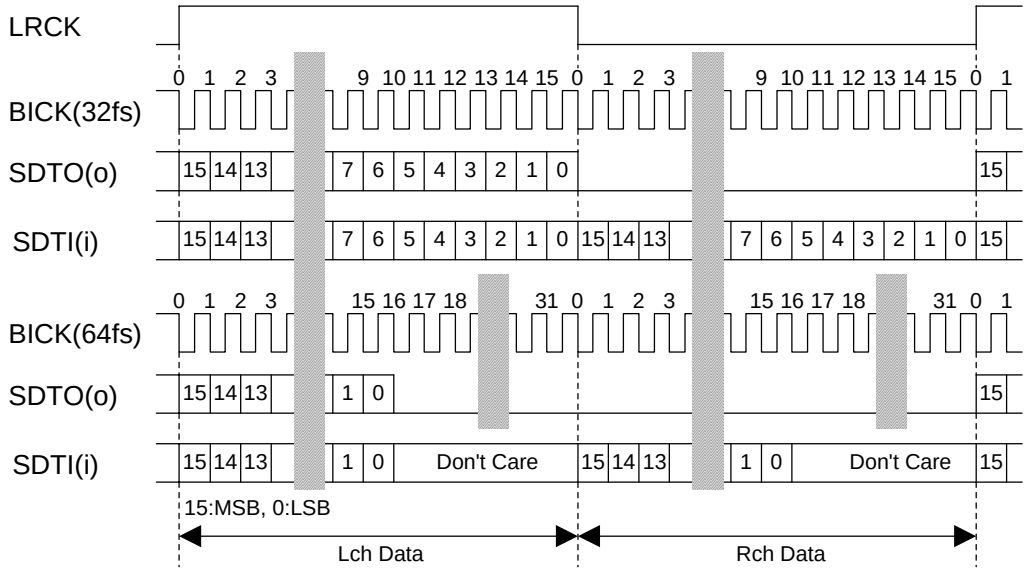


Figure 15. Mode 1 Timing

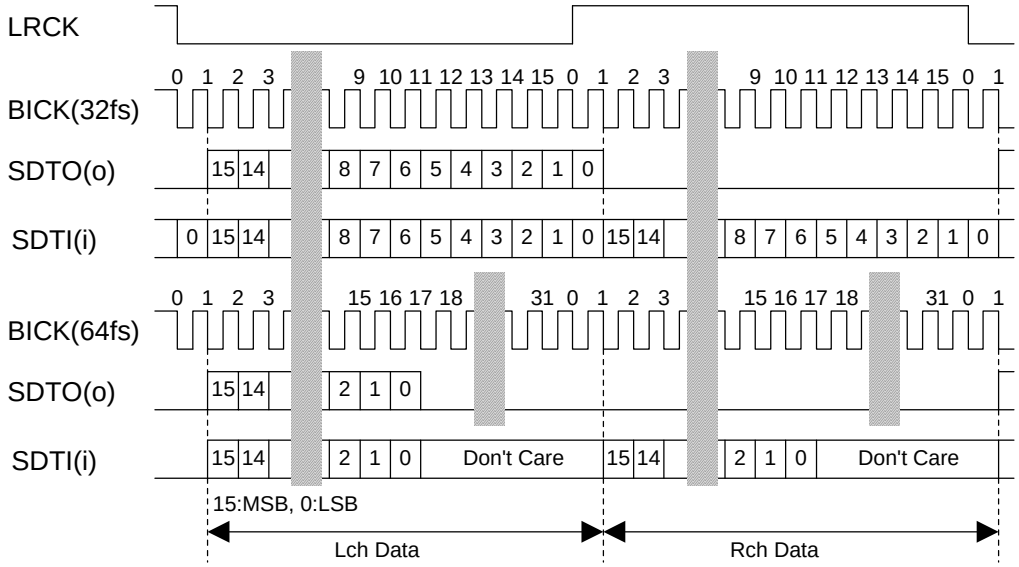


Figure 16. Mode 2 Timing

■ Audio Interface Format of Mono CODEC

Four types of data formats are available for 16bit Mono CODEC and are selected by setting the BTFMT1-0 bits. In all modes, the serial data is MSB first, 2's complement format. In short frame sync and long frame sync modes, the BSDTO is clocked out on the rising edge of BBICK and the BSDTI is latched on the falling edge. In MSB justified and I^2S modes, the BSDTO is clocked out on the falling edge of BBICK and the BSDTI is latched on the rising edge. BSYNC and BBICK must be input to the AK4641EN.

Mode	BTFMT1-0	BBICK	Figure	
Short Frame Sync	00	≥ 16Bfs	Figure 17	Default
Long Frame Sync	01	≥ 16Bfs	Figure 18	
MSB justified	10	≥ 32Bfs	Figure 19	
I^2S	11	≥ 32Bfs	Figure 20	

Table 6. Audio Interface Format for 16bit Mono CODEC

(1) Short Frame Sync

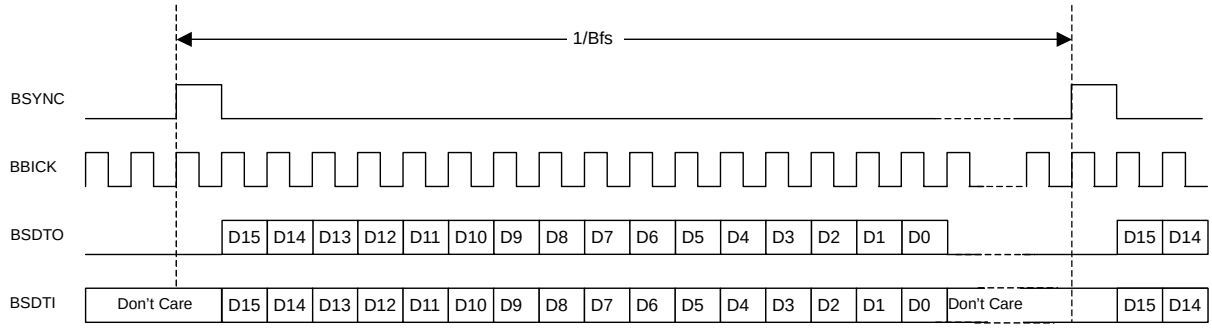


Figure 17. Timing of Short Frame Sync

(2) Long Frame Sync

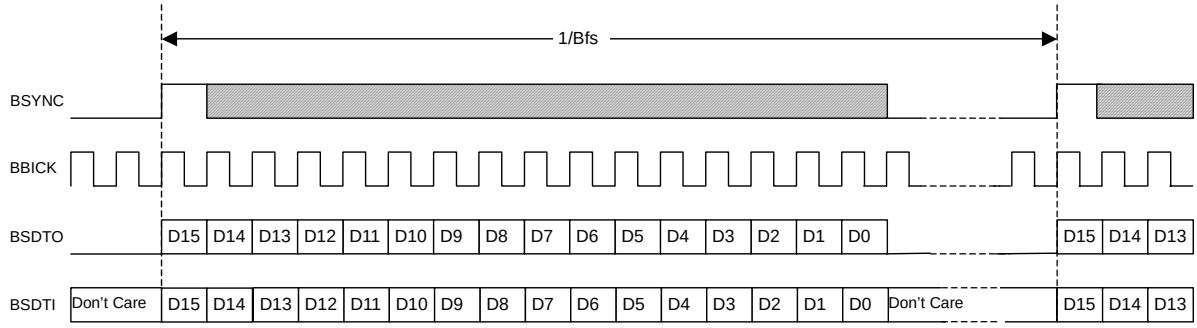


Figure 18. Timing of Long Frame Sync

(3) MSB justified

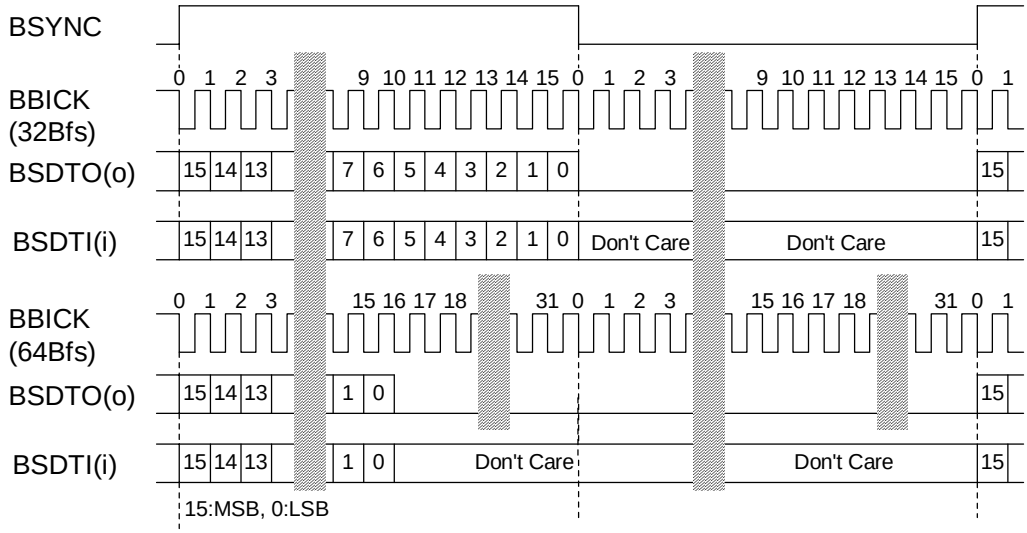


Figure 19. Timing of MSB justified

(4) I^2S

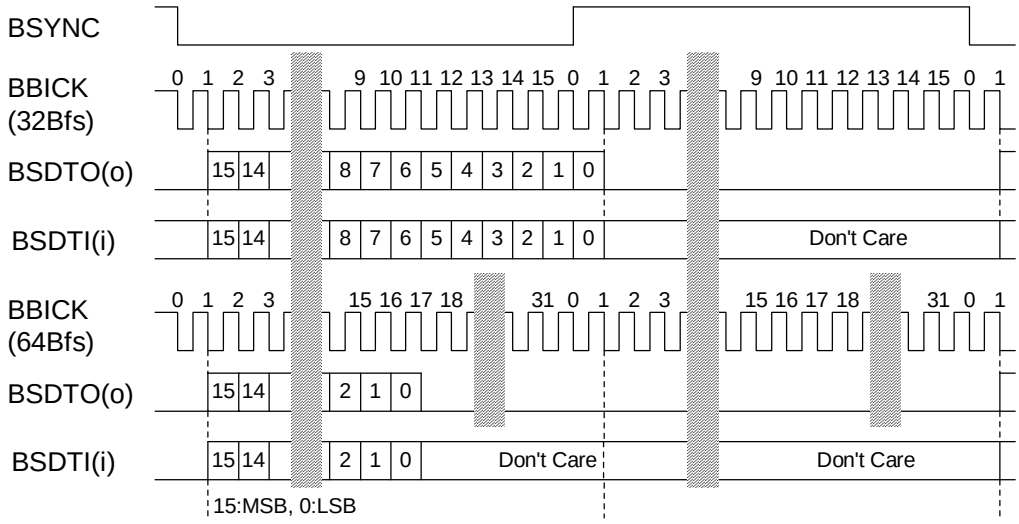


Figure 20. Timing of I^2S

■ Digital High Pass Filter

The ADC of Stereo CODEC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 3.4Hz (@fs=44.1kHz) and scales with sampling rate (fs).

The ADC of Mono CODEC also has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 0.62Hz (@Bfs=8kHz) and scales with sampling rate (Bfs).

■ MIC Input

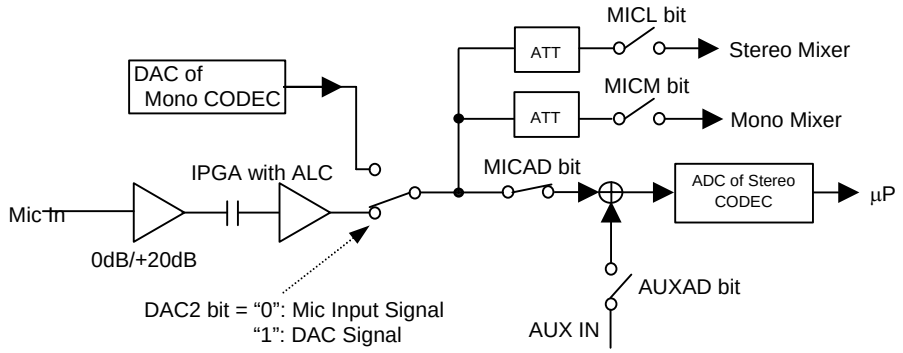


Figure 21. Microphone Input

The AK4641EN has the following functions for Mic Input.

(1) 1st MIC Amplifier of 20dB gain that can be selected ON/OFF by "MGAIN" bit.

(2) 2nd Amplifier that has PGA with ALC. This volume is controlled by "IPGA6-0" bit as Table 7.
While ALC is working, Master Clock must be present.
When Master Clock is not provided or PMMIC bit = "0", it is invalid to write to "IPGA6-0".

(3) Attenuator for stereo mixer. This volume is controlled by "ATTS2-0" bit as Table 8.

(4) Attenuator for mono mixer. This attenuator level is 4dB and this ON/OFF is controlled by "ATTM" bit.

IPGA6-0	GAIN (dB)	STEP	
47H	+27.5	0.5dB	
46H	+27.0		
45H	+26.5		
:	:		
36H	+19.0		
:	:		
10H	+0.0		Default
:	:		
06H	–5.0		
05H	–5.5		
04H	–6.0		
03H	–6.5		
02H	–7.0		
01H	–7.5		
00H	–8.0		

Table 7. Microphone Input Gain Setting

ATTS2-0	Attenuation	
7H	–6dB	
6H	–9dB	
5H	–12dB	Default
4H	–15dB	
3H	–18dB	
2H	–21dB	
1H	–24dB	
0H	–27dB	

Table 8. Attenuator Table

■ MIC Gain Amplifier

The AK4641EN has a Gain Amplifier for Microphone input. This gain is 0dB or +20dB, selected by the MGAIN bit. The typical input impedance is 30kΩ.

MGAIN bit	Input Gain	
0	0dB	
1	+20dB	Default

Table 9. Input Gain

■ MIC Power

The MPI and MPE pins supply power for the Microphone. These output voltages are 0.75 x AVDD (typ) and the load resistance is 2kΩ(min). No capacitor must be connected directly to MPI and MPE pins. MPWRI/MPWRE bit can control output from MPI and MPE pin.

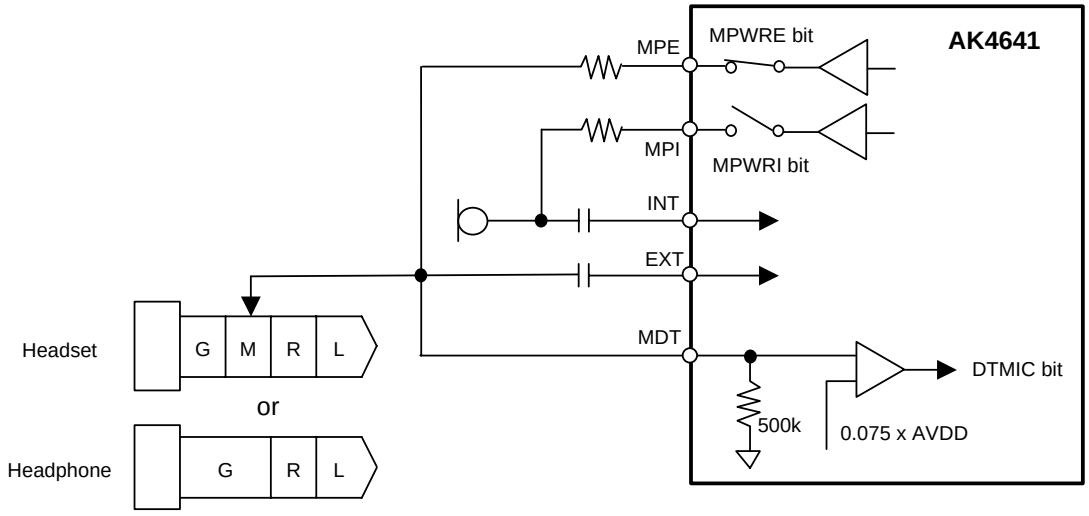


Figure 22. Microphone Power Supply and Mic Detection

■ MIC Detection Function

The AK4641EN includes the detection function of microphone. The external circuit is showed in Figure 22.

The followings show the example of external microphone detection sequence:
(1) MPWRE bit = "1".
(2) MPE drives external microphone.
(3) DTMIC bit is set as Table 10. In case of Headset, the input voltage of MDT pin is higher than 0.078 x AVDD because of the relationship between the bias resistance at MPE pin (typ. 2.2kΩ) and the microphone impedance. In case of Headphone, the input voltage of MDT pin is 0V because the pin of headphone jack connected to MDT pin is assigned as ground.

Input Level of DTM	DTMIC	Result
≥ 0.078 x AVDD	1	Mic (Headset)
< 0.050 x AVDD	0	No Mic (Headphone)

Table 10. Microphone Detection Result

■ Manual Mode

The AK4641EN becomes a manual mode at ALC1 bit = "0". This mode is used in the case shown below.

1. After exiting reset state, set up the registers for the ALC1 operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC1 operation (Limiter period, Recovery period and etc) are changed. For example; When the change of the sampling frequency.
3. When IPGA is used as a manual volume.

■ MIC-ALC Operation

The ALC (Automatic Level Control) of MIC input is done by ALC1 block when ALC1 bit is "1".

[1] ALC1 Limiter Operation

When the ALC1 limiter is enabled, and IPGA output exceeds the ALC1 limiter detection level (LMTH), the IPGA value is attenuated by the amount defined in the ALC1 limiter ATT step (LMAT1-0 bits) automatically.

When the ZELM bit = "1", the timeout period is set by the LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. If the ALC1 bit does not change into "0" after completing the attenuation, the attenuation operation repeats while the input signal level equals or exceeds LMTH.

When the ZELM bit = "0", the timeout period is set by the ZTM1-0 bits. This enables the zero-crossing attenuation function so that the IPGA value is attenuated at the zero-detect points of the waveform.

[2] ALC1 Recovery Operation

The ALC1 recovery refers to the amount of time that the AK4641EN will allow a signal to exceed a predetermined limiting value prior to enabling the limiting function. The ALC1 recovery operation uses the WTM1-0 bits to define the wait period used after completing an ALC1 limiter operation. If the input signal does not exceed the "ALC1 Recovery Waiting Counter Reset Level", the ALC1 recovery operation starts. The IPGA value increases automatically during this operation up to the reference level (REF6-0 bits). The ALC1 recovery operation is done at a period set by the WTM1-0 bits. Zero crossing is detected during WTM1-0 period, the ALC1 recovery operation waits WTM1-0 period and the next recovery operation starts.

During the ALC1 recovery operation, when input signal level exceeds the ALC1 limiter detection level (LMTH), the ALC1 recovery operation changes immediately into an ALC1 limiter operation.
In the case of "(Recovery waiting counter reset level) ≤ IPGA Output Level < Limiter detection level" during the ALC1 recovery operation, the wait timer for the ALC1 recovery operation is reset. Therefore, in the case of "(Recovery waiting counter reset level) > IPGA Output Level", the wait timer for the ALC1 recovery operation starts.

The ALC1 operation corresponds to the impulse noise. When the impulse noise is input, the ALC1 recovery operation becomes faster than a normal recovery operation.

[3] Example of ALC1 Operation

Table 11 shows the examples of the ALC1 setting. In case of this examples, ALC1 operation starts from 0dB.

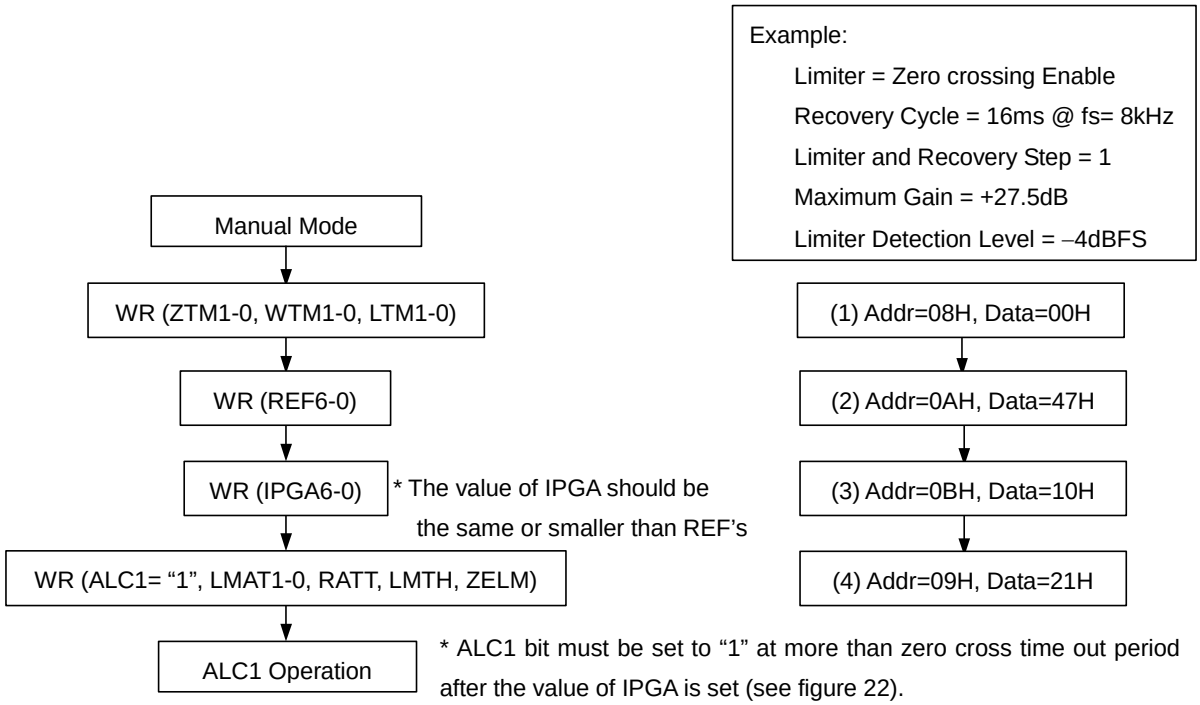
Register Name	Comment	fs=8kHz		fs=16kHz		fs=44.1kHz	
		Data	Operation	Data	Operation	Data	Operation
LMTH	Limiter detection Level	1	–4dBFS	1	–4dBFS	1	–4dBFS
LTM1-0	Limiter operation period at ZELM = 1	00	Don't use	00	Don't use	00	Don't use
ZELM	Limiter zero crossing detection	0	Enable	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	01	16ms	10	11.6ms
WTM1-0	Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits	00	16ms	01	16ms	10	11.6ms
REF6-0	Maximum gain at recovery operation	47H	+27.5dB	47H	+27.5dB	47H	+27.5dB
IPGA6-0	Gain of IPGA at ALC1 operation Start	10H	0dB	10H	0dB	10H	0dB
LMAT1-0	Limiter ATT Step	00	1 step	00	1 step	00	1 step
RATT	Recovery GAIN Step	0	1 step	0	1 step	0	1 step
ALC1	ALC1 Enable bit	1	Enable	1	Enable	1	Enable

Table 11. Example of the ALC1 setting

The following registers should not be changed during the ALC1 operation. These bits should be changed, after the ALC1 operation is finished by ALC1 bit = "0" or PMMIC bit = "0".

- **LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELM bits**

IPGA gain at ALC1 operation start can be changed from the default value of IPGA6-0 bits while PMMIC bit is "1" and ALC1 bit is "0". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set by ALC1 operation.



Note : WR : Write

Figure 23. Registers set-up sequence at ALC1 operation

[Setting timing of IPGA and ALC1 bits]

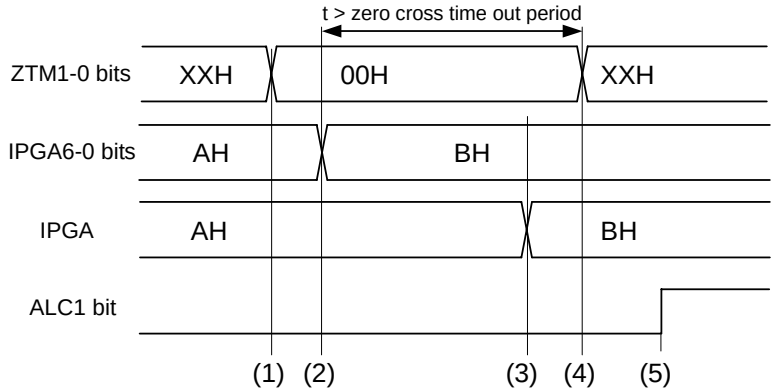


Figure 24. Setting timing of IPGA and ALC1 bits

(1) Set the zero cross time out period of IPGA as 128/fs: ZTM1-0 bits = "00". (Note)
(2) Set the IPGA value of ALC1 operation start by IPGA6-0 bits.
(3) The value of IPGA6-0 bits is reflected to actual gain at zero crossing or zero cross time out.
(4) Set the zero cross time out period of ALC1 operation by ZTM1-0 bits after the zero cross time out period set by (1).
(5) Set ALC1 bit to "1".

(Note) If ZTM1-0 bits are set to the value except for "00", ALC1 bit must be set to "1" after this zero cross time out period.

■ DAC of Stereo CODEC

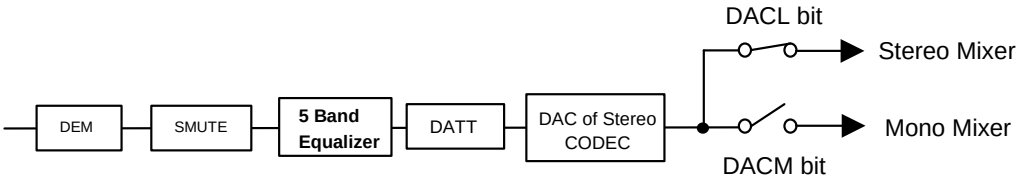


Figure 25. DAC block diagram of Stereo CODEC

The AK4641EN has the following functions for DAC of Stereo CODEC.
(1) 5 Band Equalizer
(2) Soft mute
(3) Digital Attenuator
(4) De-emphasis Filter (32kHz, 44.1kHz and 48kHz)

■ De-emphasis Filter

The AK4641EN includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 12. De-emphasis Control

■ Digital Attenuator

The AK4641EN has a channel-independent digital attenuator (256levels, 0.5dB step, Mute). The ATTL/R7-0 bits set the attenuation level of each channel (Table 13). When the DATTC bit = "1", the ATTL7-0 bits control both Lch and Rch attenuation levels. When the DATTC bit = "0", the ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level. This attenuator has a soft transition function. It takes around 1061/fs (24ms@44.1kHz) at TM bit = "0" and 256/fs (5.8ms@44.1kHz) at TM bit = "1" from 00H to FFH.

ATTL/R7-0	Attenuation	
00H	0dB	Default
01H	–0.5dB	
02H	–1.0dB	
03H	–1.5dB	
:	:	
:	:	
FDH	–126.5dB	
FEH	–127.0dB	
FFH	MUTE (–∞)	

Table 13. DATT Code Table

■ 5 Band Equalizer

The AK4641EN has 5 Band Equalizer before DAC of Stereo CODEC as shown in Figure 25.

The center frequencies and cut/boost amount are the followings.

- Center frequency: 100Hz, 250Hz, 1kHz, 3.5kHz, 10kHz (Note 25, Note 26)
- Cut/Boost amount: Minimum –10.5dB, Maximum +12dB, Step 1.5dB

Note 25: These are the frequencies when the sampling frequency is 44.1kHz. These frequencies are proportional to the sampling frequency.
Note 26: 100Hz is not center frequency but the frequency component lower than 100Hz is controlled.
Note 27: 10kHz is not center frequency but the frequency component higher than 10kHz is controlled.

EQ5 bit controls ON/OFF of this Equalizer and these Boost amount are set by EQx3-0 bit as shown in Table 14.

EQA3-0: Select the boost level of 100Hz
EQB3-0: Select the boost level of 250Hz
EQC3-0: Select the boost level of 1kHz
EQD3-0: Select the boost level of 3.5kHz
EQE3-0: Select the boost level of 10kHz

EQx3-0	Boost amount	
0H	+12.0dB	
1H	+10.5dB	
2H	+9.0dB	
3H	+7.5dB	
:	:	
8H	0dB	Default
:	:	
DH	–7.5dB	
EH	–9.0dB	
FH	–10.5dB	

Table 14. Boost amount of 5 Band Equalizer

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by −∞ ("0") during the cycle set by the TM bit. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the digital attenuator level of ATTL/R7-0 bits during the cycle set by the TM bit. If the soft mute is cancelled within the cycle set by the TM bit after starting the operation, the attenuation is discontinued and returned to the digital attenuator level. The soft mute is effective for changing the signal source without stopping the signal transmission.

Table 15 shows the Soft Mute Time when the digital attenuator level is 0dB (ATTL/R7-0 bits = "0"). As the digital attenuator level is less than 0dB, the Soft Mute Time becomes shorter.

TM	Cycle	
0	1061/fs	Default
1	256/fs	

Table 15. Soft Mute Time Setting

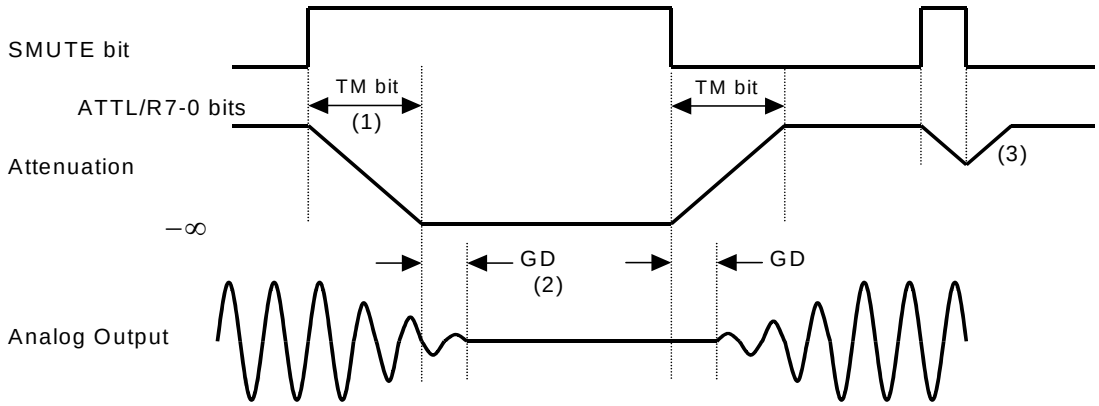


Figure 26. Soft Mute Function

NOTE:
(1) The output signal is attenuated until −∞ ("0") by the cycle set by the TM bit.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle of setting the TM bit, the attenuation is discounted and returned to 0dB(the set value).

■ AUX Input

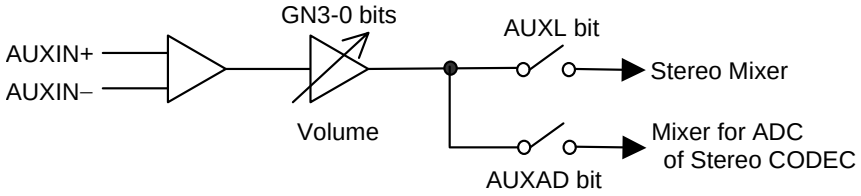


Figure 27. AUX Input

AUX input is differential input at AUXSI bit = "0" and single end input at AUXSI bit = "1". AUXIN+ pin should be used at single end input (AUXSI bit = "1"). The AK4641EN has a volume for AUX Input. This Volume is controlled by GN3-0 bits as shown in Table 16. The switching noise occurs when GN3-0 bits are changed.

GN3-0	GAIN (dB)	
FH	+24.0	
EH	+21.0	
DH	+18.0	
:	:	
7H	+0.0	Default
:	:	
2H	−15.0	
1H	−18.0	
0H	−21.0	

Table 16. AUX Input Gain Setting

■ STEREO LINE OUTPUT (LOUT and ROUT pins) and MONO LINE OUTPUT (MOUT2 pin)

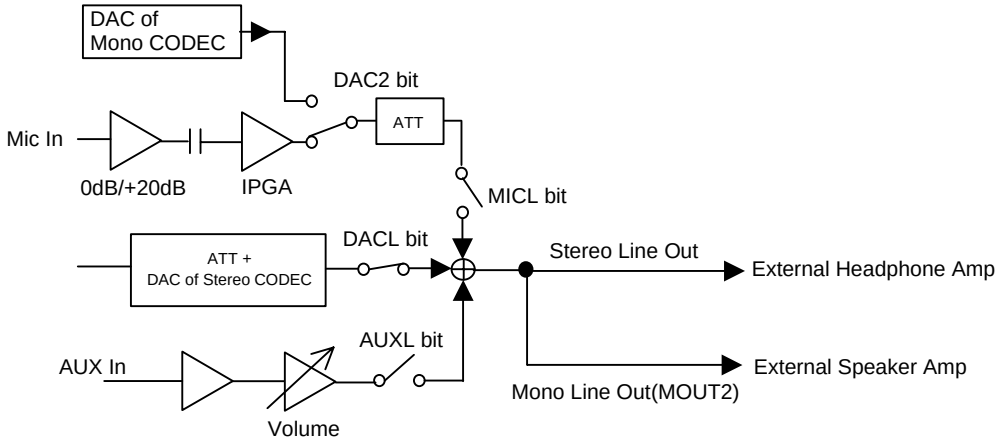


Figure 28. Stereo Line Output and Mono Line Out2

Line out path does not have volume but the attenuator of DAC of Stereo CODEC, volume of Mic In and AUX In control the output signal level. The AK4641EN does not have mute circuits to remove pop noise at power up and down for Line Output. The signal of the stereo mixer is converted to a mono signal [(L+R)/2] and this signal is output via MOUT2 pin.

■ MONO LINE OUTPUT (MOUT+/MOUT– pin)

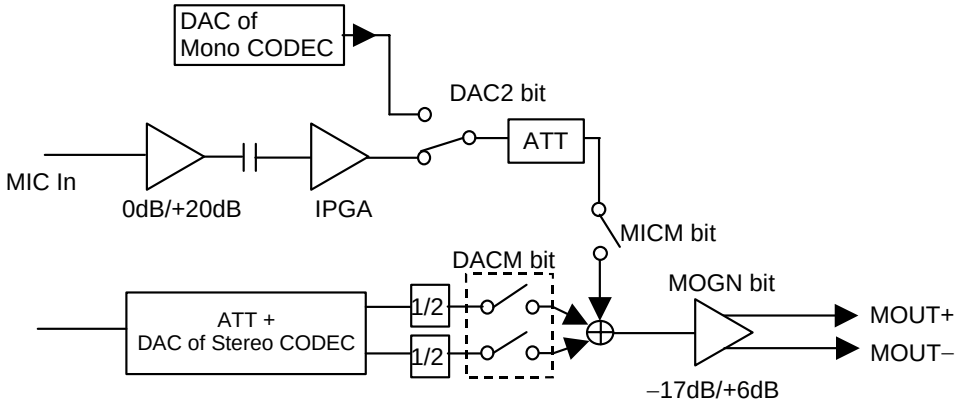


Figure 29. Mono Output

Mono mixer mixes signal from MIC In, Lch signal and Rch signal from DAC of Stereo CODEC. This mixed signal is output from the MOUT+ and MOUT– pins by differential output. Amp for mono output has 6dB gain and –17dB gain that are set by the MOGN bit.

■ 16bit Mono CODEC for Bluetooth I/F

The AK4641EN has the 16bit Mono CODEC to connect with Bluetooth Module that supports 8kHz to 16kHz sample rate. The AK4641EN includes PLL that generate the master clock for Mono CODEC from input BSYNC signal. The PLL should be powered-up after BSYNC signal is inputted. The PLL needs 90ms (max) lock time, when the PLL is powered-up (PMBIF bit = "0" → "1") and BSYNC is input. PMDA2 bit should be set to "0" or "0" data should be input to DAC of Mono CODEC during 90ms after PMBIF bit is set to "1".

BBICK and BSYNC should always be present when either ADC or DAC of Mono CODEC is power-up. If these clocks are not provided, the AK4641EN may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If BBICK or BSYNC is not present, ADC and DAC of Mono CODEC should be in the power-down mode.

ADC

The ADC of Mono CODEC outputs the signal from DAC of Stereo CODEC, Mic In and AUX In. The ADC of Mono CODEC enters an initialization cycle that starts when the PMAD2 bit is changed from "0" to "1". The initialization cycle time is 1057/Bfs, or 132ms@Bfs=8kHz. During the initialization cycle, the ADC digital data output of Mono CODEC are forced to a 2's compliment, "0". The ADC output of Mono CODEC reflects the analog input signal after the initialization cycle is complete.

- ADC full Scale Level: 0.6*AVDD [Vpp](1.98Vpp@3.3V)
  Full Scale level of ADC of Mono CODEC is the same as that of DAC of Stereo CODEC.

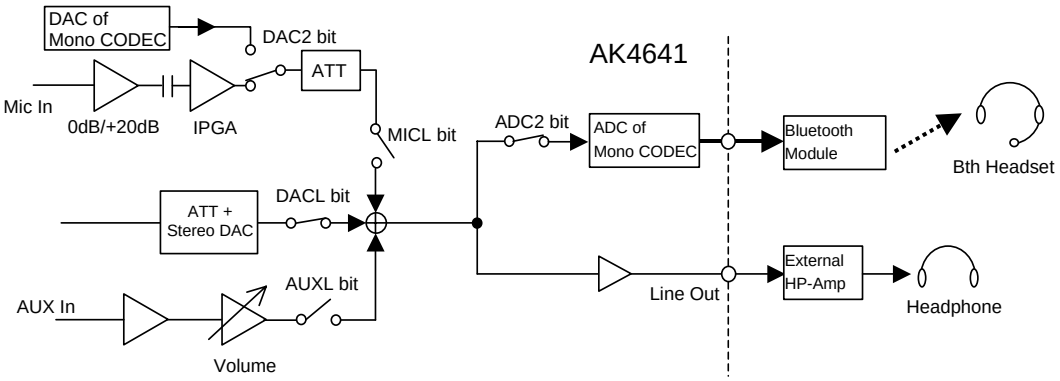


Figure 30. Path to ADC of Mono CODEC

DAC

The signal that is output from DAC of Mono CODEC is sent to Line Out, Mono Out and ADC of Stereo CODEC.

- DAC full Scale Level: 0.6*AVDD [Vpp](1.98Vpp@3.3V)
  Full Scale level of DAC of Mono CODEC is the same as that of ADC of Stereo CODEC.

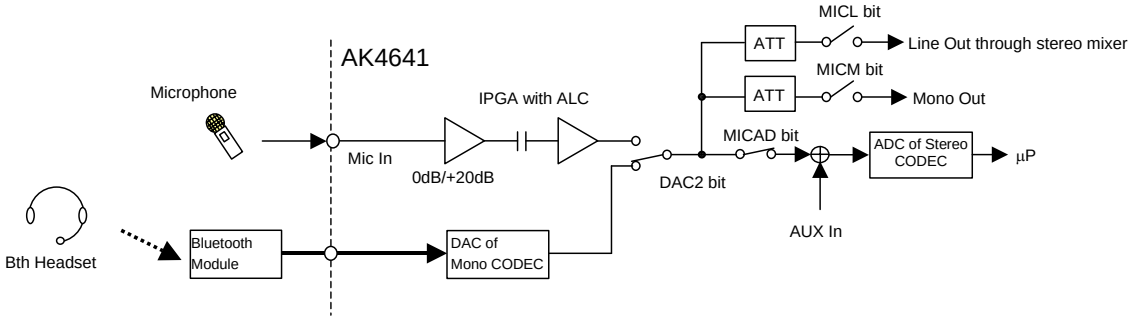


Figure 31. Path from DAC of Mono CODEC

■ I²C-bus Control Interface

The AK4641EN supports the fast-mode I²C-bus (max: 400kHz).

1. WRITE Operations

Figure 32 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 38). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010010". If the slave address matches that of the AK4641EN, the AK4641EN generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 39). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4641EN. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 34). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 35). The AK4641EN generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 38).

The AK4641EN can perform more than one byte write operation per sequence. After receipt of the third byte the AK4641EN generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 40) except for the START and STOP conditions.

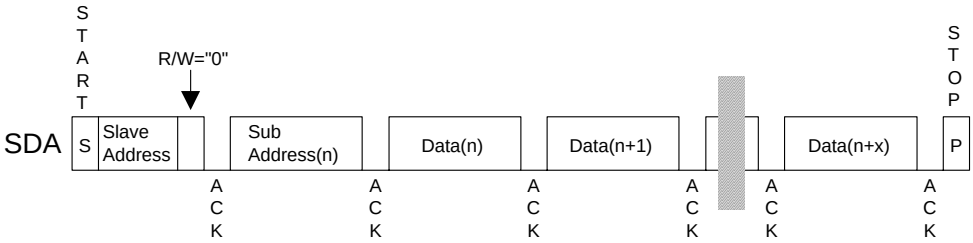


Figure 32. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	1	0	R/W

Figure 33. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 34. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 35. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK4641EN. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of generating a stop condition after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1FH prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The AK4641EN supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4641EN contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to “1”, the AK4641EN generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4641EN ceases transmission.

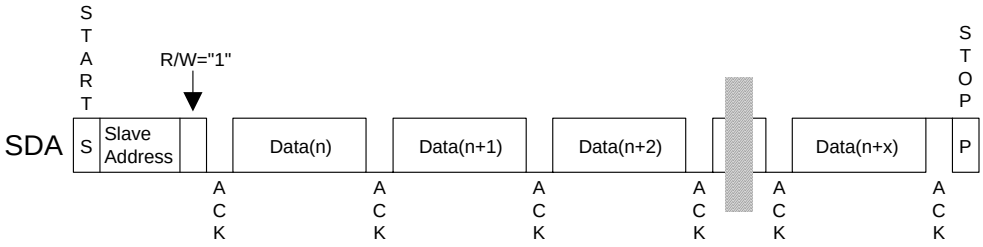


Figure 36. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to “1”. The AK4641EN then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4641EN ceases transmission.

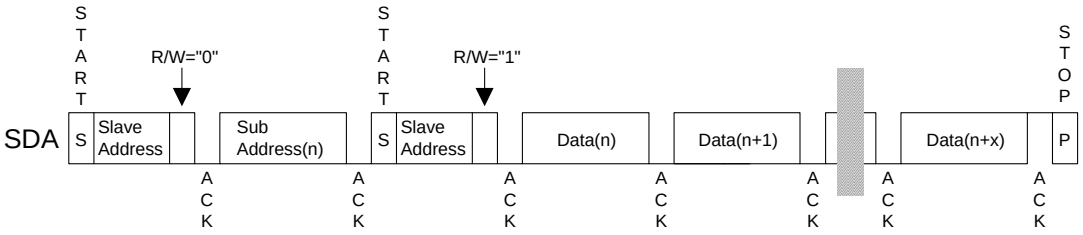


Figure 37. RANDOM ADDRESS READ

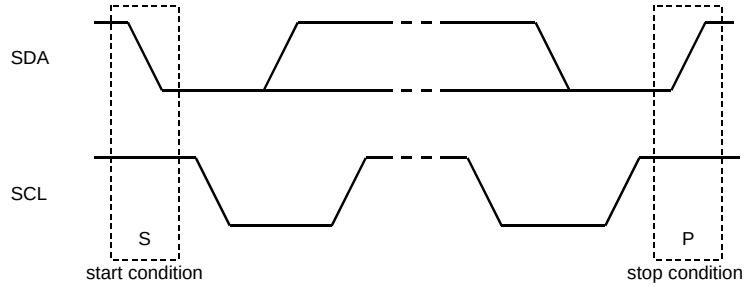


Figure 38. START and STOP Conditions

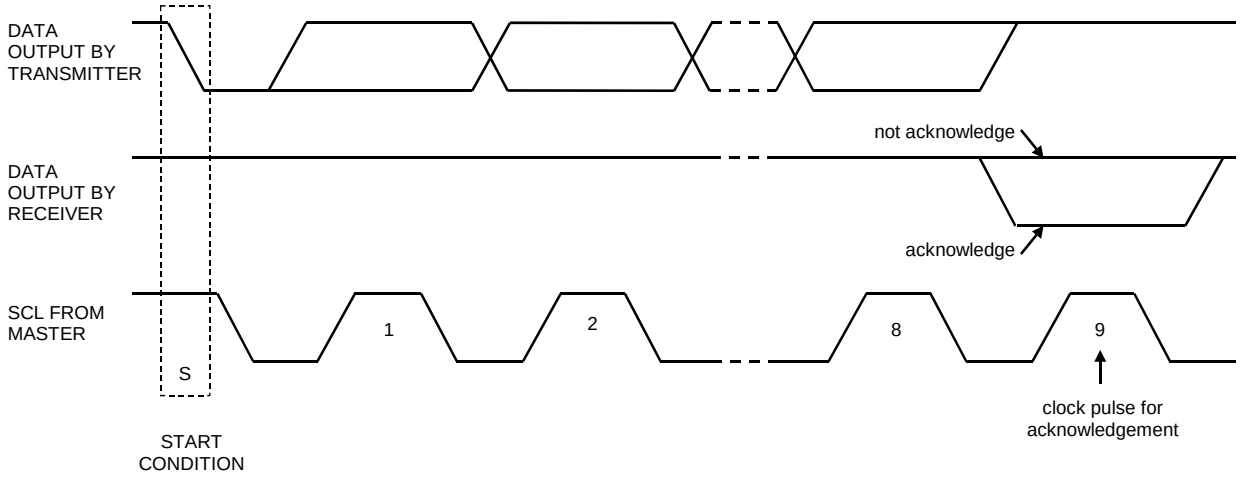


Figure 39. Acknowledge on the I^2C-Bus

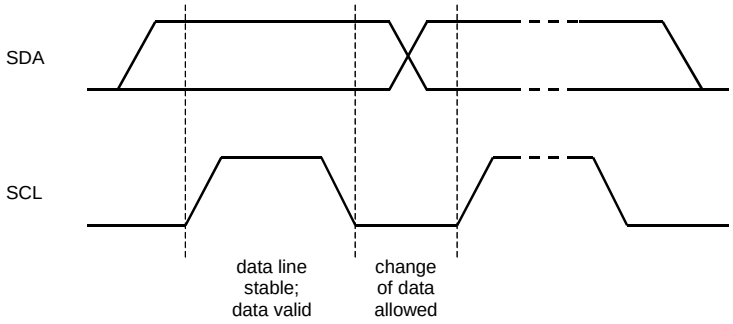


Figure 40. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMVCM	0	0	PMLO	PMMO	PMAUX	PMMIC	PMADC
01H	Power Management 2	MCKPD	0	0	MCKAC	PMMO2	0	0	PMDAC
02H	Signal Select1	MOGN	PSMO	DACM	MICM	0	0	0	PSMO2
03H	Signal Select2	DACL	0	AUXL	MICL	0	AUXSI	PSLOL	PSLOR
04H	Mode Control 1	0	0	0	0	0	0	DIF1	DIF0
05H	Mode Control 2	0	MCK1	MCK0	0	0	HPM	LOOP	0
06H	DAC Control	0	TM	SMUTE	DATTC	0	EQ	DEM1	DEM0
07H	MIC Control	0	0	AUXAD	MPWRE	MPWRI	MICAD	MSEL	MGAIN
08H	Timer Select	0	0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
09H	ALC Mode Control 1	0	0	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
0AH	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0BH	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
0CH	Lch Digital ATT Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0DH	Rch Digital ATT Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
0EH	Volume Control	ATTM	ATTS2	ATTS1	ATTS0	GN3	GN2	GN1	GN0
0FH	Status	0	0	0	0	0	0	0	DTMIC
10H	EQ Control 250Hz/100Hz	EQB3	EQB2	EQB1	EQB0	EQA3	EQA2	EQA1	EQA0
11H	EQ Control 3.5kHz/1kHz	EQD3	EQD2	EQD1	EQD0	EQC3	EQC2	EQC1	EQC0
12H	EQ Control 10kHz	0	0	0	0	EQE3	EQE2	EQE1	EQE0
13H	BT I/F CODEC Control	0	BTFMT1	BTFMT0	DAC2	ADC2	PMBIF	PMDA2	PMAD2

*PDN pin = “L” resets the registers to their default values.
*Unused bits must contain a “0” value.
*Only write to address 00H to 13H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMVCM	0	0	PMLO	PMMO	PMAUX	PMMIC	PMADC
R/W		R/W	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADC: ADC Block of Stereo CODEC Power Control
0: Power down (Default)
1: Power up
When PMADC bit changes from "0" to "1", initializing cycle (2081/fs=47.2ms@44.1kHz) starts. After initializing cycle, digital data of the ADC of Stereo CODEC is output.

PMMIC: MIC In Block Power Control
0: Power down (Default)
1: Power up

PMMO: Mono Out Power Control
0: Power down (Default)
1: Power up

PMLO: Line Out Power Control
0: Power down (Default)
1: Power up

PMAUX: AUX In Power Control
0: Power down (Default)
1: Power up

PMVCM: VCOM Block Power Control
0: Power down (Default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	MCKPD	0	0	MCKAC	PMMO2	0	0	PMDAC
R/W		R/W	RD	RD	R/W	R/W	RD	RD	R/W
Default		1	0	0	0	0	0	0	0

PMDAC: DAC Block of Stereo CODEC Power Control
0: Power down (Default)
1: Power up

PMMO2: Mono Out2 Power Control
0: Power down (Default)
1: Power up

MCKAC: Master Clock input Mode Select
0: C-MOS input (Default)
1: AC-Coupling input

MCKPD: MCLK Input Buffer Control
0: Enable
1: Disable (Default)
When MCLK input with AC coupling is stopped, MCKPD bit should be set to "1".
ADC and DAC of 16bit Stereo CODEC are powered-down at MCKPD bit = "1".

Note) The stereo mixer block (PMMIX) is powered down automatically.
PMLO=PMMO2=PMAD2 bits = "0": Power Down
Others: Power Up

Each block can be powered down respectively by writing "0" in each bit. When the PDN pin is "L", all blocks are powered down.

When all bits except MCKPD bit are "0" in the 00H and 01H addresses, all blocks are powered down. The register values remain unchanged. IPGA gain is reset when PMMIC bit is "0" (refer to the IPGA6-0 bits description).

When any of the blocks are powered up, the PMVCM bit must be set to "1".

MCLK, BICK and LRCK must always be present unless PMMIC=PMADC=PMDAC bits = "0" or PDN pin = "L".

BBICK and BSYNC must always be present unless PMAD2=PMDA2=PMBIF bits = "0" or PDN pin = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select1	MOGN	PSMO	DACM	MICM	0	0	0	PSMO2
R/W		R/W	R/W	R/W	R/W	RD	RD	RD	R/W
Default		0	0	0	0	0	0	0	0

PSMO2: Select mono output 2 of MOUT2 pin (Mixing = (L+R)/2)
0: Power Save Mode. Output VCOM voltage. (Default)
1: Normal Operation
(Note) Hi-Z is output at PMMO2 bit = “0”.

MICM: Switch Control from Mic In to Mono Mixer
0: OFF (Default)
1: ON

DACM: Switch Control from DAC of Stereo CODEC to Mono Mixer (Mixing = (L+R)/2)
0: OFF (Default)
1: ON

PSMO: Select mono output of MOUT+/– pins
0: Power Save Mode. Output VCOM voltage. (Default)
1: Normal Operation
(Note) Hi-Z is output at PMMO bit = “0”.

MOGN: Gain control for mono output
0: +6dB (Default)
1: –17dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select2	DACL	0	AUXL	MICL	0	AUXSI	PSLOL	PSLOR
R/W		R/W	RD	R/W	R/W	RD	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

PSLOR: Select Rch Line output of ROUT pin
0: Power Save Mode. Output VCOM voltage. (Default)
1: Normal Operation
(Note) Hi-Z is output at PMLO bit = “0”.

PSLOL: Select Lch Line output of LOUT pin
0: Power Save Mode. Output VCOM voltage. (Default)
1: Normal Operation
(Note) Hi-Z is output at PMLO bit = “0”.

MICL: Switch Control from Mic In to Stereo Mixer
0: OFF (Default)
1: ON

AUXL: Switch Control from AUX IN to Stereo Mixer
0: OFF (Default)
1: ON

DACL: Switch Control from DAC of Stereo CODEC to Stereo Mixer
0: OFF
1: ON (Default)

AUXSI: Select AUX Input
0: Differential Input (Default)
1: Single-ended Input. AUXIN+ pin is used for AUX input and AUXIN– pin is not available.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	0	0	0	0	0	0	DIF1	DIF0
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Digital Audio Interface Format Select (See Table 5.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	0	MCK1	MCK0	0	0	HPM	LOOP	0
R/W		RD	R/W	R/W	RD	RD	R/W	R/W	RD
Default		0	0	0	0	0	0	0	0

LOOP: Loopback ON/OFF
0: OFF (Default)
1: ON
ADC output data of Stereo CODEC is inputted to both Lch and Rch of DAC of Stereo CODEC.

HPM: Mono output select from DAC of Stereo CODEC
0: Stereo (Default)
1: Mono. (L+R)/2 signal is output from Lch and Rch of DAC of Stereo CODEC

MCK1-0: Input Master Clock Select (See Table 2.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DAC Control	0	TM	SMUTE	DATTC	0	EQ	DEM1	DEM0
R/W		RD	R/W	R/W	R/W	RD	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

DEM1-0: De-emphases response (See Table 12.)

EQ: Select 5 Band Equalizer.
0: OFF (Default)
1: ON

DATTC: DAC of Stereo CODEC Digital Attenuator Control Mode Select
0: ATTL6-0 and ATTR6-0 bits control attenuator level of Lch and Rch respectively.
1: ATTL6-0 bits control both Lch and Rch at same time. (Default)
When DATTC bit = "1", the value of ATTR6-0 does not change.

SMUTE: Soft Mute Control
0: Normal Operation (Default)
1: DAC outputs of Stereo CODEC soft-muted

TM: Soft Mute and DATT Transition Time Select (See Table 15.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	MIC Control	0	0	AUXAD	MPWRE	MPWRI	MICAD	MSEL	MGAIN
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	1

MGAIN: 1st Mic Amp Gain control
0: OFF. 0dB
1: ON. +20dB (Default)

MSEL: Microphone select
0: Internal Mic (Default)
1: External Mic

MICAD: Switch Control from Mic In to ADC of Stereo CODEC
0: OFF
1: ON (Default)

MPWRI: Power Supply Control for Internal Microphone
0: OFF (Default)
1: ON

MPWRE: Power Supply for External Microphone
0: OFF (Default)
1: ON

AUXAD: Switch Control from AUX In to ADC of Stereo CODEC
0: OFF (default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Timer Select	0	0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LTM1-0: ALC1 limiter operation period at zero crossing disable (ZELM bit = "1")
The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by LTM1-0 bits.

LTM1	LTM0		ALC1 Limiter Operation Period			
			8kHz	16kHz	44.1kHz	
0	0	0.5/fs	63μs	31μs	11μs	Default
0	1	1/fs	125μs	63μs	23μs	
1	0	2/fs	250μs	125μs	45μs	
1	1	4/fs	500μs	250μs	91μs	

Table 17. ALC1 Limiter Operation Period at zero crossing disable (ZELM bit = "1")

WTM1-0: ALC1 Recovery Waiting Period
WTM1-0 bits set a period of recovery operation when any limiter operation does not occur during ALC1 operation. When the output signal level exceeds auto recovery waiting counter reset level set by LMTH bit, the auto recovery waiting counter is reset. The waiting timer starts when the output signal level becomes below the auto recovery waiting counter reset level.

WTM1	WTM0		ALC1 Recovery Operation Waiting Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 18. ALC1 Recovery Operation Waiting Period

ZTM1-0: Zero crossing timeout at the write operation by μP, ALC1 recovery operation and zero crossing enable (ZELM bit = "0") of the ALC1 operation
When IPGA of each L/R channels perform zero crossing or timeout independently, the IPGA value is changed by μP WRITE operation or ALC1 recovery operation or ALC1 limiter operation (ZELM bit = "0").

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 19. Zero Crossing Timeout Period

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	ALC Mode Control 1	0	0	ALC1	ZELM	LMAT1	LMAT0	RATT	LMTH
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

The ALC1 limiter detection level and the ALC1 recovery counter reset level may be offset by about ±2dB.

LMTH	ALC1 Limiter Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	ADC Input ≥ –6.0dBFS	–6.0dB > ADC Input ≥ –8.0dBFS	Default
1	ADC Input ≥ –4.0dBFS	–4.0dB > ADC Input ≥ –6.0dBFS	

Table 20. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC1 Recovery GAIN Step

During the ALC1 Recovery operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is "30H" and RATT bit = "1" is set, IPGA changes to "32H" by the ALC1 recovery operation, the output signal level is gained up by 1dB (=0.5dB x 2).

When the IPGA value exceeds the reference level (REF6-0 bits), the IPGA value does not increase.

RATT	GAIN STEP	
0	1	Default
1	2	

Table 21. ALC1 Recovery Gain Step Setting

LMAT1-0: ALC1 Limiter ATT Step

During the ALC1 limiter operation, when either Lch or Rch exceeds the ALC1 limiter detection level set by LMTH, the number of steps attenuated from the current IPGA value is set. For example, when the current IPGA value is 47H and the LMAT1-0 bits = "11", the IPGA transition to "43H" when the ALC1 limiter operation starts, resulting in the input signal level being attenuated by 2dB (=0.5dB x 4). When the attenuation value exceeds IPGA = "00H" (–8dB), it clips to "00H".

LMAT1	LMAT0	ATT STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 22. ALC1 Limiter ATT Step Setting

ZELM: Enable zero crossing detection at ALC1 Limiter operation

0: Enable (Default)

1: Disable

When the ZELM bit = "0", the IPGA of each L/R channel perform a zero crossing or timeout independently and the IPGA value is changed by the ALC1 operation. The zero crossing timeout is the same as the ALC1 recovery operation. When the ZELM bit = "1", the IPGA value is changed immediately.

ALC1: ALC1 Enable

0: ALC1 Disable (Default)

1: ALC1 Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	1	1	0

REF6-0: Set the Reference value at ALC1 Recovery Operation

During the ALC1 recovery operation, if the IPGA value exceeds the setting reference value by gain operation, then the IPGA does not become larger than the reference value. For example, when REF6-0 bits = "30H", RATT = 2step, IPGA = "2FH", even if the input signal does not exceed the "ALC1 Recovery Waiting Counter Reset Level", the IPGA does not change to "2FH" + 2step = "31H", but keeps "30H". Default is "36H".

REF6-0	GAIN (dB)	STEP	
47H	+27.5		
46H	+27.0		
45H	+26.5		
:	:		
36H	+19.0		Default
:	:		
10H	+0.0		
:	:	0.5dB	
06H	–5.0		
05H	–5.5		
04H	–6.0		
03H	–6.5		
02H	–7.0		
01H	–7.5		
00H	–8.0		

Table 23. Setting Reference Value at ALC1 Recovery Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

IPGA6-0: Input Analog PGA (See Table 7.)

When IPGA gain is changed, IPGA6-0 bits should be written while PMMIC bit is "1" and ALC1 bit is "0". IPGA gain is reset when PMMIC bit is "0", and then IPGA operation starts from the default value when PMMIC is changed to "1". When ALC1 bit is changed from "1" to "0", IPGA holds the last gain value set by ALC1 operation. When IPGA6-0 bits are read, the register values written by the last write operation is read out regardless the actual gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Lch Digital ATT Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
0DH	Rch Digital ATT Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTL/R7-0: Digital ATT Output Control

These bits control the attenuation level of DAC output of Stereo CODEC. Step size of ATT is approximately 0.5dB (See Table 13).

Note) Even if DATTC bit = "1", ATTR7-0 bits are not changed when the ATTL7-0 bits are written.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Volume Control	ATTM	ATTS2	ATTS1	ATTS0	GN3	GN2	GN1	GN0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	1	1

GN3-0: Volume of AUX In (see Table 16.)

ATTS2-0: Attenuator select of signal from Mic IN to Stereo Mixer (See Table 8.)

ATTM: Attenuator control for signal from Mic IN to Mono Mixer
0: 0dB (Default)
1: –4dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Status	0	0	0	0	0	0	0	DTMIC
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

DTMIC: Microphone Detection Result
0: Microphone is not detected. (Default)
1: Microphone is detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	EQ Control 250Hz/100Hz	EQB3	EQB2	EQB1	EQB0	EQA3	EQA2	EQA1	EQA0
11H	EQ Control 3.5kHz/1kHz	EQD3	EQD2	EQD1	EQD0	EQC3	EQC2	EQC1	EQC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	EQ Control 10kHz	0	0	0	0	EQE3	EQE2	EQE1	EQE0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

EQA3-0: Select the boost level of 100Hz
EQB3-0: Select the boost level of 250Hz
EQC3-0: Select the boost level of 1kHz
EQD3-0: Select the boost level of 3.5kHz
EQE3-0: Select the boost level of 10kHz
See Table 14.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	BT I/F CODEC Control	0	BTFMT1	BTFMT0	DAC2	ADC2	PMBIF	PMDA2	PMAD2
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

PMAD2: ADC Block of Mono CODEC Power Control
0: Power down (Default)
1: Power up

PMDA2: DAC Block of Mono CODEC Power Control
0: Power down (Default)
1: Power up

PMBIF: 16bit Mono Interface and PLL Block Power Control
0: Power down (Default)
1: Power up
ADC and DAC of 16bit Mono CODEC are powered-down at PMBIF bit = “0”.

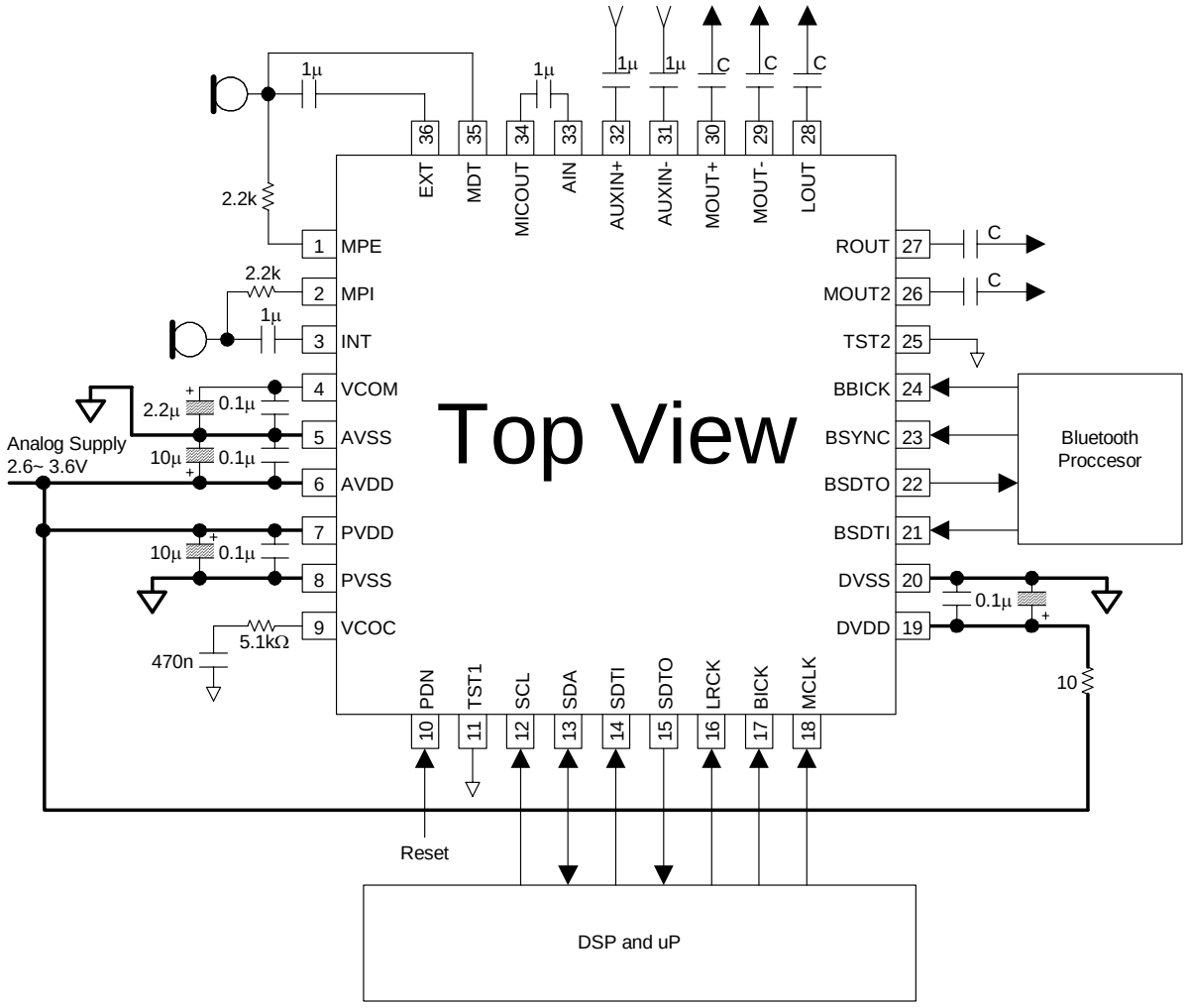
AD2: Select Signal that is input to ADC of 16bit Mono CODEC
0: OFF
1: ON (Default)

DAC2: Select DAC of Mono CODEC signal (See Figure 21.)
0: MIC Input Signal (Default)
1: DAC signal of Mono CODEC

BTFMT1-0: Digital Audio Interface Format Select for 16bit Mono CODEC (See Table 6.)

SYSTEM DESIGN

Figure 41 shows the system connection diagram for t the AK4641EN.



Notes:
- AVSS, DVSS and BVSS of the AK4641EN should be distributed separately from the ground of external controllers.
- Values of R and C in Figure 41 should depend on system.
- All digital input pins should not be left floating.

Figure 41. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4641EN requires careful attention to power supply and grounding arrangements. AVDD, DVDD and BVDD are usually supplied from the system's analog supply. If AVDD, DVDD and BVDD are supplied separately, the power up sequence is not critical. AVSS, DVSS and BVSS of the AK4641EN should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4641EN as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the AVDD and VCOM pins in order to avoid unwanted coupling into the AK4641EN.

3. Analog Inputs

The AK4641EN has the 16bit Mono CODEC to connect with Bluetooth Module that supports 8kHz to 16kHz sample rate. The AK4641EN includes PLL that generate the master clock for Mono CODEC from input BSYNC signal. The PLL should be powered-up after BSYNC signal is inputted. The PLL needs 90ms (max) lock time, when the PLL is powered-up (PMBIF bit = "0" → "1").

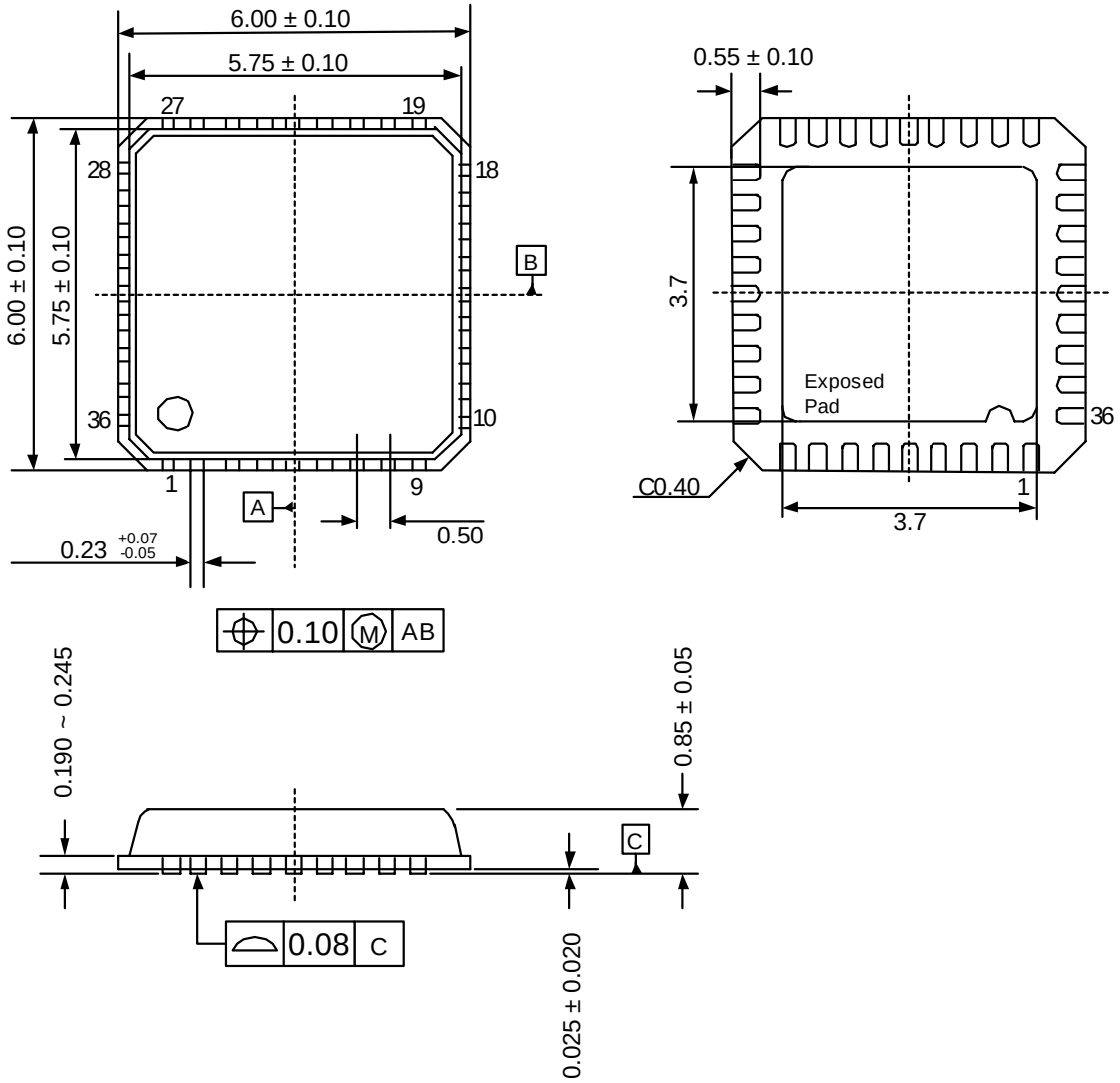
The Mic inputs are single-ended. AUX input is differential. The input signal range scales with nominally at 0.06 x AVDD Vpp for the Mic input, 0.6 x AVDD Vpp for AUX input, centered around the internal common voltage (0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = (1/2\pi RC)$. The AK4641EN can accept input voltages from AVSS to AVDD.

4. Analog Outputs

The input data format for the DAC of both Stereo and Mono CODEC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). Mono output from the MOUT2 pin, Mono Line Output from the MOUT+/MOUT– pins and Stereo Line Out from the LOUT/ROUT pins are centered at 0.45 x AVDD.

PACKAGE

● 36pin QFN (Unit: mm)

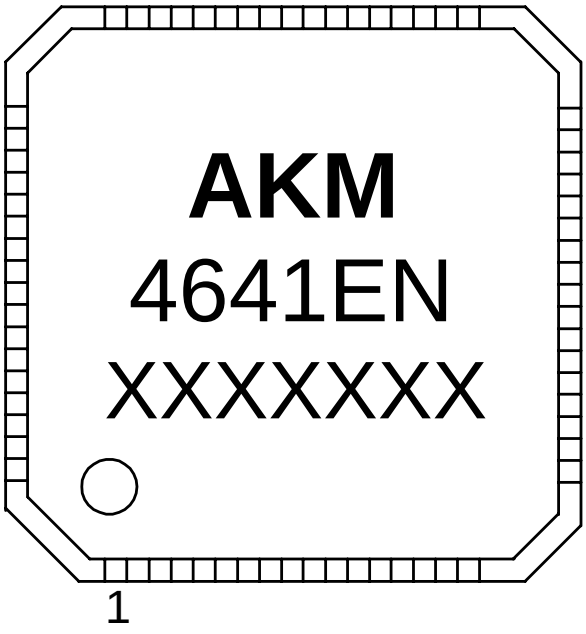


Note) The exposed pad on the bottom surface of the package must be open or connected to the grournd.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXX : Date code identifier (7 digits)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/02/22	00	First Edition		

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  a. A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  b. A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.