

# 2SK982

High Speed Switching Applications

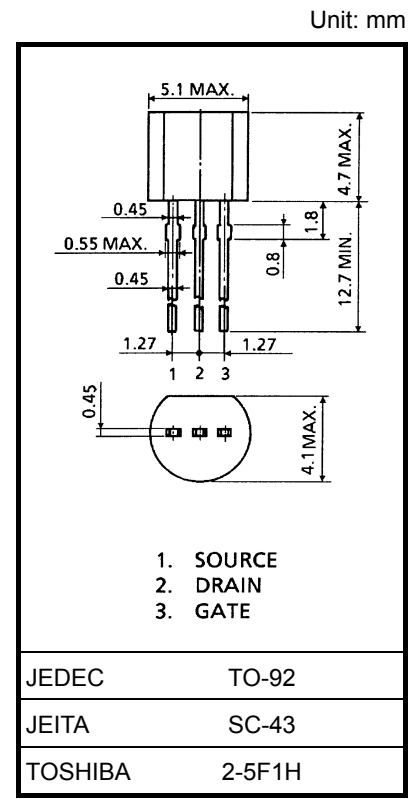
Analog Switch Applications

Interface Applications

- Excellent switching times:  $t_{on} = 14 \text{ ns (typ.)}$
- High forward transfer admittance:  $|Y_{fs}| = 100 \text{ mS (min)}$   
@  $I_D = 50 \text{ mA}$
- Low on resistance:  $R_{DS(ON)} = 0.6 \Omega \text{ (typ.) @ } I_D = 50 \text{ mA}$
- Enhancement-mode
- Complementary to 2SJ148

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DS}$	60	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$	200	mA
	Pulse	$I_{DP}$	800	
Drain power dissipation ( $T_a = 25^\circ\text{C}$ )		$P_D$	400	mW
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55~150	$^\circ\text{C}$



Weight: 0.21 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

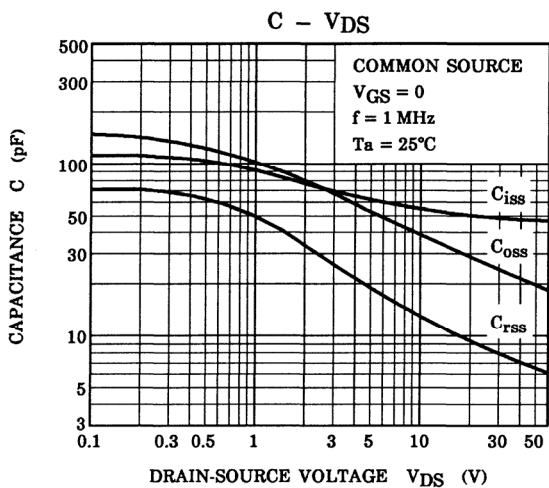
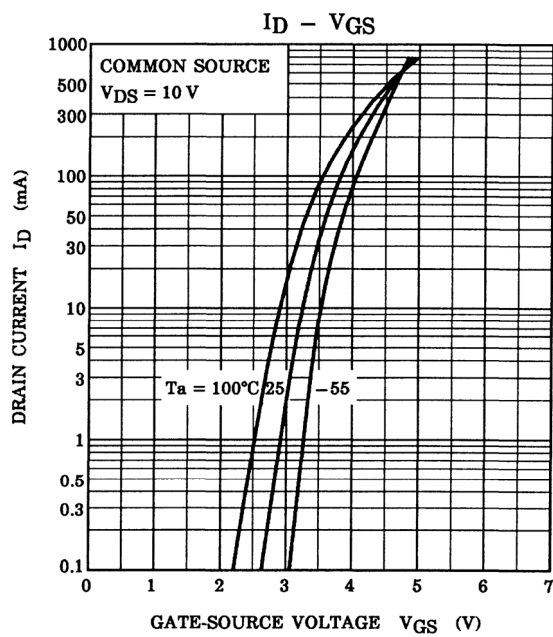
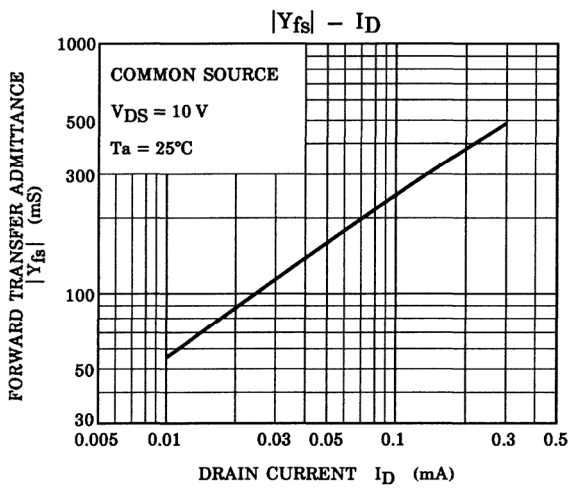
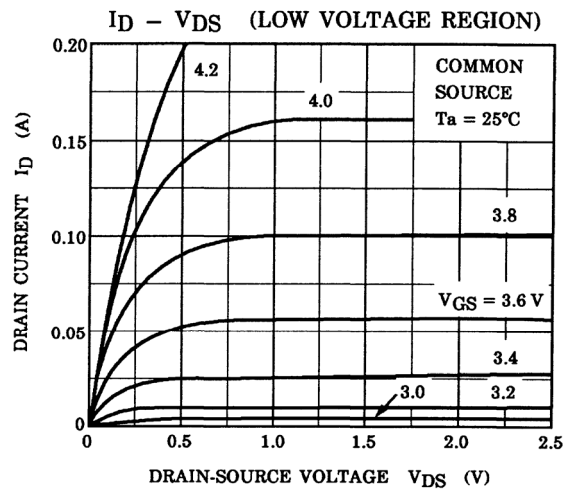
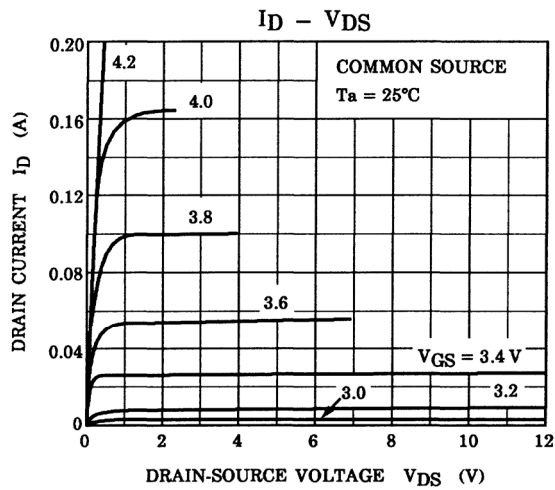
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

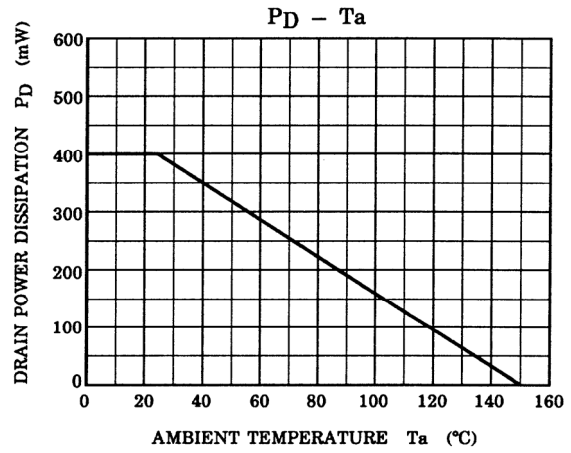
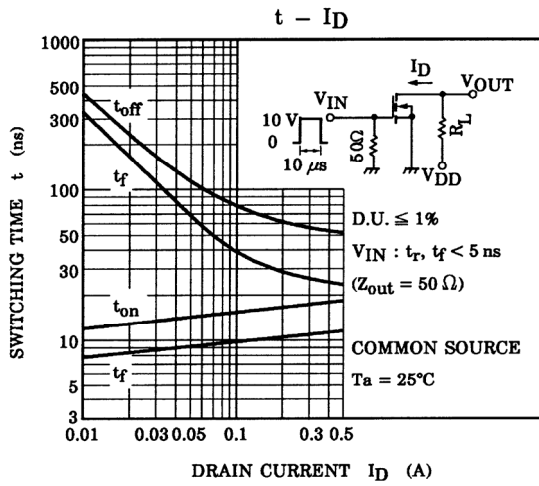
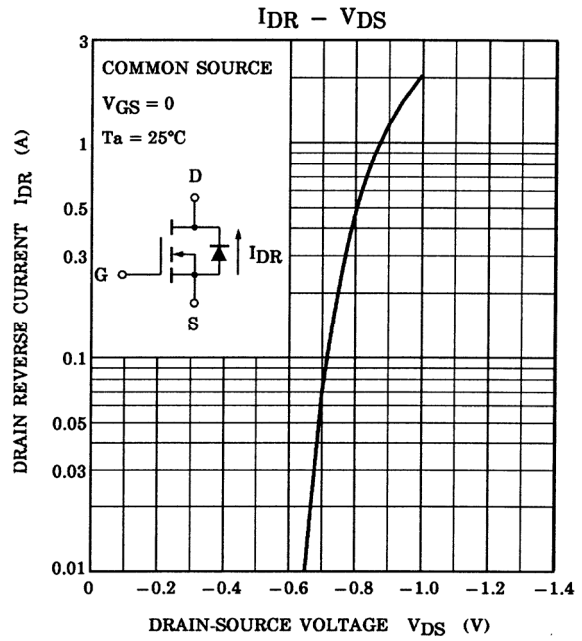
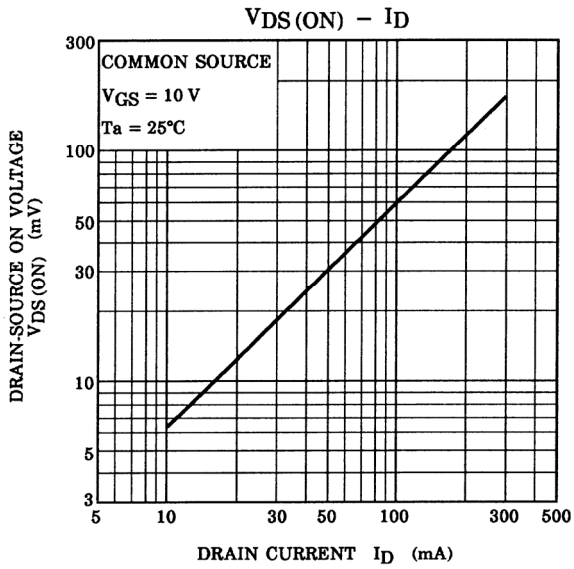
## Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = \pm 10\text{ V}, V_{DS} = 0$	—	—	$\pm 100$	nA
Drain cut-off current		$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0$	—	—	10	$\mu\text{A}$
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0$	60	—	—	V
Gate threshold voltage		$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2	—	3.5	V
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 50\text{ mA}$	100	—	—	mS
Drain-source ON resistance		$R_{DS(ON)}$	$I_D = 50\text{ mA}, V_{GS} = 10\text{ V}$	—	0.6	1.0	$\Omega$
Drain-source ON voltage		$V_{DS(ON)}$	$I_D = 50\text{ mA}, V_{GS} = 10\text{ V}$	—	30	50	mV
Input capacitance		$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	55	65	pF
Reverse transfer capacitance		$C_{rss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	13	18	pF
Output capacitance		$C_{oss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	40	50	pF
Switching time	Rise time	$t_r$		—	8	—	ns
	Turn-on time	$t_{on}$		—	14	—	
	Fall time	$t_f$		—	35	—	
	Turn-off Time	$t_{off}$		$V_{IN}; t_r, t_f < 5\text{ ns}$ $D.U \leq 1\% (Z_{out} = 50\ \Omega)$	—	75	

Note: This transistor is the electrostatic sensitive device.

Please handle with caution.





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20070701-EN GENERAL

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