TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (π -MOSVI)

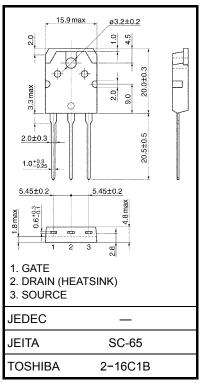
2SK3905

Switching Regulator Applications

- Low drain-source ON resistance: RDS (ON) = 0.25Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 8.2 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 100 \ \mu A (max) (V_{DS} = 500 \ V)$
- Enhancement model: $V_{th} = 2.0 \sim 4.0 \text{ V} (V_{DS} = 10 \text{ V}, \text{ID} = 1 \text{ mA})$

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-source voltage		V _{DSS}	500	V	
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V _{DGR}	500	V	
Gate-source voltage		V _{GSS}	±30	V	
Drain current	DC (Note 1)	I _D	17	А	
	Pulse (Note 1)	I _{DP}	68	A	
Drain power dissipat	ion (Tc = 25°C)	PD	150	W	
Single pulse avalanche energy (Note 2)		E _{AS}	816	mJ	
Avalanche current		I _{AR}	17	А	
Repetitive avalanche energy (Note 3)		E _{AR}	15	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	



Weight: 4.6 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Thermal Characteristics

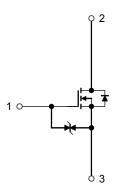
Characteristic	Symbol	Max	Unit	
Thermal resistance, channel to case	R _{th (ch-c)}	0.833	°C/W	
Thermal resistance, channel to ambient	R _{th (ch-a)}	50	°C/W	

Note 1: Ensure that the channel temperature does not exceed 150°C during use of the device.

Note 2: $V_{DD} = 90 \text{ V}, \text{ } T_{ch} = 25^{\circ}\text{C}, \text{ } L = 4.8 \text{ } \text{mH}, \text{ } R_{G} = 25 \Omega, \text{ } I_{AR} = 17 \text{ } \text{A}$

Note 3: Repetitive rating: pulse width limited by max junction temperature

This transistor is an electrostatic-sensitive device. Handle with care.



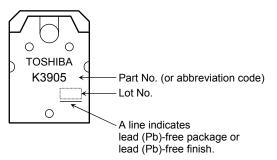
Electrical Characteristics (Ta = 25°C)

Char	acteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I _{GSS}	$V_{GS}=\pm 25~V,~V_{DS}=0~V$			±10	μA
Drain-source bre	akdown voltage	V (BR) GSS	$I_G=\pm 10~\mu\text{A},~V_{DS}=0~\text{V}$	±30	_	_	V
Drain cutoff curre	ent	I _{DSS}	$V_{DS} = 500 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	_	_	100	μA
Drain-source bre	akdown voltage	V (BR) DSS	$I_D=10\ mA,\ V_{GS}=0\ V$	500	_		V
Gate threshold ve	oltage	V _{th}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$	2.0	_	4.0	V
Drain-source ON	resistance	R _{DS (ON)}	$V_{GS} = 10 \ V, \ I_D = 8.5 \ A$	_	0.25	0.31	Ω
Forward transfer	admittance	Y _{fs}	$V_{DS} = 10 \ V, \ I_D = 8.5 \ A$	2.3	8.2	_	S
Input capacitance		C _{iss}	$V_{DS} = 25 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	_	3100	_	pF
Reverse transfer capacitance		C _{rss}		_	20	_	
Output capacitance		C _{oss}		_	270	_	
Switching time	Rise time	tr	$V_{GS}^{10 \text{ V}} \downarrow I_D = 8.5 \text{ A} \\ 0 \text{ V} \downarrow I_D = 8.5 \text{ A} \\ 0 \text{ V} \downarrow I_W = 10 \text{ A} \\ V_{DD} \simeq 200 \text{ V} \\ Duty \leq 1\%, t_W = 10 \mu\text{s}$		70		
	Turn-on time	t _{on}			130		
	Fall time	tf			70		ns
	Turn-off time	t _{off}		_	280	_	
Total gate charge (gate-source plus gate-drain)		Qg	$V_{DD}\simeq 400$ V, $V_{GS}=10$ V, $I_{D}=17$ A		62		nC
Gate-source charge		Q _{gs}		_	40	_	
Gate-drain ("Miller") charge		Q _{gd}			22		

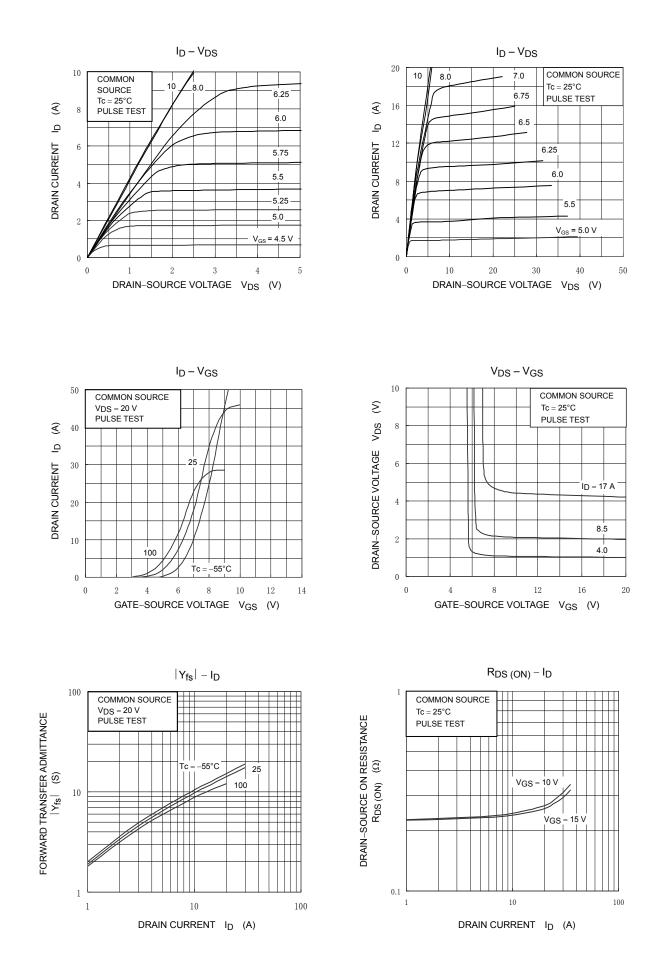
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	—	_		17	А
Pulse drain reverse current (Note 1)	I _{DRP}	—	_	_	68	А
Forward voltage (diode)	V _{DSF}	I _{DR} = 17 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 17 A, V _{GS} = 0 V,	_	1300	_	μS
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 100 A/μs		18		μC

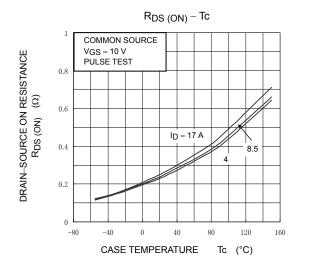
Marking

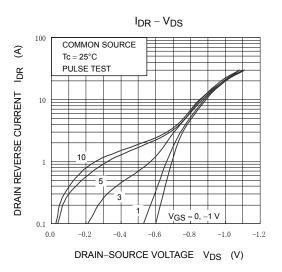


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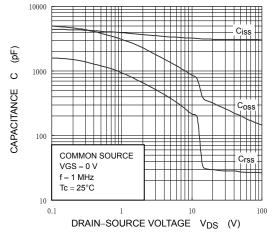


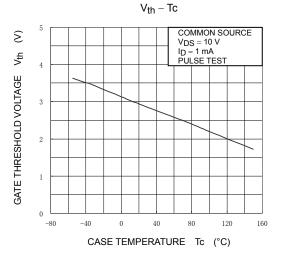
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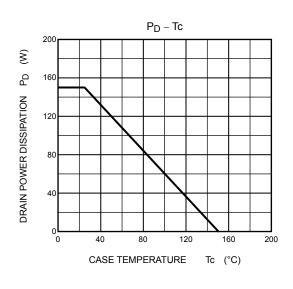




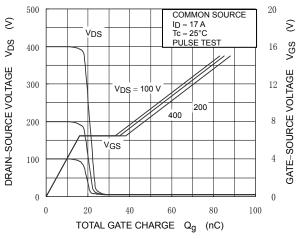
CAPACITANCE – V_{DS}

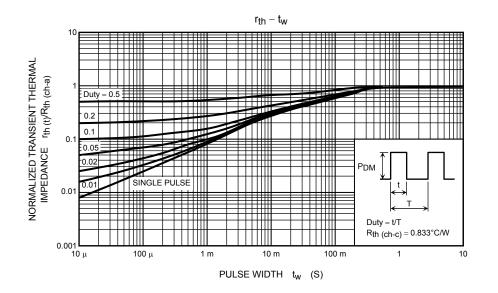






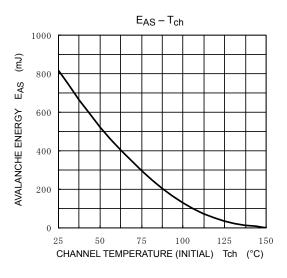
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

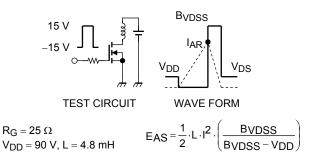




SAFE OPERATING AREA 100 ID max (PULSE) * E 10 DRAIN CURRENT ID ID max (CONTINUOUS) DC 1 $Tc = 25^{\circ}C$ 0.1 SINGLE NONPETITIVE PULSE $Tc = 25^{\circ}C$ Curves must be derated linearly with V_{DSS} max increase in temperature. 0.01 10 100 1000 1

DRAIN-SOURCE VOLTAGE VDS (V)





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20070701-EN

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