ZL30461

Compact Stratum 3 Timing Module

Data Sheet

December 2003

Features

- Meets requirements of Telcordia GR-253-CORE for SONET Stratum 3 clocks
- Meets requirements of Telcordia GR-1244-CORE for Stratum 3 clocks
- Meets requirements of G.813 Option 1 and 2 for SDH Equipment Clocks (SEC)
- 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz input reference frequencies
- Output clock frequencies from 8 kHz to 155.52 MHz
- Low intrinsic jitter and wander generation
- Selectable operation modes
- Alarm output indication

Ordering Information

ZL30461MGG 240 BGA

0°C to +70°C

Applications

- SONET/SDH Add/Drop multiplexers
- SONET/SDH up-links
- ATM edge switches
- Line cards

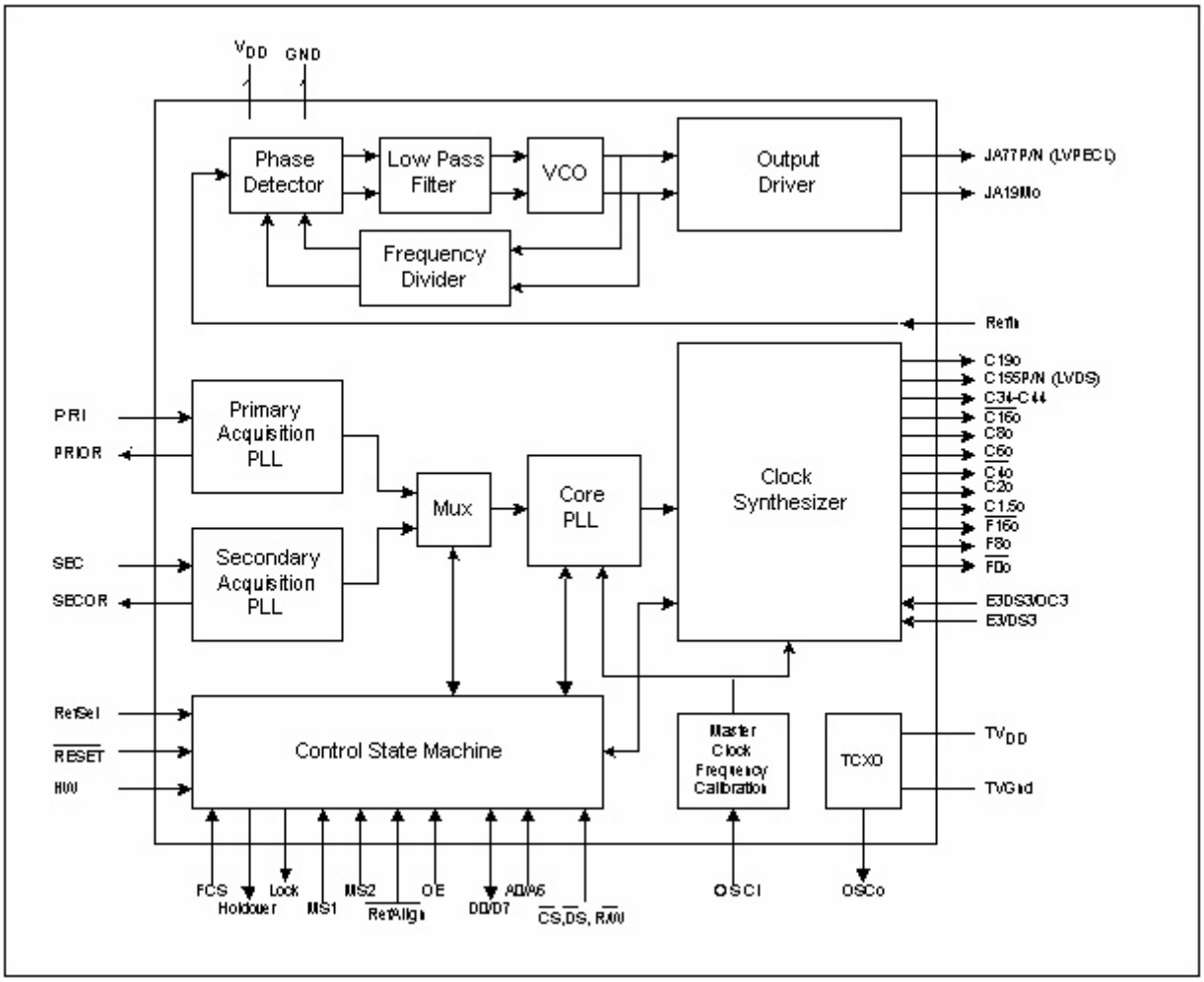


Figure 1 - Functional Block Diagram

Description

The ZL30461 is a Compact Timing Module, which functions as a complete system clock solution for general Stratum 3 and SONET/SDH timing applications.

The ZL30461 uses Zarlink's Digital and Analog Phase Locked Loop (DPLL and APLL) technology and can lock to 1 of 4 input frequencies automatically. The module has multiple output clocks ranging from 8 kHz to 155.52 MHz, its primary output at 77.76 MHz has low jitter performance at less than 40 ps (Pk to Pk). The availability of multiple clocks and features such as holdover and out-of-range detection enable the ZL30461 to be used on the master timing card as well as the linecard.

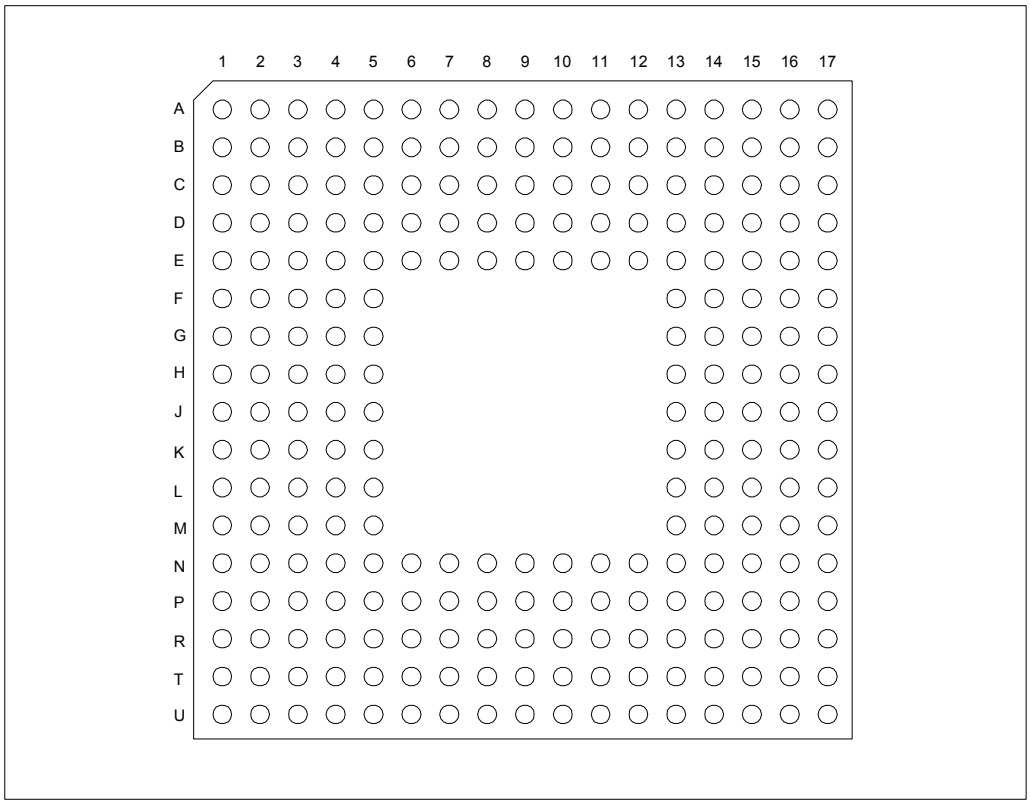


Figure 2 - 240 Pin BGA Top View

Note: All undefined pins must be left unconnected.

Pin Description

Ball # BGA	Name	Description
M1	PRI	**Primary Reference (Input)**. This input is a Primary reference source for synchronization. The module can synchronize to falling edge of the following reference clocks: 8 kHz, 1.544 MHz, 2.048 MHz or the rising edge of 19.44 MHz. This pin is selected when a logic 0 is applied to the RefSel input pin. This pin is internally pulled to V_{DD1}.

Pin Description (continued)

Ball # BGA	Name	Description
L1	SEC	**Secondary Reference (Input)**. This input is a Secondary reference source for synchronization. The module can synchronize to falling edge of the following reference clocks: 8 kHz, 1.544 MHz, 2.048 MHz or the rising edge of 19.44 MHz. This pin is selected when a logic 1 is applied to the RefSel input pin. This pin is internally pulled to V_{DD1}.
A10	PRIOR	**Primary Reference Rejection Range (Output)**. When used in Stratum 3 applications, a logic 1 at this output pin indicates that the Primary reference is off the PLL centre frequency by more than ±12 ppm. This threshold is relative to the accuracy of the 20 MHz master oscillator input OSCi.
B10	SECOR	**Secondary Reference Rejection Range (Output)**. When used in Stratum 3 applications, a logic 1 at this output pin indicates that the Primary reference is off the PLL centre frequency by more than ±12 ppm. This threshold is relative to the accuracy of the 20 MHz master oscillator input OSCi.
B15	RefSel	**Reference Source Select (Input)**. Logic 0 selects the PRI (Primary) reference source as the input reference signal and logic 1 selects the SEC (Secondary) input. The logic level at this input is sampled on the rising edge of F8o. This pin is internally pulled to GND.
A8	$\overline{\text{RESET}}$	**Reset (5 V tolerant Input)**. Logic 0 will forces the module into a reset state. This pin must be held to logic 0 for a minimum of 1 µs to reset the module properly. The module must be reset after power-up.
A11	LOCK	**Lock Indicator (Output)**. Logic 1 at this output indicates that the clock synthesizer outputs are locked to the selected input reference. Logic 0 indicates that the selected input reference has exceeded (or is close to) the core PLL frequency tracking range. This threshold is set at ±104 ppm and is relative to the accuracy of the 20 MHz master oscillator input OSCi.
A12	HOLDOVER	**Holdover Indicator (Output)**. Logic 1 at this output indicates that the module is in holdover.
B16	$\overline{\text{RefAlign}}$	**Reference Align (Input)**. A high to low transition at this input initiates phase realignment between the input reference and the generated output clocks. This pin is internally pulled to GND.
J1	MS1	**Mode Select 1 (Input)**. The MS1 and MS2 inputs select the module's mode of operation (normal, holdover or free-run), see Table 1 for details. The logic level at this input is sampled on the rising edge of the F8o frame pulse.
K1	MS2	**Mode Select 2 (Input)**. The MS2 and MS1 inputs select the module's mode of operation (normal, holdover or free-run), see Table 1 for details. The logic level at this input is sampled on the rising edge of the F8o frame pulse.
A9	OE	**Output Enable (Input)**. Logic 1 on this input enables C19o, $\overline{\text{F16o}}$, $\overline{\text{C16o}}$, C8o, C6o, $\overline{\text{C4o}}$, C2o, C1.5o, F8o and $\overline{\text{F0o}}$ signals. Logic 0 will force these output clocks pins into a high impedance state.
U8	JA19OE	**JA19Mo Output Enable (Input)**. Logic 1 on this input will enable the JA19Mo output clock and logic 0 will disable this it. **(Note 1)**
U10	JA77OE	**JA77P/N Output Enable (Input)**. Logic 1 on this input will enable the JA77P/N output clock and logic 0 will disable this it. **(Note 1)**
U5	JA19Mo	**JA 19.44 MHz Clock (Output)**. This output provides a low jitter 19.44 MHz clock.

Pin Description (continued)

Ball # BGA	Name	Description
K17 J17	JA77P JA77N	**JA 77.76 MHz Clock (LVPECL Output)**. This differential output provides a low jitter 77.76 MHz clock.
G2	$\overline{\text{F0o}}$	**Frame Pulse ST-BUS 2.048 Mbps (Output)**. This is an 8 kHz, 244 ns, active low framing pulse, which marks the beginning of a ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mbps and 4.096 Mbps.
H2	F8o	**Frame Pulse ST-BUS/GCI 8.192 Mbps (Output)**. This is an 8 kHz, 122 ns, active low framing pulse, which marks the beginning of a ST-BUS/GCI frame. This is typically used for ST-BUS/GCI operation at 8.192 Mbps.
E2	$\overline{\text{F16o}}$	**Frame Pulse ST-BUS 8.192 Mbps (Output)**. This is an 8 kHz, 61 ns, active low framing pulse, which marks the beginning of a ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mbps.
D17	C1.5o	**Clock 1.544 MHz (Output)**. This output provides a 1.544 MHz DS1 rate clock.
G1	C2o	**Clock 2.048 MHz (Output)**. This output provides a 2.048 MHz E1 rate clock, which can be used for ST-BUS operation at 2.048 Mbps.
F2	$\overline{\text{C4o}}$	**Clock 4.096 MHz (Output)**. This clock is used for ST-BUS operation at 4.096 Mbps.
D16	C6o	**Clock 6.312 MHz (Output)**. This output provides a 6.312 MHz DS2 rate clock.
F1	C8o	**Clock 8.192 MHz (Output)**. This clock is used for ST-BUS operation at 8.192 Mbps.
E1	$\overline{\text{C16o}}$	**Clock 16.384 MHz (Output)**. This clock is used for ST-BUS operation at 16.384 Mbps.
T11	C19o	**Clock 19.44 MHz (Output)**. This output provides a 19.44 MHz clock, which must be connected to the RefIn input.
T10	RefIn	**APLL Reference (Input)**. This is the input reference of the APLL circuitry and must be linked directly to the C19o output. **(Note 1)**
B17	C34-C44	**Clock 34.368 MHz / Clock 44.736 MHz (Output)**. This clock can provide several frequency outputs, depending on the status of the E3/DS3 and E3DS3/OC3 input pins, see Figure 4 for details.
R1 P1	C155P C155N	**Clock 155.52 MHz (LVDS Output)**. Differential outputs for a 155.52 MHz clock. These outputs are enabled by applying logic 0 to E3DS3/OC3 input or can be switched into high impedance state by applying logic 1 to E3DS3/OC3 input.
K2	E3DS3/$\overline{\text{OC3}}$	**E3DS3 or OC3 Selection Input**. Logic 0 on this pin enables the C155P/N outputs and enables the C34/C44 output to provide an 8.592 MHz or 11.184 MHz clock. Logic 1 at this input sets the C155P/N clock outputs into high impedance and enables C34/C44 outputs to provide 34.368 MHz or 44.736 MHz clock.
L2	E3/$\overline{\text{DS3}}$	**E3 or DS3 Selection (Input)**. When the E3DS3/OC3 pin is set to logic 1, a logic 0 on E3/DS3 pin selects a 44.736 MHz clock on C34/C44 output and logic 1 selects 34.368 MHz clock. When the E3DS3/OC3 pin is set to logic 0, a logic 0 on E3/DS3 pin selects 11.184 MHz clock on C34/C44 output and logic 1 selects 8.592 MHz clock.

Pin Description (continued)

Ball # BGA	Name	Description
D1	FCS	**Filter Selector (Input)**. Logic 0 on this pin sets the filter corner frequency to 1.5 Hz, this selection meets requirements of G.813 option 1 and GR-1244 Stratum 3 clocks. Logic 1 on this pin sets the filter corner frequency to 0.1 Hz, this selection meets requirements of G.813 option 2, GR-253 for SONET Stratum 3 and GR-253 for SONET Minimum Clocks (SMC).
A16	OSCo	**Oscillator Out (Output)**. This output provides access to the internal 20 MHz TCXO and will normally be connected to the OSCi pin.
A15	OSCi	**Oscillator In (Input)**. This is the master 20 MHz clock input pin and is normally connected directly to the OSCo (internal TXCO) pin. However, this input can be connected to an external 20 MHz reference if required. If an external reference is going to be used, then the TV_{DD}, TGND and OSCo pins should be left unconnected; this will save on power and reduce any unwanted noise.
A13, B13	TV_{DD}	**TCXO Positive Power Supply**
A14, B14, C13, C14, D10 - D15, E10 - E13	TGND	**TCXO Ground**
T14, U14	V_{CC}	**Positive Power Supply.** Note 1.
H1, J2,	V_{DD1}	**Positive Power Supply**
K4, K5, L4, L5, M4, M5,	V_{DD2}	**Positive Power Supply.** Note 1.
J3, K3	AV_{DD}	**Positive Power Supply**
F16, F17	$V_{CC}V_{CO}$	**Positive Power Supply.** Note 1.
N15, P15, T16, U16	V_{CPECL}	**Positive Power Supply.** Note 1.
H4, H5, J4, J5	AGND1	**Ground**
G13 - G16, H13 - H16, J13 - J16, K13 - K16, L13 - L16, M13 - M16, N8 - N14, N16, P8 - P14, P16, R8 - R16, T12, T13, T15, U12, U13, U15, U17	AGND2	**Ground**

Pin Description (continued)

Ball # BGA	Name	Description
C3 - C8, D3 - D9, E3 - E9, F3 - F5, G3 - G5, H3, N1 - N7, P2 - P7, R2, R3, T1, T2	DGND	**Ground**
B12, T6, T8, T9, U6, U7, U9, U11,T5	GC	**Ground Connections (Input).** Internal gates to be externally connected to DGND.
B7	HW	**Hardware/Software Control (Input).** If this input is tied to logic 0, then the module is controlled via the microprocessor port. If it is tied to logic 1, then the module is controlled via the control pins MS1, MS2, FCS, RefSel, /RefAlign, E3/DS3 and E3DS3/OC3.
B8	$\overline{CS}$	**Chip Select (5 V tolerant input).** This active low input enables the microprocessor interface. When this input is at logic 1, the microprocessor interface is idle and all Data Bus I/O pins will be in a high impedance state.
B9	$\overline{DS}$	**Data Strobe (5 V tolerant input).** This input is the active low data strobe of the processor interface.
A7	R/$\overline{W}$	**Read/Write Strobe (5 V tolerant input).** This input controls the direction of the Data Bus I/O during a microprocessor access. When the R/W input is logic 1, the processor is reading data from the State Control Machine. When logic 0, the processor is writing to the State Control Machine.
A2	A0	**Address 0 (5 V tolerant input).** Address input for the microprocessor interface. A0 is the least significant input.
A1	A1	**Address 1 (5 V tolerant input).** Address input A1 for the microprocessor interface.
B2	A2	**Address 2 (5 V tolerant input).** Address input A2 for the microprocessor interface.
B1	A3	**Address 3 (5 V tolerant input).** Address input A3 for the microprocessor interface.
C2	A4	**Address 4 (5 V tolerant input).** Address input A4 for the microprocessor interface.
C1	A5	**Address 5 (5 V tolerant input).** Address input A5 for the microprocessor interface.
D2	A6	**Address 6 (5 V tolerant input).** Address input A6 for the microprocessor interface. A6 is the most significant input
A6	D0	**Data 0 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port, D0 is the least significant bit.
B6	D1	**Data 1 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7).
A5	D2	**Data 2 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7).
B5	D3	**Data 3 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7).

Pin Description (continued)

Ball # BGA	Name	Description
A4	D4	**Data 4 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7).
B4	D5	**Data 5 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7).
A3	D6	**Data 6 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7).
B3	D7	**Data 7 (5 V tolerant three-state I/O).** Data input/output for the microprocessor port (D0 - D7), D7 is the most significant bit.
U4	Tdo	**IEEE1149.1a Test Data Output.** JTAG serial data is output on this pin on the falling edge of Tclk clock. If not used, this pin should be left unconnected.
U3	Tms	**IEEE1149.1a Test Mode Selection (3.3 V input).** JTAG signal that controls the state transition on the TAP controller. This pin is internally pulled to V_{DD}. If not used, this pin should be left unconnected.
U1	Tclk	**IEEE1149.1a Test Clock Signal (3.3 V input).** Input clock for the JTAG test logic. If not used, this pin should be pulled up to V_{DD}.
U2	$\overline{\text{Trst}}$	**IEEE1149.1a Reset Signal (3.3 V input).** Asynchronous reset for the JTAG TAP controller. This pin should be pulsed low on power-up to ensure that the TAP is reset. This pin is internally pulled down to DGND. If not used, this pin should be left unconnected.
E16,E17, F15,G17, H17,L17, M17,N17, P17,R17, T17,	NC	**Do NOT connect to these pins, internal connections**
T3	Tdi	**IEEE1149.1a Test Data Input (3.3 V input).** Input for JTAG serial test instructions and data. This pin is internally pulled up to V_{DD1}. If not used, this pin should be left unconnected.

Note 1: Connections relate to the Analog PLL stage, if the jitter attenuated outputs are not being used, you do not need to make these connections.

Table of Contents

List of Figures

List of Tables

1.0 Functional Description

The ZL30461 offers a complete timing solution in a BGA module package. The ZL30461 has been designed to provide timing for SDH and SONET equipment, conforming to ITU-T, ANSI, ETSI and Telcordia recommendations. In addition, it generates clocks for legacy PDH equipment operating at DS1, DS2, E1 and E3 rates. The ZL30461 also provides clocks for industry standard ST-BUS and GCI backplanes. The functional block diagram for the module is shown in Figure 1 “Functional Block Diagram” and its operation is described in the following sections.

1.1 Acquisition PLLs

The ZL30461 has two Acquisition PLLs for monitoring availability and quality of the Primary (PRI) and Secondary (SEC) reference clocks. Each Acquisition PLL operates independently and locks to the falling edges of input reference frequencies: 8 kHz, 1.544 MHz, 2.048 MHz or to the rising edge of 19.44 MHz. The reference frequency can be determined from reading the Acquisition PLL Status Register bits InpFreq1 and InpFreq0 (see Table 17 “Primary Acquisition PLL Status Register (R)” and Table 18 “Secondary Acquisition PLL Status Register (R)”).

The Primary and Secondary Acquisition PLLs are designed to provide status information that identifies three levels of reference clock quality. For clarity, only the Primary Acquisition PLL is referenced in the text, but the same applies to the Secondary Acquisition PLL.

- Reference frequency drifts more than ±30000 ppm or is lost completely. In response, the Primary Acquisition PLL enters its own holdover state and indicates this by asserting the HOLDOVER bit in the Primary Acquisition PLL Status Register (Table 17 “Primary Acquisition PLL Status Register (R)”). Entry into holdover forces the Core PLL into the Auto holdover state.
- Reference frequency drifts more than ±104 ppm. In response, the Primary Acquisition PLL asserts the Frequency Limit bit PAFL in its Primary Acquisition PLL Status Register (Table 17), indicating that the reference frequency crossed the boundary of the capture range.
- Reference frequency drifts more than ±12 ppm. In response, the PRIOR (Primary Reference Acceptance Range) bit and pin change state to logic 1, in conformance with Stratum 3 requirements defined in GR-1244-CORE.

Outputs of both Acquisition PLLs are connected to a multiplexer (MUX), which allows selecting a reference signal that guarantees better traceability to the Primary Reference Clock. This multiplexer channels binary words to the Core PLL digital phase detector (instead of analog signals). The digital phase detector in the Core PLL eliminates quantization errors and improves phase alignment accuracy.

The bandwidth of the Acquisition PLL is much wider than the bandwidth of the following Core PLL. This feature allows cascading Acquisition and Core PLLs without changing the transfer function of the Core PLL.

1.2 Core PLL

The most critical element of the ZL30461 is the Core PLL. This generates a phase-locked clock, filters jitter and wander and suppresses input phase transients. All of these features are in agreement with international standards:

- G.813 Option 1 clocks for SDH equipment
- GR-253 for SONET Stratum 3 and SONET Minimum Clocks (SMC)
- GR-1244 for Stratum 3 Clocks

The Core PLL supports three mandatory modes of operation: Free-run, Normal (Locked) and Holdover. Each of these modes places specific requirements on the building blocks of the Core PLL.

- In Free-run Mode, the Core PLL locks to the 20 MHz Master Clock Oscillator connected to pin OSCi. The stability of the generated clock remains the same as the stability of the Master Clock Oscillator but frequency accuracy can be greatly improved by use of the Master Clock Frequency Calibration register. This register compensates oscillator frequency, practically eliminating manufacturing tolerances.

- In Normal Mode, the Core PLL locks to one of the Acquisition PLLs. Both Acquisition PLLs provide preprocessed phase data to the Core PLL including detection of reference clock quality. This preprocessing reduces the load on the Core PLL and improves quality of the generated clock.
- In Holdover Mode, the Core PLL generates a clock based on data collected from past reference signals. The Core PLL enters Holdover Mode if the attached Acquisition PLL switches into the holdover state under external software or hardware control.

1.3 Digitally Controlled Oscillator (DCO)

The DCO is an arithmetic unit that continuously generates a stream of numbers representing the phase-locked clock. These numbers are passed to the Clock Synthesizer (see Section 1.4) where they are converted into electrical clock signals of different frequencies.

1.3.1 Filters

In Normal Mode, the clock generated by the DCO is phase-locked to the input reference signal and band-limited to meet network synchronization standards. The ZL30461 provides four software programmable (FCS bit in Control Reg 1 and FCS2 bit in Control Reg 3) and two hardware selectable (FCS pin) filtering options. The filtering characteristics are similar to a first order low pass filter with corner frequencies that support international standards:

FCS2 (bit)	FCS (pin/bit)	Filter	Conformance
0	0	1.5 Hz	Meets requirements of G.813 Option 1 and GR-1244 Stratum 3, Stratum 4E and Stratum 4 clocks.The maximum phase slope is limited to 41 ns in 1.326 ms.
0	1	0.1 Hz	Meets requirements of G.813 Option 2 and GR-253 for SONET stratum 3. The maximum phase slope is limited to 885 ns in one second.
1	0	12 Hz	This filter configuration limits output phase slope to 1200 µs/sec.
1	1	6 Hz	Meets requirements of G.813 Option 1 for SDH Equipment Clocks (SEC) and GR-1244 for Stratum 4 and Stratum 4E clocks. The maximum phase slope is limited to 50 ns in 1.326 ms.

Table 1 - Loop Filter Selection

1.3.2 Lock Indicator (LOCK)

The ZL30461 is considered locked (LOCK = 1) when the residual phase movement after declaring locked condition does not exceed 20 ns; as required by standard wander generation MTIE and TDEV tests. To ensure the integrity of the LOCK status indication, the ZL30461 holds LOCK bit/pin low for a minimum of 65 sec in the 0.1 Hz filtering mode and 10 sec in the 1.5 Hz filtering mode.

1.3.3 Reference Alignment ($\overline{\text{RefAlign}}$)

When the ZL30461 finishes locking to a reference an arbitrary phase difference will remain between its output clocks and its reference; this phase difference is part of the normal operation of the ZL30461. If so desired, the output clocks can be brought into phase alignment with the PLL reference (see Figure 17) by using the $\overline{\text{RefAlign}}$ control bit/pin.

Using $\overline{\text{RefAlign}}$ with 1.544 MHz, 2.048 MHz or 19.44 MHz Reference

If the ZL30461 is locked to a 1.544 MHz, 2.048 MHz or 19.44 MHz reference, then the output clocks can be brought into phase alignment with the PLL reference by using the $\overline{\text{RefAlign}}$ control bit/pin according to one of the procedures below:

For 0.1 Hz filtering applications (FCS=1, FCS2=0)

- Wait until the ZL30461 LOCK indicator is high, indicating that it is locked
- Pull FCS low
- Pull $\overline{\text{RefAlign}}$ low
- Hold $\overline{\text{RefAlign}}$ low for 250 µs
- Pull $\overline{\text{RefAlign}}$ high
- Wait until the LOCK indicator goes high
- Pull FCS high

After initiating a reference realignment, the ZL30461 will enter Holdover Mode for 200 ns while aligning the internal clocks to remove the static phase error. The ZL30461 will then begin the normal locking procedure. The LOCK indicator will go low 5 sec after $\overline{\text{RefAlign}}$ is pulled low and it will remain low for 10 sec.

For 1.5 Hz filtering applications (FCS=0, FCS2=0)

- Wait until the ZL30461 LOCK indicator is high, indicating that it is locked
- Pull $\overline{\text{RefAlign}}$ low
- Hold $\overline{\text{RefAlign}}$ low for 250 µs
- Pull $\overline{\text{RefAlign}}$ high

After initiating a reference realignment the ZL30461 will enter Holdover Mode for 200 ns while aligning the internal clocks to remove the static phase error. The ZL30461 will then begin the normal locking procedure. The LOCK indicator will go low 5 sec after $\overline{\text{RefAlign}}$ is pulled low and it will remain low for 10 sec.

For 6 Hz and 12 Hz filtering applications (FCS=1, FCS2=1 or FCS=0, FCS2=1)

- Wait until the ZL30461 LOCK indicator is high, indicating that it is locked
- Pull $\overline{\text{RefAlign}}$ low
- Hold $\overline{\text{RefAlign}}$ low for 250 µs
- Pull $\overline{\text{RefAlign}}$ high

After initiating a reference realignment the ZL30461 will enter Holdover Mode for 200 ns while aligning the internal clocks to remove the static phase error. The ZL30461 will then begin the normal locking procedure. The LOCK pin will remain high during the realignment process.

Using $\overline{\text{RefAlign}}$ with an 8 kHz Reference

If the ZL30461 is locked to an 8 kHz reference, then the output clocks can be brought into phase alignment with the PLL reference by using the $\overline{\text{RefAlign}}$ control bit/pin according to one of the procedures below:

For 0.1 Hz filtering applications (FCS=1, FCS2=0)

- Wait until the ZL30461 LOCK indicator is high, indicating that it is locked
- Pull FCS low
- Pull $\overline{\text{RefAlign}}$ low
- Hold $\overline{\text{RefAlign}}$ low for 10 sec
- Pull $\overline{\text{RefAlign}}$ high
- Wait until the LOCK indicator goes high
- Pull FCS high

After initiating a reference realignment the ZL30461 will enter Holdover Mode for 200 ns while aligning the internal clocks to remove the static phase error. The ZL30461 will then begin the normal locking procedure. The LOCK pin will remain high during the realignment process.

For 1.5 Hz filtering applications (FCS=0, FCS2=0)

- Wait until the ZL30461 LOCK indicator is high, indicating that it is locked
- Pull $\overline{\text{RefAlign}}$ low
- Hold $\overline{\text{RefAlign}}$ low for 10 sec
- Pull $\overline{\text{RefAlign}}$ high

After initiating a reference realignment the ZL30461 will enter Holdover Mode for 200 ns while aligning the internal clocks to remove the static phase error. The ZL30461 will then begin the normal locking procedure. The LOCK pin will remain high during the realignment process.

For 6 Hz and 12 Hz filtering applications (FCS=1, FCS2=1 or FCS=0, FCS2=1)

- Wait until the ZL30461 LOCK indicator is high, indicating that it is locked
- Pull $\overline{\text{RefAlign}}$ low
- Hold $\overline{\text{RefAlign}}$ low for 3 sec
- Pull $\overline{\text{RefAlign}}$ high

After initiating a reference realignment the ZL30461 will enter Holdover Mode for 200 ns while aligning the internal clocks to remove the static phase error. The ZL30461 will then begin the normal locking procedure. The LOCK pin will remain high during the realignment process.

1.4 Output Clocks

The ZL30461 has multiple clock outputs, from the Clock Synthersizer and the Jitter Attenuator. The very low jitter output clocks of the 19.44 MHz and 77.76 MHz are used for the backplane clocks and the high speed optical framers and physical interfaces

1.4.1 Clock Synthesizer

The output of the Core PLL is connected to the Clock Synthesizer that generates 12 clocks and three frame pulses.

1.4.2 Jitter Attenuator

The ZL30461 output driver circuit provides a jitter attenuated output at 77.76 MHz with less than 40 ps jitter performance. This output must be terminated correctly and failure to do so will affect the modules performance. The recommend termination for this output is shown in Figure 3.

In addition to the 77.76 MHz output, the ZL30461 also provides a 19.44 MHz jitter attenuated output.

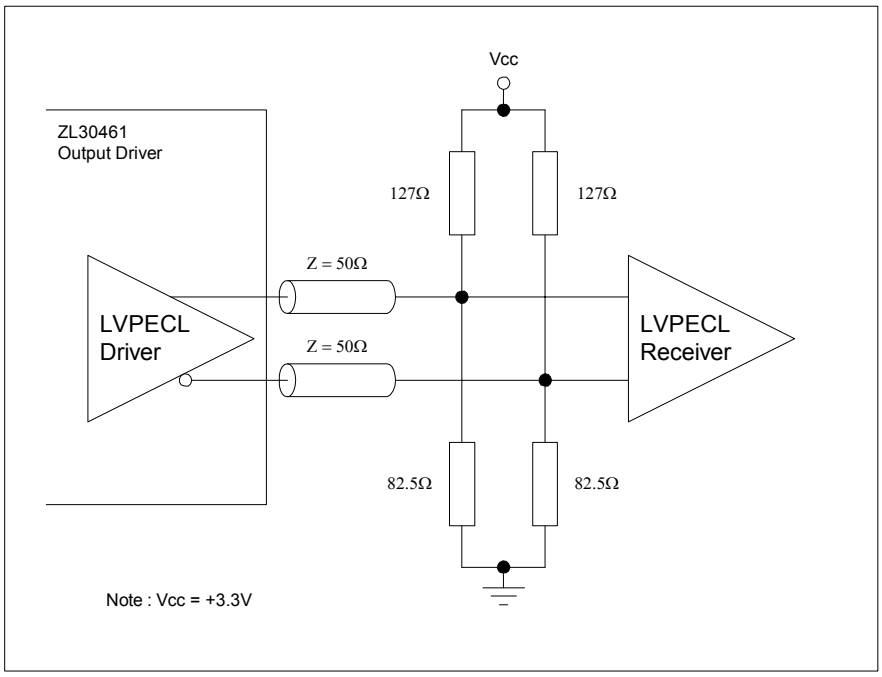


Figure 3 - LVPECL Output Termination Circuit

1.4.3 Clock Formats

The ZL30461 outputs the following clock and frame pulses:

- C1.5o: 1.544 MHz clock with nominal 50% duty cycle
- C2o: 2.048 MHz clock with nominal 50% duty cycle
- $\overline{\text{C4o}}$: 4.096 MHz clock with nominal 50% duty cycle
- C6o: 6.132 MHz clock with nominal 50% duty cycle
- C8o: 8.192 MHz clock with nominal 50% duty cycle
- C8.5o: 8.592 MHz clock with duty cycle from 30% to 70%
- C11o: 11.184 MHz clock with duty cycle from 30% to 70%
- $\overline{\text{C16o}}$: 16.384 MHz clock with nominal 50% duty cycle
- C19o: 19.44 MHz clock with nominal 50% duty cycle
- C34o: 34.368 MHz clock with nominal 50% duty cycle
- C44o: 44.736 MHz clock with nominal 50% duty cycle
- C155P/N: 155.52 MHz clock with nominal 50% duty cycle
- JA19Mo: 19.44 MHz clock with nominal 50% duty cycle
- JA77P/N: 77.76 MHz clock with nominal 50% duty cycle
- $\overline{\text{F0o}}$: 8 kHz frequency, with 244 ns wide, logic low frame pulse
- F8o: 8 kHz frequency, with 122 ns wide, logic high frame pulse
- $\overline{\text{F16o}}$: 8 kHz frequency, with 61 ns wide, logic low frame pulse

The combination of two pins, E3DS3/$\overline{\text{OC3}}$ and E3DS3, controls the selection of different clock configurations (see Figure 4 “C155o and C34/C44 Clock Generation Options” for details).

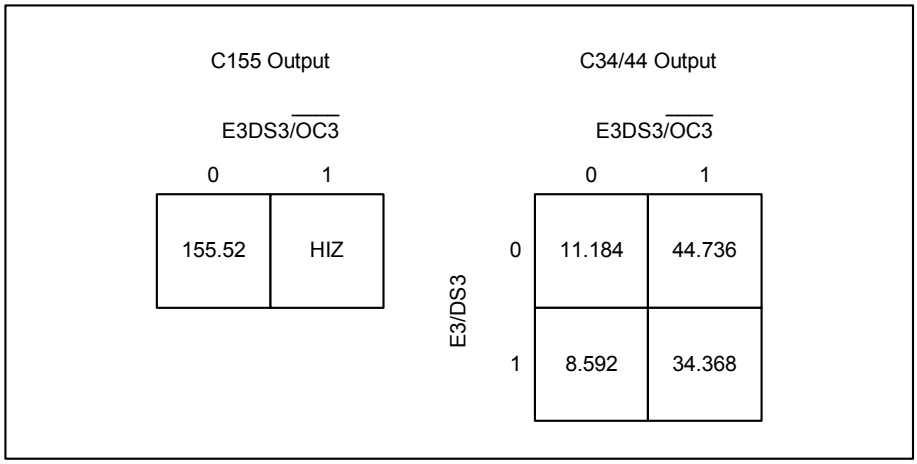


Figure 4 - C155o and C34/C44 Clock Generation Options

1.4.4 Output Clocks Phase Adjustment

The ZL30461 provides three control registers dedicated to programming the output clock phase offset. Clocks C16o, C8o, C4o, C2o and frame pulses F16o, F8o and F0o are derived from 16.384 MHz and can be jointly shifted with respect to an active reference clock by up to 125 µs with a step size of 61 ns. The required phase shift of clocks is programmable by writing to the Phase Offset Register 2 (Table 9) and to the Phase Offset Register 1 (Table 10). The C1.5o clock can be shifted as well in step sizes of 81ns by programming C1.5POA bits in Control Register 3 (Table 12).

The coarse phase adjustment is augmented with a very fine phase offset control of approximately 477 ps per step. This fine adjustment is programmable by writing to the Fine Phase Offset Register (Table 16 “Fine Phase Offset Register (R/W)”). The offset moves all clocks and frame pulses generated by ZL30461 including C155 clock.

1.5 Control State Machine

1.5.1 Clock Modes

Any Network Element that operates in a synchronous network must support three Clock Modes: Free-run, Normal (Locked) and Holdover. These clock modes determine the behavior of a Network Element to the unforeseen changes in the network synchronization hierarchy. Requirements for clock modes are defined in the international standards e.g.: G.812, G.813, GR-1244-CORE and GR-253-CORE and they are very strictly enforced by network operators. The ZL30461 supports all clock modes and each of these modes have a corresponding state in the Control State Machine.

1.5.2 ZL30461 State Machine

The ZL30461 Control State Machine is a complex combination of many internal states supporting the three mandatory clock modes. The simplified version of this state machine is shown in Figure 5 and it includes the mandatory states: Free-run, Normal and Holdover. These three states are complemented by two additional states: Reset and Auto Holdover, which are critical to the ZL30461 operation under the changing external conditions.

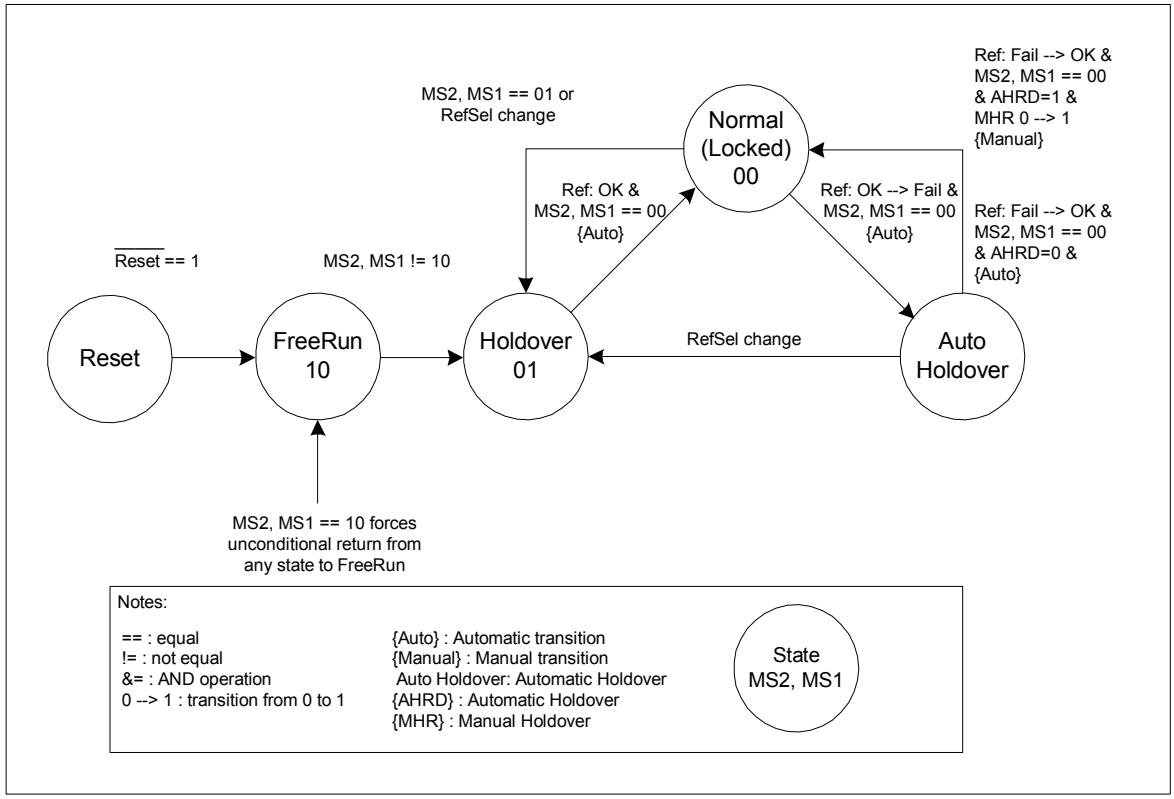


Figure 5 - ZL30461 State Machine

1.5.2.1 Reset State

The Reset State must be entered when ZL30461 is powered-up. In this state, all arithmetic calculations are halted, clocks are stopped, the microprocessor port is disabled and all internal registers are reset to their default values. The Reset state is entered by pulling the $\overline{\text{RESET}}$ pin to logic 0 for a minimum of 1 µs. When the $\overline{\text{RESET}}$ pin is pulled back to logic 1, internal logic starts a 625 µs initialization process before switching into the Free-run state (MS2, MS1 = 10). It is recommended to perform a module reset immediately after power up, to ensure the ZL30461 is set to a know state.

1.5.2.2 Free-Run State

The Free-run state is entered when synchronization to the network is not required or is not possible. Typically, this occurs during installation, repairs or when a Network Element operates as a master node in an isolated network. In the Free-run state, the accuracy of the generated clocks is determined by the accuracy and stability of the ZL30461 Master Crystal Oscillator. When equipment is installed for the first time (or periodically maintained), the accuracy of the Free-run clocks can be adjusted to within $1x10^{-12}$ by setting the offset frequency in the Master Clock Frequency Calibration Register. When powering up the equipment, it is recommended that the module has at least 12 hours to stabilize after the equipment has reached it normal operating temperature.

1.5.2.3 Normal State (Locked State)

The Normal State is entered when Normal Mode is selected and a good quality reference clock is available. The ZL30461 automatically detects the frequency of the reference clock (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) and sets the LOCK status bit and pin to logic 1 after acquiring synchronization. In the Normal state all generated clocks (C1.5o, C2o, $\overline{\text{C4o}}$, C6o, C8o, $\overline{\text{C16o}}$, C19o, JA19Mo, C34/C44, JA77 and C155) and frame pulses ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$) are derived from network timing. To guarantee uninterrupted synchronization, the ZL30461 has two

Acquisition PLLs that continuously monitor the quality of the incoming reference clocks. This dual architecture enables quick replacement of a poor or failed reference and minimizes the time spent in other states.

During this state the ZL30461 can tolerate a frequency change (on the active input) without generating an alarm or changing state. With the 0.1 Hz filter selected, the module can withstand a 0.06 ppm change and with the 1.5 Hz filter selected, the module can withstand a 10 ppm change.

1.5.2.4 Holdover State

The Holdover State is typically entered for short durations while network synchronization is temporarily disrupted. In Holdover Mode, the ZL30461 generated clocks are not locked to an external reference signal, but these outputs are based on stored coefficients in memory. These coefficients are determined while the module is in Normal State for at least 10 minutes after the modules stabilization period.

The initial frequency offset of the ZL30461's Core PLL in Holdover Mode is $\pm 32 \times 10^{-12}$. This is more accurate than Telcordia's GR-1244-CORE Stratum 3E requirement of $\pm 1 \times 10^{-9}$. Once the ZL30461 has transitioned into Holdover Mode, holdover stability is determined by the stability of the 20 MHz Master Clock Oscillator applied to the OSCi pin. The on-board TCXO conforms to Telcordia's GR-1244-CORE Stratum 3 requirement of $\pm 50 \times 10^{-9}$, with a short term stability of $\pm 0.37 \times 10^{-6}$, for the first 24 hours (after the module's stabilization period).

1.5.2.5 Auto Holdover State

The Auto Holdover state is a transitional state that the ZL30461 enters automatically when the active reference fails unexpectedly. When the ZL30461 detects loss of reference, it sets the HOLDOVER status bit and waits in Auto Holdover state until the failed reference recovers. The HOLDOVER status may alert the control processor about the failure and in response the control processor may switch to the secondary reference clock. The Auto Holdover and Holdover states are internally combined together and they are output as a HOLDOVER status pin and bit 4 in Status Register 1 (Table 7).

1.5.3 State Transitions

In a typical Network Element application, the ZL30461 will typically operate in Normal Mode (MS2, MS1 == 00) generating synchronous clocks. Its two Acquisition PLLs will continuously monitor the input references for signs of degraded quality and output status information for further processing. The status information from the Acquisition PLLs and the CORE PLL, combined with status information from line interfaces and framers (as listed below), forms the basis for creating reliable network synchronization.

- Acquisition PLLs (PRIOR, SECOR, PAH, PAFL, SAH, SAFL)
- Core PLL (LOCK, HOLDOVER, FLIM)
- Line interfaces (e.g. LOS - Loss of Signal, AIS - Alarm Indication Signal)
- Framers (e.g. LOF - Loss of frame or Synchronization Status Messages carried over SONET S1 byte or ESF-DS1 Facility Data Link)

The ZL30461 State Machine is designed to perform some transitions automatically, leaving other less time dependent tasks to the control processor. The State Machine includes two stimulus signals which are critical to automatic operation: "OK --> FAIL" and "FAIL --> OK" that represent loss (and recovery) of reference signal or its drift by more than ±30000 ppm. Both of them force the Core PLL to transition into and out of the Auto Holdover state. The ZL30461 State Machine may also be driven by controlling the mode select pins or bits MS2, MS1. In order to avoid network synchronization problems, the State Machine has built-in basic protection that does not allow switching the Core PLL into a state where it cannot operate correctly e.g. it is not possible to force the Core PLL into Normal Mode when all references are lost.

1.6 TCXO and Master Clock Frequency Calibration Circuit

In an ordinary timing generation module, the Free-run Mode accuracy of generated clocks is determined by the accuracy of the Master Crystal Oscillator. If the Master Crystal Oscillator has a manufacturing tolerance of +/-4.6 ppm, the generated clocks will have no better accuracy.

The ZL30461 has its own on-board Stratum 3 TCXO (+/-4.6 ppm), which outputs 20 MHz on the OSCo pin. For most applications this oscillator offers sufficient accuracy and can be connected back into the module by simply linking the OSCo in OSCi pins together. However, if a more accurate reference is required, then the on-board TCXO can be disconnected completely and an external 20 MHz reference applied to the OSCi pin. If any external reference is going to be used, then it is recommended that the TCXO power applied to the TV_{DD} and TGND pins is removed. This will minimize the risk of noise or harmonics causing any problems.

The ZL30461 minimizes tolerance problems by providing a programmable Master Clock Frequency Calibration circuit. This can reduce the oscillator manufacturing tolerance to near zero. The feature reduces the need for high precision 20 MHz crystal oscillators, that could be very expensive, for equipment that has to maintain accuracy over a very long period of time (e.g. 20 years in some applications).

The compensation value for the Master Clock Calibration Register (MCFC3 to MCFC0) can be calculated from the following equation:

$$MCFC = 45036 * f_{offset} \qquad \text{where:} \quad f_{offset} = f_m - 20\,000\,000 \text{ Hz} \qquad \text{(EQ 1)}$$

The f_m frequency should only be measured after the Master Oscillator has been powered long enough for it to reach a steady operating temperature. The ZL30461 should have a warm-up time of 10 hours to ensure that the module has reached a stable operating temperature (however, reasonable operation can be expected with 30 minutes).

Section 3.3 provides two examples of how to calculate an offset frequency and convert the decimal value to a binary format. The maximum frequency compensation range of the MCFC register is equal to ±2384 ppm (±47680 Hz).

1.7 Microprocessor Interface

The ZL30461 DPLL can be controlled by a device connected directly to the hardware control pins. If the HW pin is tied to logic 0 (see Figure 6 “Hardware and Software Control options”), a microprocessor with a Motorola type bus may be used to control PLL operation and check its status. Under software control, the control pins MS2, MS1, FCS, RefSel, RefAlign are disabled and they are replaced by the equivalent control bits. The output pins LOCK, HOLDOVER, PRIOR and SECOR are always active and provide current status information whether the device is in microprocessor or hardware control. Software (microprocessor) control provides additional functionality that is not available in hardware control such as output clock phase adjustment, master clock frequency calibration and extended access to status registers.

1.8 JTAG Interface

The ZL30461 core PLL JTAG (Joint Test Action Group) interface conforms to the Boundary-Scan standard IEEE1149.1-1990, that specifies a design-for-testability technique called Boundary-Scan Test (BST). The BST architecture is made up of four basic elements, Test Access Port (TAP), TAP Controller, Instruction Register (IR) and Test Data Registers (TDR), and all these elements are implemented on the ZL30461.

Zarlink Semiconductor provides a Boundary Scan Description Language (BSDL) file that contains all the information required for a JTAG test system to access the ZL30461's core PLL boundary scan circuitry. The file is available for download from the Zarlink Semiconductor web site: www.zarlink.com.

2.0 Hardware and Software Control

The ZL30461 offers Hardware and Software Control options that simplify design of basic or complex clock synchronization modules. Hardware control offers fewer features but still allows for building of sophisticated timing cards without extensive programming. The complete set of control and status functions for each mode are shown in Figure 6 “Hardware and Software Control options”.

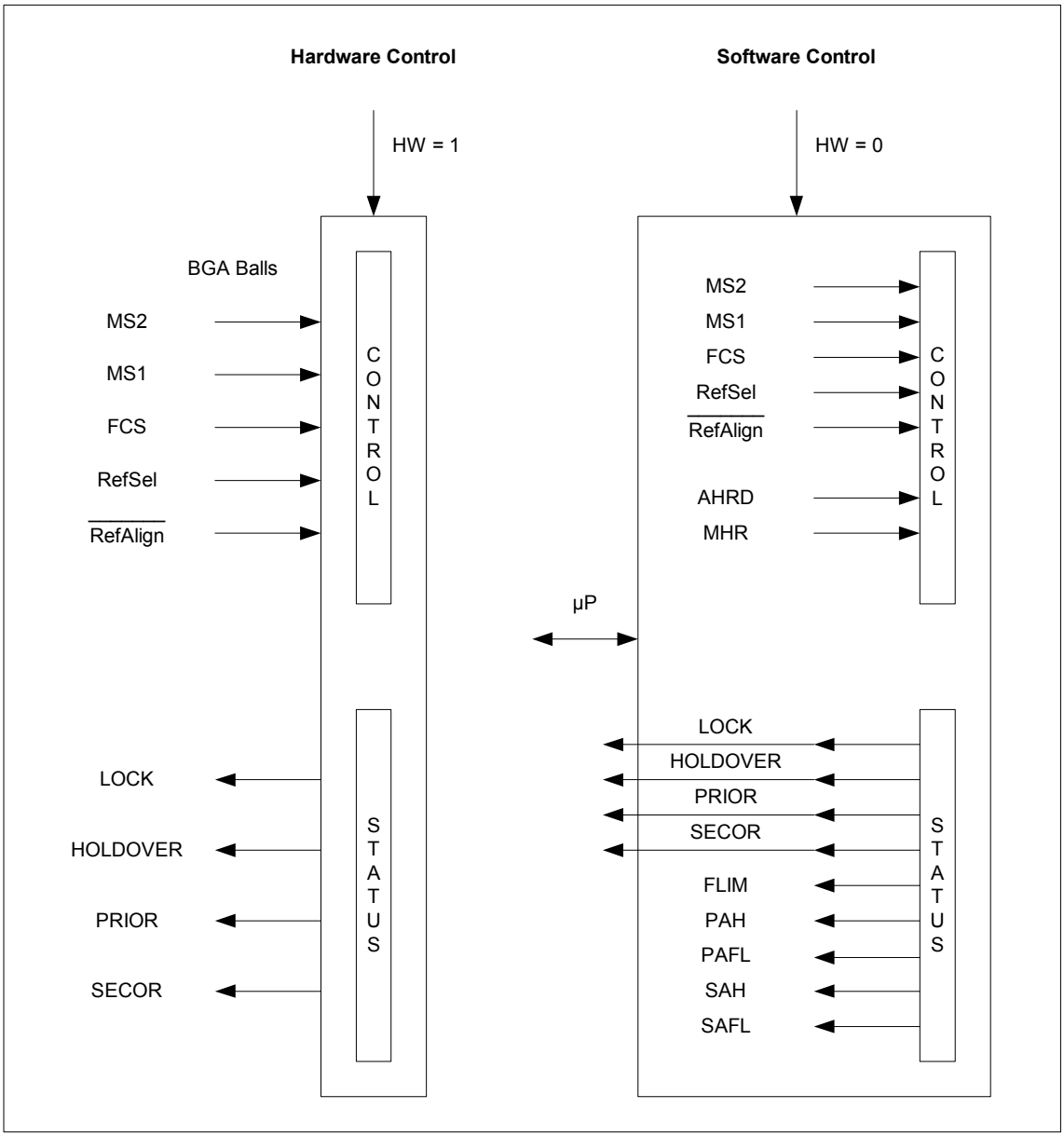


Figure 6 - Hardware and Software Control Options

2.1 Hardware Control

The Hardware control is a subset of software control and it will only be briefly described with cross-referencing to Software control programmable registers.

2.1.1 Control Pins

The ZL30461 has six dedicated control pins for selecting modes of operation and activating different functions. These pins are listed below:

MS2 and MS1 pins: Mode Select. The MS2 and MS1 inputs select the PLL mode of operation. See Table 2 for details. The logic level at these inputs is sampled by the rising edge of the F8o frame pulse.

FCS pin: Filter Characteristic Select. The FCS input is used to select the filtering characteristics of the Core PLL. See Table 3 for details.

MS2	MS1	Mode of Operation
0	0	Normal Mode
0	1	Holdover Mode
1	0	FreeRun Mode
1	1	Reserved

Table 2 - Operating Modes and States

FCS	Filtering Characteristic	Phase Slope
0	**Filter corner frequency set to 1.5 Hz.** This selection meets requirements of G.813 Option 1 and GR-1244 Stratum 3 clocks.	41 ns in 1.326 ms
1	**Filter corner frequency set to 0.1 Hz.** This selection meets requirements of G.813 Option 2, GR-253 for SONET Stratum 3 and GR-253 for SONET Minimum Clocks (SMC).	885 ns/s

Table 3 - Filter Characteristic Selection

RefSel: Reference Source Select. The RefSel input selects the PRI (Primary) or SEC (Secondary) input as the reference clock for the Core PLL. The logic level at this input is sampled by the rising edge of F8o.

RefSel	Input Reference
0	Core PLL connected to the Primary Acquisition PLL
1	Core PLL connected to the Secondary Acquisition PLL

Table 4 - Reference Source Select

$\overline{\text{RefAlign}}$: Reference Align. The $\overline{\text{RefAlign}}$ input controls phase realignment between the input reference and the generated output clocks.

2.1.2 Status Pins

The ZL30461 has four dedicated status pins for indicating modes of operation and quality of the Primary and Secondary reference clocks. These pins are listed below:

LOCK - This output goes to logic 1 when the core PLL is locked to the selected Acquisition PLL.

HOLDOVER - This output goes to logic 1 when the Core PLL enters Holdover Mode. The Core PLL will switch to Holdover Mode if the respective Acquisition PLL enters Holdover Mode or if the mode select pins or bits are set to Holdover (MS2, MS1 = 01).

PRIOR - Primary Reference Acceptance Range. This output goes to logic 1 when the primary reference frequency is outside of the acquisition PLL ±12 ppm acceptance range.

SECOR - Secondary Reference Acceptance Range. This output goes to logic 1 when the secondary reference frequency is outside of the acquisition PLL ±12 ppm acceptance range.

2.2 Software Control

Software control is enabled by setting the HW pin to logic 0 (HW = 0). In this mode all hardware control pins (inputs) are disabled, but the status (outputs) are still enabled. The ZL30461 has 18 registers that provide all the functionality available in Hardware control and also offer advanced control and monitoring that is only available in Software control (see Figure 6 “Hardware and Software Control options”).

2.2.1 Control Bits

The ZL30461 has seven control bits as is shown in Figure 6 “Hardware and Software Control options”. Five bits replace the five hardware control pins: MS2, MS1, FCS, RefSel and $\overline{\text{RefAlign}}$ (Table5: Control Register 1), and two bits support recovery from Auto Holdover Mode: AHRD and MHR (Table 15: Core PLL Control Register).

In addition to the Control bits shown in Figure 6 “Hardware and Software Control Options”, the ZL30461 has a number of bits and registers that are accessed infrequently or during configuration only e.g. Phase Offset Adjustment or Master Clock Frequency Calibration.

2.2.2 Status Bits

The ZL30461 has nine status bits (see Figure 6 “Hardware and Software Control options”, Tables 6, 17 and 18). Four bits perform the same function as their equivalent status pins (PRIOR, SECOR, LOCK and HOLDOVER). Five bits perform two functions. Bits FLIM, PAFL, SAFL indicate drift of the reference clock frequencies beyond the capture range of Acquisition and Core PLLs and bits PAH and SAH show entry of Primary and Secondary Acquisition PLLs into Holdover Mode. These bits are described in detail in Section 2.2.3. The status pins are enabled when the ZL30461 operates in software control and they can be used to trigger interrupts.

2.2.3 ZL30461 Register Map

Addresses: 00H to 6FH

Address hex	Register	Read Write	Function
00	Control Register 1	R/W	RefSel, 0, 0, MS2, MS1, FCS, 0, RefAlign
01	Status Register 1	R	PRIOR, SECOR, LOCK, HOLDOVER, rsv, FLIM, rsv, rsv

Table 5 - ZL30461 Register Map

Address hex	Register	Read Write	Function
04	Control Register 2	R/W	E3DS3/$\overline{OC3}$, E3/$\overline{DS3}$, 0, 0, 0, 0, 0, 0,
06	Phase Offset Register 2	R/W	0, 0, 0, 0, OffEn, C16POA10, C16POA9, C16POA8
07	Phase Offset Register 1	R/W	C16POA7, C16POA6, C16POA5, C16POA4, C16POA3, C16POA2, C16POA1, C16POA0
0F	Device ID Register	R	0111 0000
11	Control Register 3	R/W	rsv, rsv, C1.5POA2, C1.5POA1, C1.5POA0, 0, 0, FCS2
13	Clock Disable Register 1	R/W	0, 0, C16odis, C8odis, C4odis, C2odis, C1.5odis,0
14	Clock Disable Register 2	R/W	0, 0, 0, F8odis, F0odis, F16odis, C6odis, C19odis
19	Core PLL Control Register	R/W	0, 0, 0, 0, 0, MHR, AHRD, 0
1A	Fine Phase Offset Register	R/W	FPOA7, FPOA6, FPOA5, FPOA4, FPOA3, FPOA2, FPOA1, FPOA0
20	Primary Acquisition PLL Status Register	R	rsv, rsv, rsv, InpFreq1, InpFreq0, rsv, PAH,PAFL
28	Secondary Acquisition PLL Status Register	R	rsv, rsv, rsv, InpFreq1, InpFreq0, rsv, SAH, SAFL
40	Master Clock Frequency Calibration Register - Byte 4	R/W	MCFC31, MCFC30, MCFC29, MCFC28, MCFC27, MCFC26, MCFC25, MCFC24,
41	Master Clock Frequency Calibration Register - Byte 3	R/W	MCFC23, MCFC22, MCFC21, MCFC20, MCFC19, MCFC18, MCFC17, MCFC16
42	Master Clock Frequency Calibration Register - Byte 2	R/W	MCFC15, MCFC14, MCFC13, MCFC12, MCFC11, MCFC10, MCFC9, MCFC8
43	Master Clock Frequency Calibration Register - Byte 1	R/W	MCFC7, MCFC6, MCFC5, MCFC4, MCFC3, MCFC2, MCFC1, MCFC0

Table 5 - ZL30461 Register Map (continued)

Note: The ZL30461 uses address space from 00 h to 6 Fh. Registers at address locations not listed above must not be written or read.

2.2.4 Register Description

Address: 00 H

Bit	Name	Functional Description	Default
7	RefSel	**Reference Select.** A zero selects the PRI (Primary) reference source as the input reference signal and a one selects the SEC (Secondary) reference.	0
6-5	RSV	**Reserved.**	00

Table 6 - Control Register 1 (R/W)

Bit	Name	Functional Description	Default
4-3	MS2, MS1	**Mode Select.** - MS2 = 0 MS1 = 0 Normal Mode (Locked Mode) - MS2 = 0 MS1 = 1 Holdover Mode - MS2 = 1 MS1 = 0 Free-run Mode - MS2 = 1 MS1 = 1 Reserved	10
2	FCS	**Filter Characteristic Select.** (see Table 12 for complimentary FCS2 bit description) - FCS2 = 0, FCS = 0: Filter corner frequency set to 1.5 Hz - FCS2 = 0, FCS = 1: Filter corner frequency set to 0.1 Hz - FCS2 = 1, FCS = 0: Filter corner frequency set to 12 Hz - FCS2 = 1, FCS = 1: Filter corner frequency set to 6 Hz Conformance of these filter settings to standards is presented in Table 1.	0
1	RSV	**Reserved.**	0
0	$\overline{\text{RefAlign}}$	**Reference Align.** A high-to-low transition aligns the generated output clocks to the input reference signal (see Section 1.3.3 for details). **This bit should never be held low permanently.**	1

Table 6 - Control Register 1 (R/W) (continued)

Address: 01 H

Bit	Name	Functional Description
7	PRIOR	**Primary Reference Acceptance Range.** A one indicates that the primary reference is off the nominal frequency by more than ±12 ppm. This indicator has built-in hysteresis and is updated once a second. Monitoring is always active and is independent of filter characteristics (FCS). Switching thresholds are determined by the accuracy of the Master Clock OSCi. In an extreme case when over time the Master Clock oscillator drifts ±4.6 ppm, the switching thresholds will drift as well. The Master Clock Frequency Calibration Register can be used to eliminate dependence of PRIOR (SECOR) switching threshold and Free-run Mode accuracy on the Master Crystal Oscillator tolerance.
6	SECOR	**Secondary Reference Acceptance Range.** A one indicates that the secondary reference is off the nominal frequency by more than ±12 ppm. Functionally, this bit is equivalent to the PRIOR bit for Primary Acquisition PLL.
5	TRUELOCK	**True Lock.** This bit goes to 1 when the Core PLL is locked to the selected Acquisition PLL (±142 ppm - relative to the accuracy of the 20 MHz master oscillator input OSCi).
4	HOLDOVER	**Holdover.** This bit goes to 1 when the Core PLL is in Holdover mode.
3	RSV	**Reserved.**
2	FLIM	**Frequency Limit.** This bit goes to 1 when the Core PLL is pulled by the input reference signal to the edge of its frequency tracking range set at ±104 ppm (relative to the accuracy of the 20 MHz master oscillator input OSCi). This bit may change state momentarily in the event of large jitter or wander excursions occurring when the input reference is close to the frequency limit range.

Table 7 - Status Register 1 (R)

Bit	Name	Functional Description
1	RSV	**Reserved.**
0	RSV	**Reserved.**

Table 7 - Status Register 1 (R) (continued)

Address: 04 H

Bit	Name	Functional Description	Default
7	E3DS3/$\overline{OC3}$	**E3, DS3 or OC-3 Clock Select.** Setting this to 0 enables the C155P/N outputs and enables the C34/C44 output to provide C8 or C11 clocks. A 1 sets the C155 clock outputs into high impedance and enables the C34/C44 output to provide a C34 or C44 clock.	0
6	E3/$\overline{DS3}$	**E3 or DS3 Clock Select.** When E3DS3/$\overline{OC3}$ bit is 1, a 0 on the E3/$\overline{DS3}$ bit selects a 44.736 MHz clock on the C34/C44 output and a 1 selects a 34.368 MHz clock. When the E3DS3/$\overline{OC3}$ bit is set to 0, a 0 on the E3/$\overline{DS3}$ bit selects an 11.184 MHz clock on the C34/C44 output and a 1 selects an 8.592 MHz clock.	0
5-0	RSV	**Reserved.**	000000

Table 8 - Control Register 2 (R/W)

Address: 06 H

Bit	Name	Functional Description	Default
7-4	RSV	**Reserved.**	0000
3	OffEn	**Offset Enable.** Set to 1 to enable programmable phase offset adjustment (C16 Phase Offset Adjustment and C1.5 Phase Offset Adjustment) between the input reference and the generated clocks.	0
2-0	C16POA10 to C16POA8	**C16 Phase Offset Adjustment.** These three bits (most significant) in conjunction with the eight bits of Phase Offset Register 1 allow for phase shifting of all clocks and frame pulses that are derived from the C16 clock (C8o, C4o, C2o, F16o, F8o, F0o). The phase offset is an unsigned number in a range from 0 to 2047. Each increment by one represents phase-offset advancement by 61.035 ns with respect to the input reference signal. The phase offset is a two-byte value and it must be written in one step increments. For example: from a current position of 22H, four writes are required to advance the clocks by 244 ns: write 23H, 24H, 25H, 26H. Writing numbers in reverse order will delay clocks from their present position.	000

Table 9 - Phase Offset Register 2 (R/W)

Address: 07 H

Bit	Name	Functional Description	Default
7-0	C16POA7 to C16POA0	**C16 Phase Offset Adjustment.** The eight least significant bits of the phase offset adjustment word. See the Phase Offset Register 2 for details.	0000 0000

Table 10 - Phase Offset Register 1 (R/W)

Address: 0F H

Bit	Name	Functional Description
7-4	ID7 - 4	**Device Identification Number.** These four bits represent the device part number. The ID number for ZL30461 is 0111.
3-0	ID3 - 0	**Device Revision Number.** These bits represent the revision number, starts from 0000.

Table 11 - Device ID Register (R)

Address: 11 H

Bit	Name	Functional Description	Default
7	RSV	**Reserved.**	0
6	RSV	**Reserved.**	0
5-3	C1.5POA2 to C1.5POA0	**C1.5 Phase Offset Adjustment.** These three bits allow for changing of the phase offset of the C1.5o clock relative to the active input reference. The phase offset is an unsigned number in a range from 0 to 7. Each increment by one represents phase-offset advancement by 80.96 ns. Example: Writing 010 advances the C1.5o clock by 162 ns, writing 001 delays this clock by 80.96 ns from this (010) position, writing 000 will remove programmed the offset.	000
2-1	RSV	**Reserved.**	000
0	FCS2	**Filter Characteristic Select.** (see Table 6 for complimentary FCS bit description) - FCS2 = 0, FCS = 0: Filter corner frequency set to 1.5 Hz. - FCS2 = 0, FCS = 1: Filter corner frequency set to 0.1 Hz. - FCS2 = 1, FCS = 0: Filter corner frequency set to 12 Hz. - FCS2 = 1, FCS = 1: Filter corner frequency set to 6 Hz. Conformance of these filter settings to standards is presented in Table 1.	000

Table 12 - Control Register 3 (R/W)

Address: 13 H

Bit	Name	Functional Description	Default
7-6	RSV	**Reserved.**	00
5	C16odis	**$\overline{\text{C16o}}$ (16.384 MHz) Clock Disable.** When set to 1, this bit tristates the 16.384 MHz clock output.	0
4	C8odis	**C8o (8.192 MHz) Clock Disable.** When set to 1, this bit tristates the 8.192 MHz clock output.	0
3	C4odis	**$\overline{\text{C4o}}$ (4.096 MHz) Clock Disable.** When set to 1, this bit tristates the 4.096 MHz clock output.	0
2	C2dis	**C2o (2.048 MHz) Clock Disable.** When set to 1, this bit tristates the 2.048 MHz clock output.	0
1	C1.5dis	**C1.5o (1.544 MHz) Clock Disable.** When set to 1, this bit tristates the 1.544 MHz clock output.	0
0	RSV	**Reserved.**	0

Table 13 - Clock Disable Register 1 (R/W)

Address: 14 H

Bit	Name	Functional Description	Default
7-5	RSV	**Reserved.**	000
4	F8odis	**F8o Frame Pulse Disable.** When set to 1, this bit tristates the 8 kHz 244 ns active high framing pulse output.	0
3	F0odis	**$\overline{\text{F0o}}$ Frame Pulse Disable.** When set to 1, this bit tristates the 8 kHz 122 ns active low framing pulse output.	0
2	F16odis	**$\overline{\text{F16o}}$ Frame Pulse Disable.** When set to 1, this bit tristates the 8 kHz 61 ns active low framing pulse output.	0
1	C6odis	**C6o (6.312 MHz) Clock Disable.** When set to 1, this bit tristates the 6.312 MHz clock output.	0
0	C19odis	**C19o (19.44 MHz) Clock Disable.** When set to 1, this bit tristates the 19.44 MHz clock output.	0

Table 14 - Clock Disable Register 2 (R/W)

Address: 19 H

Bit	Name	Functional Description	Default
7-3	RSV	**Reserved.**	00000
2	MHR	**Manual Holdover Release**. A change form 0 to 1 on the MHR bit will release the Core PLL from Auto Holdover when automatic return from holdover is disabled (AHRD is set to 1). This bit is level sensitive and it must be cleared immediately after it is set to 1 (next write operation). This bit has no effect if AHRD is set to 0.	0
1	AHRD	**Automatic Holdover Return Disable**. When set high, this bit inhibits the Core PLL from automatically switching back to Normal Mode from Auto Holdover state when the active Acquisition PLL regains lock to input reference. The active Acquisition PLL is the Acquisition PLL to which the Core PLL is currently connected.	0
0	RSV	**Reserved.**	0

Table 15 - Core PLL Control Register (R/W)

Address: 1A H

Bit	Name	Functional Description	Default
7-0	FPOA7 - 0	**Fine Phase Offset Adjustment.** This register allows phase offset adjustment of all output clocks and frame pulses ($\overline{C16o}$, C8o, $\overline{C4o}$, C2o, $\overline{F16o}$, F8o, $\overline{F0o}$, C155o, C19o, JA19Mo, C34/44, JA77P/N) relative to the active input reference. The adjustment can be positive (advance) or negative (delay) with a nominal step size of 477 ps (61.035 ns / 128). The rate of phase change is limited to 885 ns/s in SONET Stratum 3, and 41ns in 1.326 ms for all other filter characteristic selections. The phase offset value is a signed 2's complement number e.g.: Advance: +1 step = 01H, +2 steps = 02H, +127 steps = EFH Delay: -1 step = FFH, -2 steps = FEH, -128 steps = 80H Example: Writing 08H advances all clocks by 3.8 ns and writing F3H delays all clocks	0000 0000

Table 16 - Fine Phase Offset Register (R/W)

Address: 20 H

Bit	Name	Functional Description
7-5	RSV	**Reserved.**
4-3	InpFreq1-0	**Input Frequency.** These two bits identify the Primary Reference Clock frequency. - 00 = 19.44 MHz - 01 = 8 kHz - 10 = 1.544 MHz - 11 = 2.048 MHz
2	RSV	**Reserved.**
1	PAH	**Primary Acquisition PLL Holdover.** This bit goes to 1 whenever the Acquisition PLL enters Holdover Mode. Holdover Mode is entered when the reference frequency: - is lost completely - drifts more than ±30000 ppm off from the nominal frequency - of a large phase hit occurs on the reference clock
0	PAFL	**Primary Acquisition PLL Frequency Limit.** This bit goes to 1 whenever the Acquisition PLL exceeds its capture range of ±104 ppm. This bit can flicker high in the event of a large excursion of still tolerable input jitter.

Table 17 - Primary Acquisition PLL Status Register (R)

Address: 28 H

Bit	Name	Functional Description
7-5	RSV	**Reserved.**
4-3	InpFreq1-0	**Input Frequency.** These two bits identify the Secondary Reference Clock frequency. - 00 = 19.44 MHz - 01 = 8 kHz - 10 = 1.544 MHz - 11 = 2.048 MHz
2	RSV	**Reserved.**
1	SAH	**Secondary Acquisition PLL Holdover.** This bit goes to 1 whenever the Acquisition PLL enters Holdover Mode. Holdover Mode is entered when the reference frequency: - is lost completely - drifts more than ±30000 ppm off from the nominal frequency - of a large phase hit occurs on the reference clock
0	SAFL	**Secondary Acquisition PLL Frequency Limit.** This bit goes to 1 whenever the Acquisition PLL exceeds its capture range of ±104 ppm. This bit can flicker high in the event of a large excursion of still tolerable input jitter.

Table 18 - Secondary Acquisition PLL Status Register (R)

Address: 40 H

Bit	Name	Functional Description	Default
7-0	MCFC32-24	**Master Clock Frequency Calibration.** This most significant byte contains the 31st to 24th bit of the Master Clock Frequency Calibration Register. See Applications Section 3.3 for a detailed description of how to calculate the MCFC value.	0000 0000

Table 19 - Master Clock Frequency Calibration Register 4 (R/W)

Address: 41 H

Bit	Name	Functional Description	Default
7-0	MCFC23-16	**Master Clock Frequency Calibration.** This byte contains the 23rd to 16th bit of the Master Clock Frequency Calibration Register.	0000 0000

Table 20 - Master Clock Frequency Calibration Register 3 (R/W)

Address: 42 H

Bit	Name	Functional Description	Default
7-0	MCFC15-8	**Master Clock Frequency Calibration.** This byte contains the 15th to 8th bit of the Master Clock Frequency Calibration Register.	0000 0000

Table 21 - Master Clock Frequency Calibration Register 2 (R/W)

Address: 43 H

Bit	Name	Functional Description	Default
7-0	MCFC7-0	**Master Clock Frequency Calibration.** This byte contains Bit 7 to Bit 0 of the Master Clock Frequency Calibration Register.	0000 0000

Table 22 - Master Clock Frequency Calibration Register 1 (R/W)

3.0 Applications

This section contains application specific details for Mode Switching, Master Clock Oscillator calibration and power supply decoupling for the Analog PLL.

3.1 ZL30461 Mode Switching - Examples

The ZL30461 is designed to transition from one mode to the other driven by the internal State Machine or by manual control. The following examples present a couple of typical scenarios of how the ZL30461 can be employed in network synchronization equipment (e.g. timing modules, line cards or stand alone synchronizers).

3.1.1 System Start-Up Sequence: FREE-RUN --> HOLDOVER --> NORMAL

The Free-run to Holdover to Normal transition represents a sequence of steps that will most likely occur during a new system installation or scheduled maintenance of timing cards. The process starts from the RESET state and then transitions to Free-run state when the device is being initialized. At the end of this process, the ZL30461 should be switched into Normal Mode (with MS2, MS1 set to 00) instead of Holdover Mode. If the reference clock is available, the ZL30461 will transition briefly into Holdover state to acquire synchronization and switch automatically to Normal state. If the reference clock is not available, the ZL30461 will stay in Holdover state indefinitely. Whilst in Holdover state, the Core PLL will continue generating clocks with the same accuracy as in the Free-run Mode, waiting for a valid reference clock. When the system is connected to the network (or timing card switched to a valid reference), the Acquisition PLL will quickly synchronize and clear its own Holdover status (PAH bit). This will enable the Core PLL to start the synchronization process. After acquiring lock, the ZL30461 will automatically switch from Holdover state to Normal state without system intervention. This transition to the Normal state will be flagged by the LOCK status bit and pin.

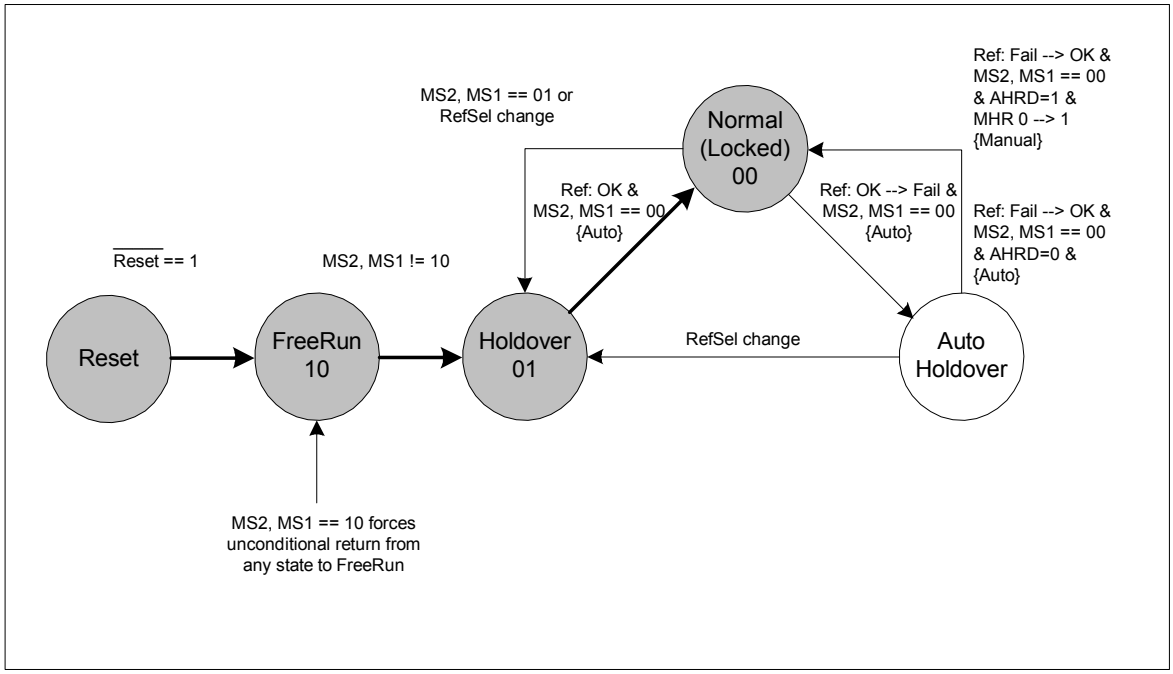


Figure 7 - Transition from Free-Run to Normal Mode

3.1.2 Single Reference Operation: NORMAL --> AUTO HOLDOVER --> NORMAL

The Normal to Auto-Holdover to Normal transition will usually happen when the Network Element loses its single reference clock unexpectedly or when it has two references but switching to the secondary reference is not a desirable option.

The sequence starts with the unexpected failure of a reference signal shown as transition OK --> FAIL in Figure 8 “Automatic entry into Auto Holdover State and recovery into Normal mode” at a time when ZL30461 operates in Normal Mode. This failure is detected by the active Acquisition PLL based on the following FAIL criteria:

- Frequency offset on 8 kHz, 1.544 MHz, 2.048 MHz and 19.44 MHz reference clocks exceeds ±30000 ppm (±3%).
- Phase hit on 1.544 MHz, 2.048 MHz and 19.44 MHz exceeds half of the cycle of the reference clock.

After detecting any of these anomalies on a reference clock the Acquisition PLL will switch itself into Holdover state forcing the Core PLL to automatically switch into the Auto Holdover state. This condition is flagged by LOCK = 0 and HOLDOVER = 1.

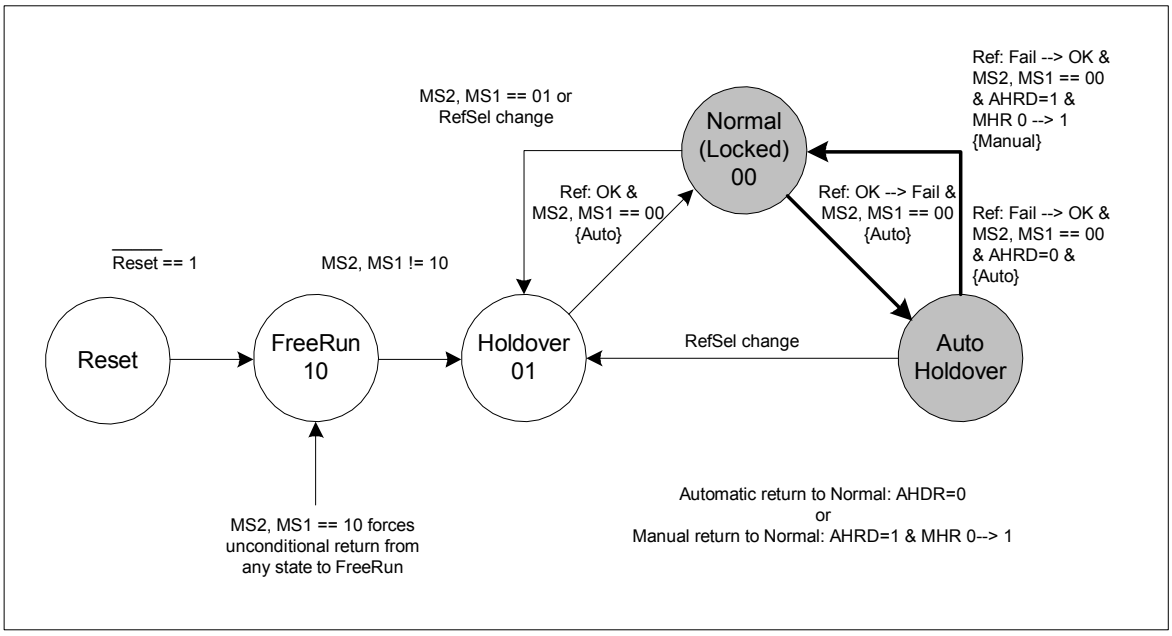


Figure 8 - Automatic Entry into Auto Holdover State and Recovery into Normal Mode

There are two possible returns to Normal Mode after the reference signal is restored:

- With the AHRD (Automatic Holdover Return Disable) bit set to 0. In this case, the Core PLL will automatically return to the Normal state after the reference signal recovers from failure. This transition is shown on the state diagram as a FAIL --> OK change. This change becomes effective when the reference is restored and there have been no phase hits detected for at least 64 clock cycles.
- With the AHRD bit set to 1 to disable automatic return to Normal state and the change of MHR (Manual Holdover Release) bit from 0 to 1 to trigger the transition from Auto Holdover to Normal state. This option is provided to protect the Core PLL from toggling between Normal and Auto Holdover states in case of an intermittent quality reference. In the case when MHR has been changed when the reference is still not available (Acquisition PLL in Holdover state), the transition to Normal state will not occur and MHR 0 to 1 transition must be repeated.

This transition from Auto Holdover to Normal state is performed as “hitless” reference switching.

3.1.3 Dual Reference Operation: NORMAL --> AUTO HOLDOVER --> HOLDOVER --> NORMAL

The Normal to Auto-Holdover to Holdover to Normal sequence represents the most likely operation of ZL30461 in Network Equipment.

The sequence starts from the Normal state and transitions to Auto Holdover state due to an unforeseen loss of reference. The failure conditions triggering this transition were described in Section 3.1.2. When in the Auto Holdover state, the ZL30461 can return to Normal state automatically if the lost reference is restored and the ADHR bit is set to 0. If the reference clock failure persists for a period of time that exceeds the system design limit, the system control processor may initiate a reference switch. If the secondary reference is available the ZL30461 will briefly switch into Holdover state and then transition to Normal state.

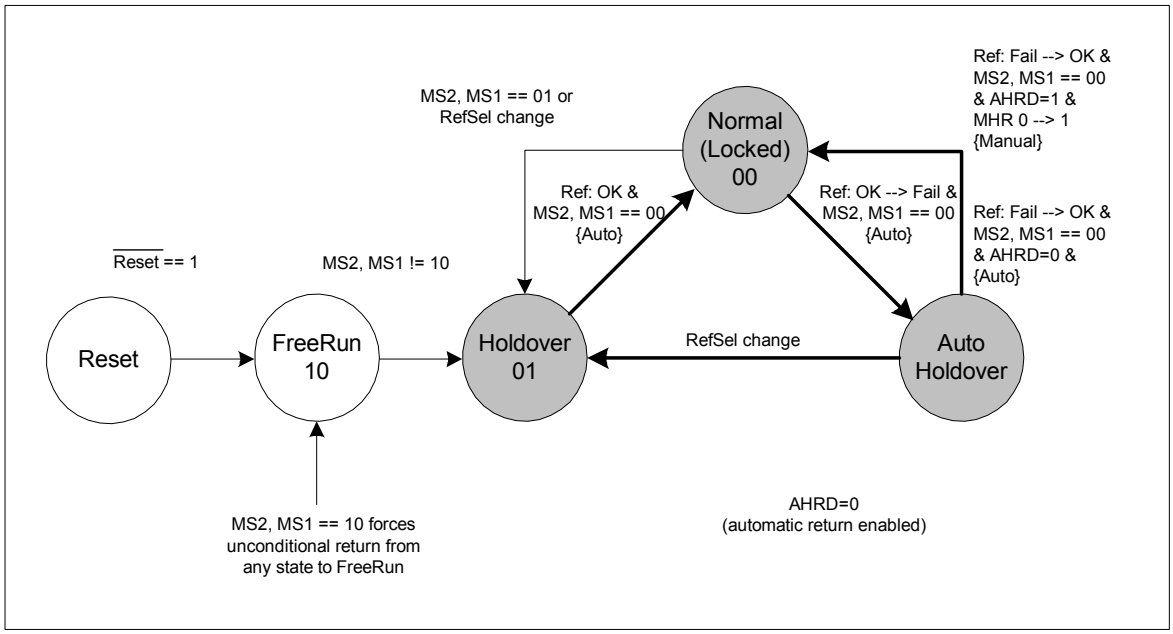


Figure 9 - Entry into Auto Holdover State and Recovery into Normal Mode by Switching References

The new reference clock will most likely have a different phase, but it may also have a different fractional frequency offset. To lock to a new reference with a different frequency, the Core PLL will step gradually towards the new frequency. The frequency slope will be limited to less than 2.0 ppm/sec.

3.1.4 Reference Switching (RefSel): NORMAL --> HOLDOVER --> NORMAL

The Normal to Holdover to Normal sequence switching is usually performed when:

- A reference clock is available but its frequency drifts beyond some specified limit. In a Network Element with Stratum 3 internal clocks, the reference failure is declared when its frequency drifts more than ±12 ppm beyond its nominal frequency. The ZL30461 indicates this condition by setting PRIOR or SECOR status bits and pins to logic 1.
- During routine maintenance of equipment orderly switching of reference clocks is possible. This may occur when synchronization references must be rearranged or when a faulty line card must be replaced.

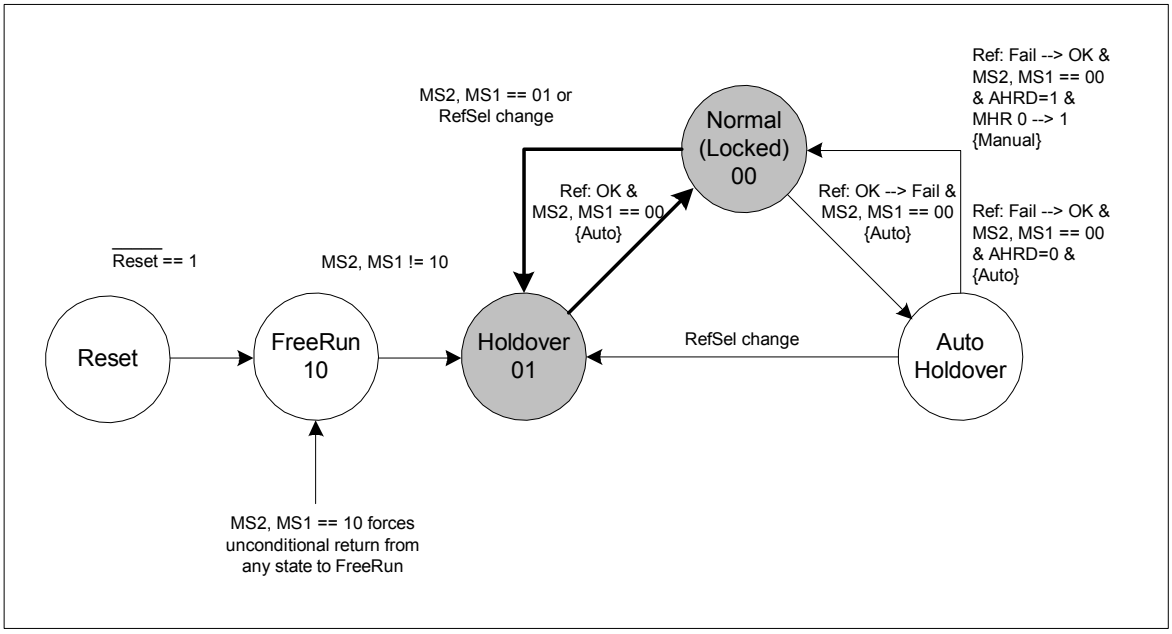


Figure 10 - Manual Reference Switching

Two types of transitions are possible:

- Semi-automatic transition, which involves changing RefSel input to select a secondary reference clock without changing the mode select inputs MS2, MS1 = 00 (Normal Mode). This forces ZL30461 to momentarily transition through the Holdover state and automatically return to Normal state after synchronizing to a secondary reference clock.
- Manual transition, which involves switching into Holdover Mode (MS2, MS1 = 01), changing references with RefSel, and manual return to the Normal Mode (MS2, MS1 = 00).

In both cases, the change of references provides “hitless” switching.

3.2 Master/Slave Timing Protection Switching

Carrier-Class Telecommunications Equipment deployed in today’s networks guarantee better than 99.999% operational availability (equivalent to less than 7 minutes of downtime per year). This high level of uninterrupted service is achieved by fully redundant architectures with hot swappable cards. Timing for these types of systems can be generated by the ZL30461, which supports Master/Slave Timing Protection Switching, shown in Figure 11.

The redundant architecture shown in this figure is based on the ZL30461 being deployed on two separate timing cards; the Master Timing Card and the Slave Timing Card. In normal operation, the Master Timing Card receives synchronization from the network and provides timing for the whole system. All Line Cards in the system are configured to receive from the backplane a reference clock generated by the Master Timing Card. The redundant Slave Timing Card is phase locked (through the SEC input) to one of the backplane clocks supplied by the Master Timing Card. The ZL30461 on the Slave Timing Card is programmed for 12 Hz loop filter operation (FCS2=1, FCS=0) which allows it to track the Master Timing Card clocks with minimal phase error.

When the Master Timing card fails unexpectedly, (this failure is not related to reference failure), then all Line Cards will detect this failure and they will switch to the timing supplied by the Slave Timing Card. At this moment the ZL30461 on the Slave Timing Card must be switched from 12 Hz to the same loop filter characteristic (e.g. 1.5 Hz filter for SDH networks) as the Master Timing Card.

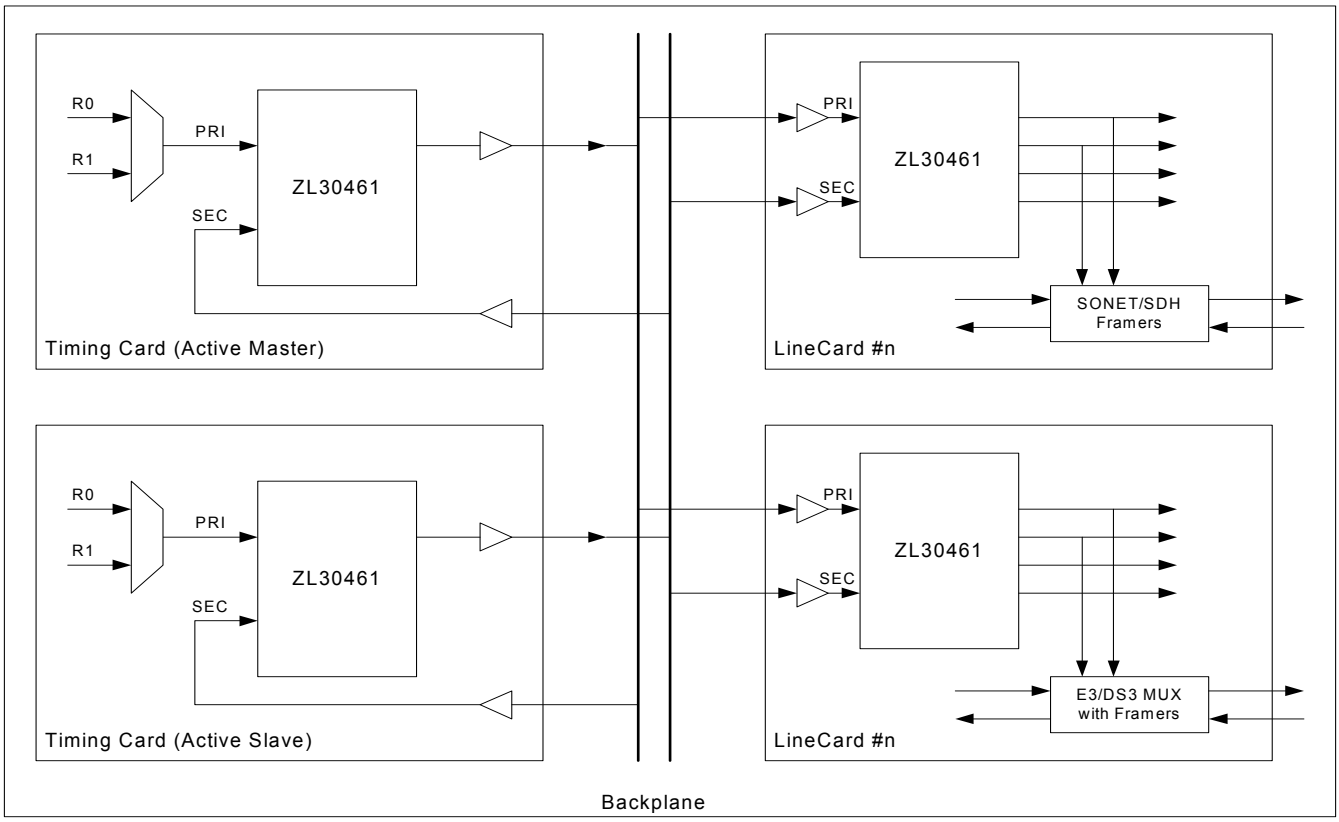


Figure 11 - Block Diagram of the Master/Slave Timing Protection Switching

A detailed description of this Master/Slave redundant timing architecture based on ZL30461 can be found in Application Note ZLAN-67 “Applications of the ZL30461 Master/Slave Application”.

3.3 Programming Master Clock Oscillator Frequency Calibration Register

The Master Crystal Oscillator and its programmable Master Clock Frequency Calibration register (see Table 19, Table 20, Table 21, and Table 22) have been described in Section 1.6 “TCXO and Master Clock Frequency Calibration Circuit”. Programming of this register should be done after system has been powered long enough for the Master Crystal Oscillator to reach a steady operating temperature. When the temperature stabilizes the crystal oscillator frequency should be measured with an accurate frequency meter. The frequency measurement should be substituted for the f_{offset} variable in the following equation.

$$MCFC = 45036 * f_{offset} \quad \text{(EQ 2)}$$

where f_{offset} is the crystal oscillator frequency offset from the nominal 20 000 000 Hz frequency expressed in Hz.

Example 1: Calculate the binary value that must be written to the MCFC register to correct a +1 ppm offset of the Master Crystal Oscillator. The +1 ppm offset for a 20 MHz frequency is equivalent to 20 Hz:

$$MCFC = 45036 * 20 = 900720 = 00\ 0D\ BE\ 70\ H \quad \text{(EQ 3)}$$

Example 2: Calculate the binary value that must be written to the MCFC register to correct a -2 ppm offset of the Master Crystal Oscillator. The -2 ppm offset for 20 MHz frequency is equivalent to -40 Hz:

$$MCFC = 45036 * (-40) = -1801440 = FF\ E4\ 83\ 20\ H \quad \text{(EQ 4)}$$

4.0 Characteristics

4.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltages	V_{DD} AV_{DD} TV_{DD}	-0.3	5.0	V
2	Input Voltage	V_{IN}	-0.05	V_{DD}+0.5	V

* Voltages are with respect to ground (GND) unless otherwise stated.
* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions*

	Parameter	Symbol	Min.	Typ.	Max.	Units
1	Supply Voltages	V_{DD} AV_{DD} TV_{DD}	3.135	3.3	3.465	V
2	Operating Temperature	T_A	0	25	70	^oC

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Current	I_{DD}			450	mA	Output unloaded
2	Supply Current	TI_{DD}			20	mA	Output unloaded
3	High-level input voltage	V_{IH}	$0.7V_{DD}$			V	
4	Low-level input voltage	V_{IL}			$0.3V_{DD}$	V	
5	Input leakage current	I_{IL}			15	µA	V_I=V_{DD} or GND
6	High-level output voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
7	Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
8	LVDS: Differential output voltage	V_{OD}	250		450	mV	Z_T=100 Ohms
9	LVDS: Change in VOD between complementary output states	dV_{OD}			50	mV	Z_T=100 Ohms
10	LVDS: Offset voltage	V_{OS}	1.125		1.375	V	Note 1
11	LVDS: Output short circuit current	I_{OS}			24	mA	Pin short to GND

DC Electrical Characteristics* (continued)

	Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Conditions
12	LVDS: Output rise and fall times	T_{RF}	260		900	ps	Note 2
13	LVPECL: Differential output voltage	$\|V_{OD}\|$	480	600	720	mV	Z_T=100 Ohms
14	LVPECL: High-level output voltage	V_{OH}		V_{DD}-0.9		V	Z_T=100 Ohms
15	LVPECL: Low-level output voltage	V_{OL}		V_{DD}-1.5		V	
16	LVPECL: Output rise and fall times	T_{RF}	200			ps	Note 2

* Voltages are with respect to ground (GND) unless otherwise stated.
Note 1: VOS is defined as (V_{OH} + V_{OL}) / 2.
Note 2: Rise and fall times are measured at 20% and 80% levels.

AC Electrical Characteristics*

	Parameter	Symbol	Min.	Max.	Units	Test Conditions
1	I/P Frequency Range	F_{IN}			Hz	Note 3
2	O/P Frequency Range	F_{OUT}			Hz	Note 4
3	Reference Rejection	R_{REJ}				GR-1244 3.5: R3-36 G.813 6.3a
4	Reference Pull-in	R_{PULL}				GR-1244 3.5: R3-37 GR-253 5.4.4.2.3: R5-126 G.813 6.1a,b
5	Reference Hold-in	R_{HOLD}				GR-1244 3.5: R3-38 GR-253 5.4.4.2.3: R5-126 G.813 6.2b
6	Reference Settling Time	R_{STIME}				GR-1244 3.5: R3-39 GR-253 5.4.4.2.3: R5-128
7	Jitter Tolerance	J_T				GR-1244 4.2: R4-2, CR4-3, R4-4 GR-253 5.6.2.2: R5-240, R5-241 G.813 8.2a,b
8	Wander Tolerance	W_{TOL}				GR-1244 4.3: R4-5 GR-253 5.4.4.2.4: R5-129 G.813 8.1 a,b
9	Phase Transient Tolerance	P_{TT}				GR-1244 4.4: R4-7 GR-253 5.4.4.3.3: R5-135

AC Electrical Characteristics* (continued)

	Parameter	Symbol	Min.	Max.	Units	Test Conditions
10	Free-Run Accuracy	F_A				GR-1244 5.1: R5-1 GR-253 5.4.4.1: R5-117 G.813 5a
11	Holdover Frequency Stability	H_{ST}				GR-1244 5.2: R5-2 GR-253 5.4.4.2.2: R5-123, R5-124, R5-125 G.813 10.2a,b
12	Holdover Entry Phase Transient	H_{EPT}				GR-1244 5.6: R5-12 GR-253 5.4.4.2.2: R5-122 G.813 10.2b
13	Wander Generation	W_{GEN}				GR-1244 5.3: R5-4, R5-5 GR-253 5.4.4.3.2: R5-133, R5-134 G.813 7.1 a,b
14	Wander Transfer	W_{TR}				GR-1244 5.4: R5-6 GR-253 5.4.4.2.4: R5-129, R5-130, R5-131 G.813 9.0 a,b
15	Jitter Generation	J_G				GR-1244 5.5: R5-7 GR-253 5.6.1: R5-235 G.813 7.3a,b
16	Phase Transient Generation (Holdover to Normal transition)	PT_{G1}				GR-1244 5.6: R5-10, O5-11, R5-14 GR-235 5.4.4.3.3: R5-136, O5-137
17	Phase Transient Generation (Alternate Reference)	PT_{G2}				GR-1244 5.6: R5-10, O5-11, R5-14 GR-235 5.4.4.3.3: R5-136, O5-137 G.813 10.1 a,b
18	Phase Transient Generation (Input Transient)	PT_{G3}				GR-1244 5.6: R5-10, O5-11, R5-14 GR-235 5.4.4.3.3: R5-136, O5-137
19	Phase Transient Generation (Input Interruptions)	PT_{G3}				G.813 10.3 a
20	Phase Changes (during pull-in)	P_C				GR-1244 5.8: R5-17
21	Lock Time	L_T		100	s	
22	Tuning Alarm	T_A	-12	+12	ppm	Note 5

* Voltages are with respect to ground (GND) unless otherwise stated.
Note 3: 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz.
Note 4: Various outputs from 8 kHz to 155.52 MHz.
Note 5: With reference to the Free-Run accuracy.

AC Electrical Characteristics - Timing Parameter Measurements - CMOS Voltage Levels*

	Characteristics	Symbol	Typical	Units
1	Threshold voltage	V_T	$0.5V_{DD}$	V
2	Rise and fall threshold voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and fall threshold voltage Low	V_{LM}	$0.3V_{DD}$	V

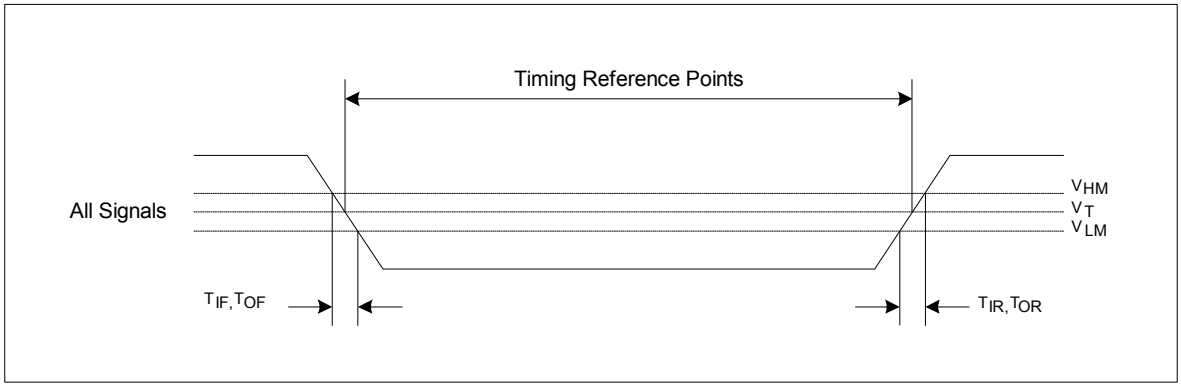


Figure 12 - Timing Parameters Measurement Voltage Levels

AC Electrical Characteristics - Microprocessor Timing*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	$\overline{DS}$ low	t_{DSL}	65		ns	
2	$\overline{DS}$ high	t_{DSH}	100		ns	
3	$\overline{CS}$ setup	t_{CSS}	0		ns	
4	$\overline{DS}$ hold	t_{CSH}	0		ns	
5	R/$\overline{W}$ setup	t_{RWS}	20		ns	
6	R/$\overline{W}$ hold	t_{RWH}	5		ns	
7	Address setup	t_{ADS}	10		ns	
8	Address hold	t_{ADH}	10		ns	
9	Data read delay	t_{DRD}		60	ns	C_L = 150 pF
10	Data read hold	t_{DRH}		10	ns	
11	Data write setup	t_{DWS}	10		ns	
12	Data write hold	t_{DWH}	5		ns	

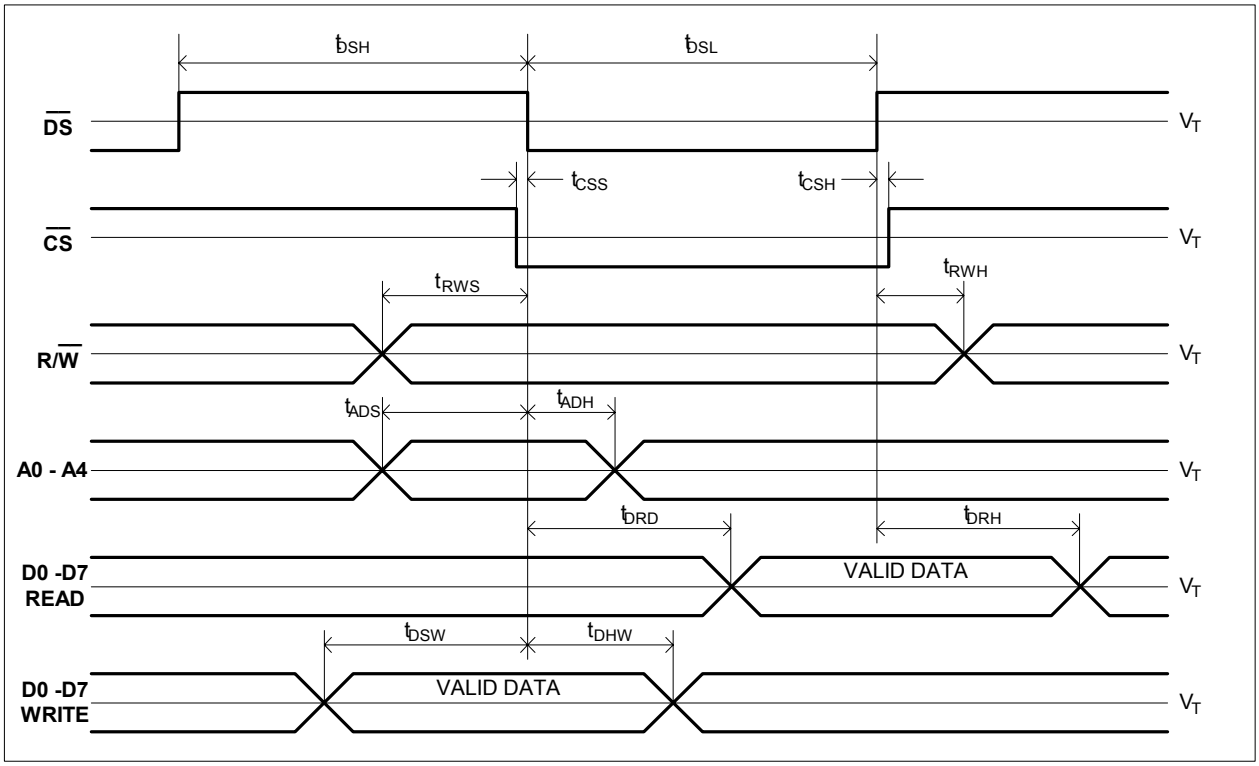


Figure 13 - Microport Timing

AC Electrical Characteristics - ST-BUS and GCI Output Timing*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	$\overline{\text{F16o}}$ pulse width low	t_{F16L}	56	62	ns	
2	F8o to $\overline{\text{F16o}}$ delay	t_{F16D}	27	33	ns	
3	$\overline{\text{C16o}}$ pulse width low	t_{C16L}	26	32	ns	
4	F8o to $\overline{\text{C16o}}$ delay	t_{C16D}	-3	3	ns	
5	F8o pulse width high	t_{F8H}	119	125	ns	
6	C8o pulse width low	t_{C8L}	56	62	ns	
7	F8o to C8o delay	t_{C8D}	-3	3	ns	
8	$\overline{\text{F0o}}$ pulse width low	t_{F0L}	241	247	ns	
9	F8o to $\overline{\text{F0o}}$ delay	t_{F0D}	119	125	ns	
10	$\overline{\text{C4o}}$ pulse width low	t_{C4L}	119	125	ns	
11	F8o to $\overline{\text{C4o}}$ delay	t_{C4D}	-3	3	ns	
12	C2o pulse width low	t_{C2L}	240	246	ns	
13	F8o to C2o delay	t_{C2D}	-3	3	ns	

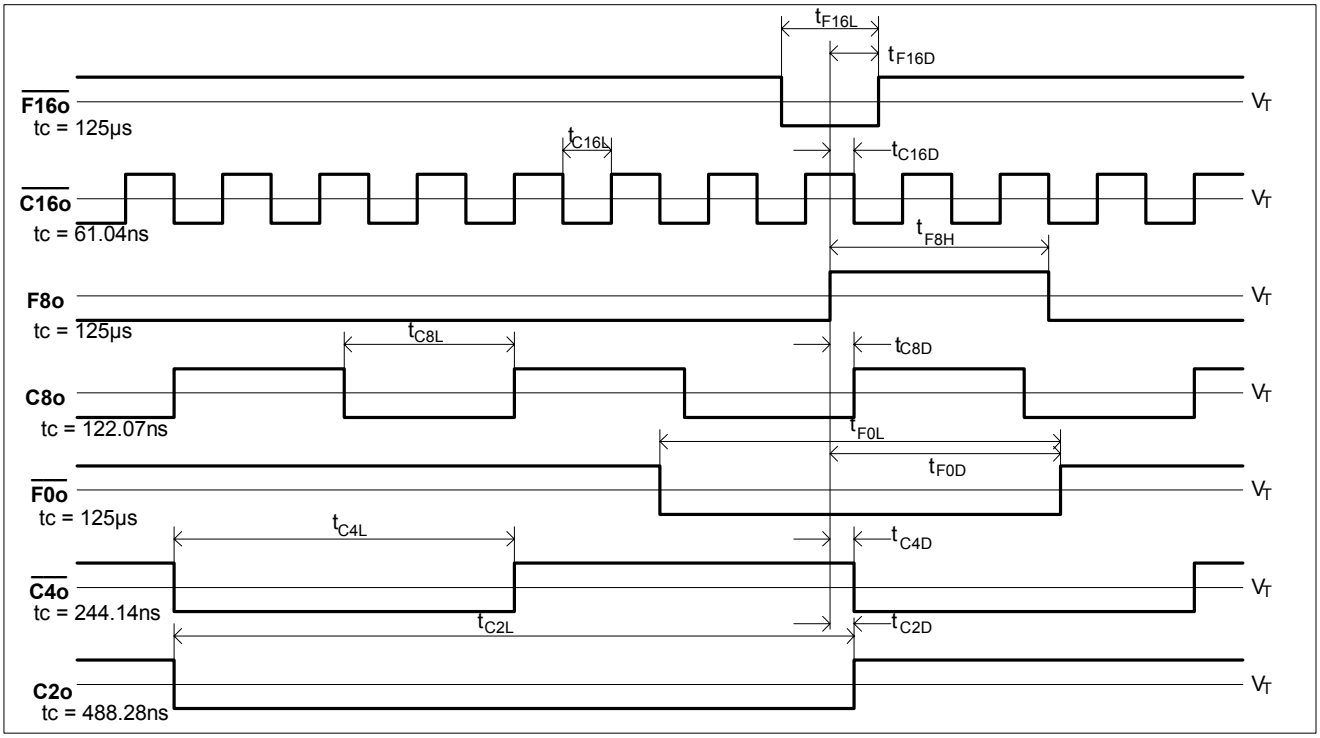


Figure 14 - ST-BUS and GCI Output Timing

AC Electrical Characteristics - DS1, DS2 and C19o Clock Timing*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	C6o pulse width low	t_{C6L}	75	83	ns	
2	F8o to C6o delay	t_{C6D}	-4	11	ns	
3	C1.5o pulse width low	$t_{C1.5L}$	320	328	ns	
4	F8o to C1.5o delay	$t_{C1.5D}$	-4	11	ns	
5	C19o pulse width high	t_{C19H}	23	29	ns	
6	F8o to C19o delay	t_{C19D}	-5	7	ns	

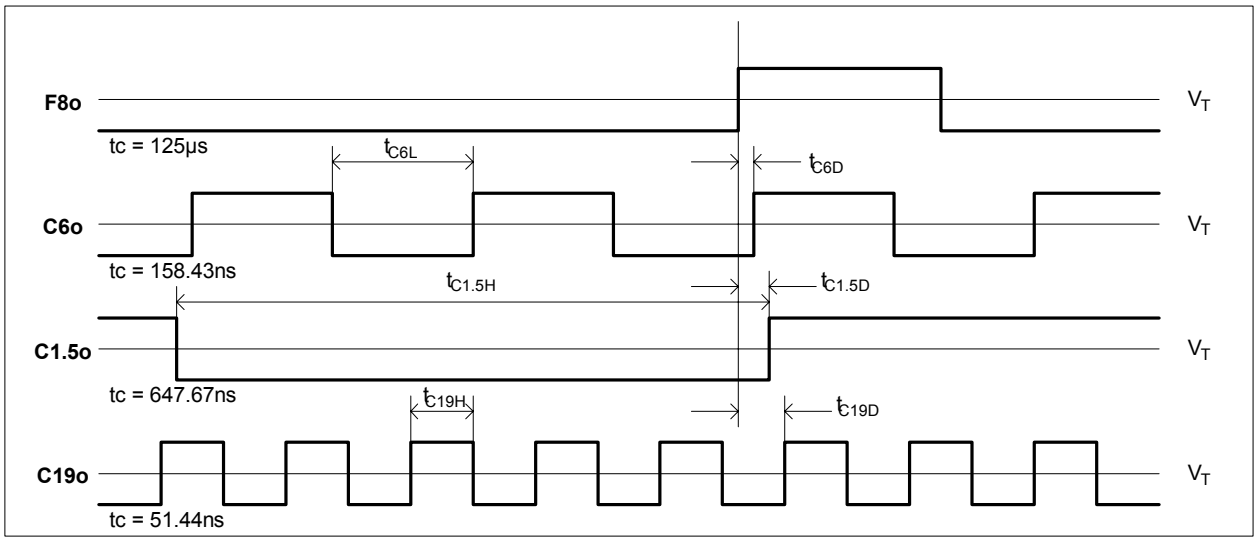


Figure 15 - DS1, DS2 and C19o Clock Timing

AC Electrical Characteristics - C155o and C19o Clock Timing*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	C155o pulse width low	t_{C155L}	2.6	3.8	ns	
2	C1550 to C19o rising edge delay	t_{C19DLH}	-1	7	ns	
3	C155o to C19o falling edge delay	t_{C19DHL}	-2	6	ns	

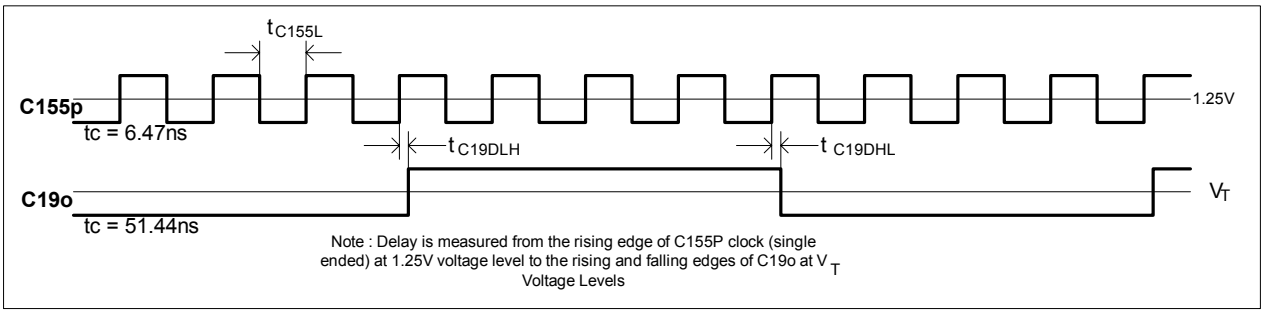


Figure 16 - C155o and C19o Timing

AC Electrical Characteristics - Input to Output Phase Alignment ($\overline{\text{RefAlign}}$ change from 1 to 0)*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	8 kHz ref pulse width high	t_{R8H}	100		ns	
2	8 kHz to F8o ref input delay	t_{R8D}	-6	29	ns	
3	1.544 MHz ref pulse width high	$t_{R1.5H}$	100		ns	
4	1.544 MHz ref input to F8o delay	$t_{R1.5D}$	335	350	ns	
5	2.048 MHz ref pulse width high	t_{R2H}	100		ns	
6	2.048 MHz ref input to F8o delay	t_{R2D}	225	272	ns	
7	19.44 MHz ref pulse width high	t_{R19H}	20		ns	
8	19.44 MHz to F8o input delay	t_{R19D}	8	21	ns	
9	19.44 MHz ref input to C19o delay	$t_{R19C19D}$	6	21	ns	
10	Reference input rise and fall time	t_{IR}, t_{IF}		10	ns	

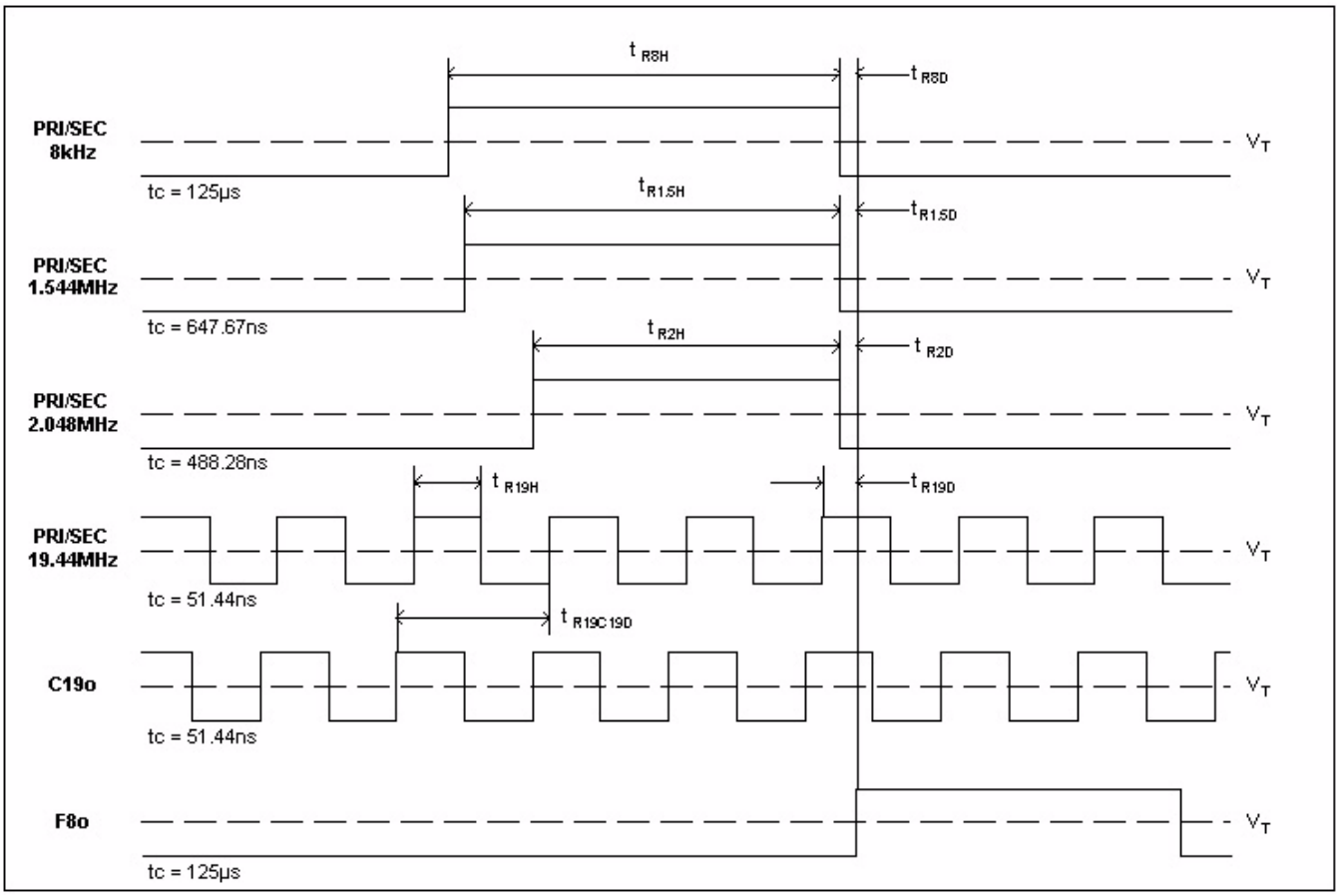


Figure 17 - Input Reference to Output Clock Phase Alignment

AC Electrical Characteristics - Input Control Timing*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	Input control setup time	t_S	100		ns	
2	Input control hold time	t_H	100		ns	

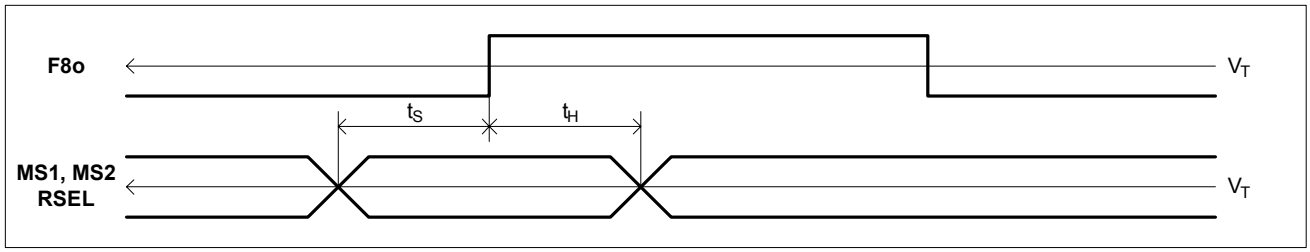


Figure 18 - Input Control Signal Setup and Hold Time

AC Electrical Characteristics - E3 and DS3 Output Timing*

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	C44o clock pulse width high	t_{C44H}	11	13	ns	
2	C11o clock pulse width high	t_{C11H}	5	26	ns	
3	C34o clock pulse width high	t_{C34H}	13	16	ns	
4	C8.5o clock pulse width high	$t_{C8.5H}$	9	24	ns	

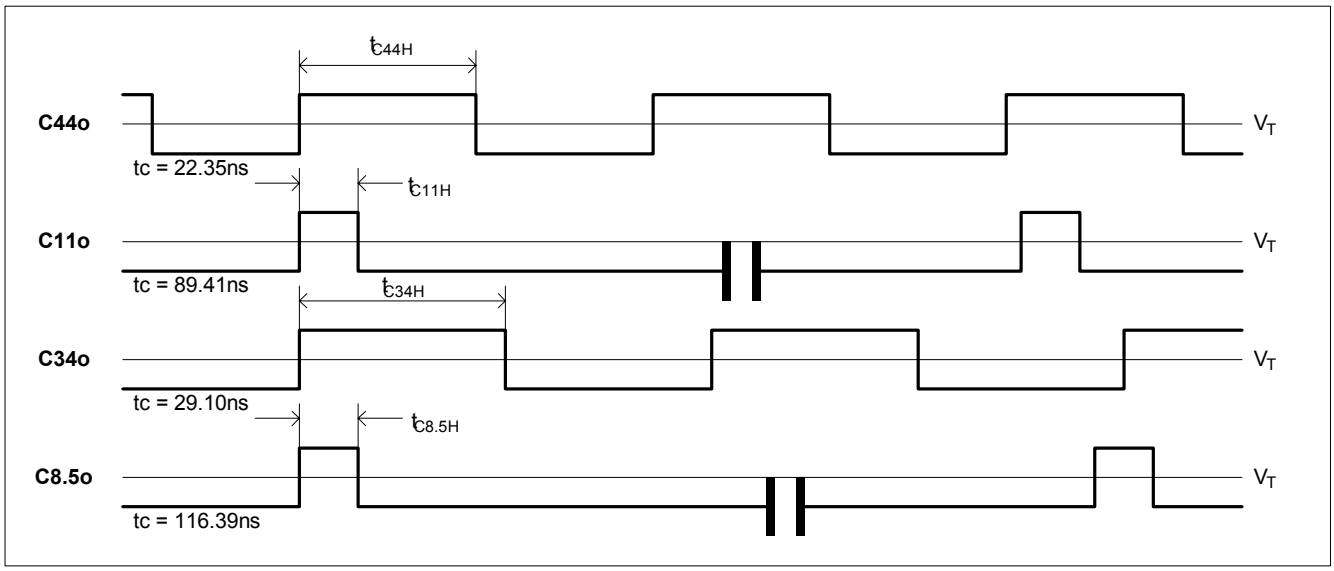


Figure 19 - E3 and DS3 Output Timing

4.2 Performance Characteristics

Performance Characteristics - Mode Switching*

	Characteristics	Typical	Units	Test Conditions
1	Core PLL Holdover accuracy	0.000032	ppm	
2	Holdover stability	±4.6	ppm	Determined by stability of the on-board TCXO
3	Frequency limit range (LOCK pin and FLIM bit)	±104	ppm	Relative to OSCi
4	Capture range (TRUELOCK bit)	±142	ppm	Relative to OSCi
5	Reference Acceptance Threshold	±12	ppm	Relative to OSCi Tested without presence of jitter on reference clock
	Lock time			
6	6 Hz or 12 Hz Filter	6	s	

Performance Characteristics - Mode Switching* (continued)

	Characteristics	Typical	Units	Test Conditions
7	1.5 Hz Filter	20	s	
8	0.1 Hz Filter	75	s	
	Output Phase Continuity (MTIE)			
9	Reference switching: PRI => SEC, SEC => PRI	50 5	ns ns	PRI = SEC = 8 kHz PRI or SEC = 1.544 MHz, 2.048 MHz, 19.44 MHz
10	Switching from Normal Mode to Holdover Mode	0	ns	
11	Switching from Holdover Mode to Normal Mode	50 2	ns ns	PRI = SEC = 8 kHz PRI or SEC = 1.544 MHz, 2.048 MHz, 19.44 MHz (for 0 ppm frequency offset)
	Output Phase Slope			
12	0.1 Hz Filter	885	$\frac{ns}{sec}$	G.813 Option 2 GR-253 SONET Stratum 3 GR-253 SONET SMC
13	1.5 Hz Filter	41	$\frac{ns}{1.326ms}$	G.813 Option 1, GR-1244 Stratum 3, Note 6
14	6 Hz Filter	50	$\frac{ns}{sec}$	G.813 Option 1, Note 6
15	12 Hz Filter	1200	$\frac{\mu s}{sec}$	

Note 6: The phase slope is less than 7.5 ppm if the step in phase is less than 120 ns.

Performance Characteristics: Measured Output Jitter - GR-253-CORE and T1.105.03 conformance*

Telcordia GR-253-CORE and ANSI T1.105.03 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C155o Clock Output		
1	OC-3 155.52 Mbps	65 kHz to 1.3 MHz	0.15 UI_{PP}	0.964	0.425	ns_{P-P}	
					0.048	ns_{RMS}	
2		12 kHz to1.3 MHz (Category II)	0.1 UI_{PP}	0.643	0.508	ns_{P-P}	
			0.01 UI_{RMS}	0.064	0.048	ns_{RMS}	
3		500 Hz to 1.3 MHz	1.5 UI_{PP}	9.645	0.548	ns_{P-P}	
					0.063	ns_{RMS}	
					JA77P/N Clock Output		
4	OC-12 622.08 Mbps	12 kHz to 5 MHz (Category II)	0.1 UI_{PP}	161	34.9	ps_{P-P}	
					2.8	ps_{RMS}	
					JA19Mo Clock Output		
5	OC-12 622.08 Mbps	12 kHz to 5 MHz (Category II)	0.1 UI_{PP}	161	91.68	ps_{P-P}	
					7.06	ps_{RMS}	
					C19o Clock Output		
6	OC-3 155.52 Mbps	65 kHz to 1.3 MHz	0.15 UI_{PP}	0.964	0.886	ns_{P-P}	
					0.146	ns_{RMS}	
7		12 kHz to1.3 MHz (Category II)	0.1 UI_{PP}	0.643	0.909	ns_{P-P}	
			0.01 UI_{RMS}	0.064	0.149	ns_{RMS}	
8		500 Hz to 1.3 MHz	1.5 UI_{PP}	9.645	0.973	ns_{P-P}	
					0.151	ns_{RMS}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - T1.403 Conformance*

ANSI T1.403 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C1.5o Clock Output		
1	DS1 1.544 Mbps	8 kHz to 40 kHz	0.07 UI_{PP}	45.3	0.922	ns_{P-P}	
2		10 Hz to 40 kHz	0.5 UI_{PP}	324	1.45	ns_{P-P}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - G.747 Conformance*

ITU-T G.747 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C6o Clock Output		
1	6312 kbps (DS2)	10 Hz to 60 kHz	0.05 UI_{PP}	7.92	1.96	ns_{P-P}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - T1.404 Conformance*

ANSI T1.404 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C44o Clock Output		
1	DS3 44.736 Mbps	30 kHz to 400kHz	0.05 UI_{PP}	1.12	0.892	ns_{P-P}	
2		10 Hz to 400 kHz	0.5 UI_{PP}	11.2	1.5	ns_{P-P}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - G.732, G.735 to G.739 Conformance*

ITU-T G.732, G.735, G.736, G.737, G.738, G739 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					$\overline{C16o}$, C8, $\overline{C4}$ and C2 Clock Outputs		
1	E1 2048 kbits/s	20 Hz to 100 kHz	0.05 UI_{PP}	24.4	1.26	ns_{P-P}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - G.751 Conformance*

ITU-T G.751 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C34 Clock Outputs		
1	E3 34368 kbits/s	100 Hz to 800 kHz	0.05 UI_{PP}	1.45	1.04	ns_{P-P}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

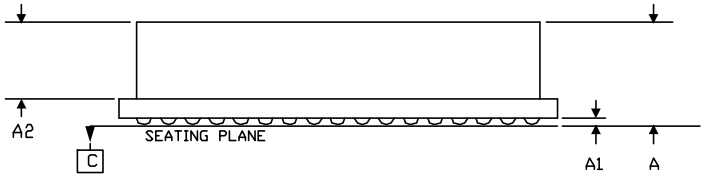
Performance Characteristics: Measured Output Jitter - G.813 conformance - Option 1

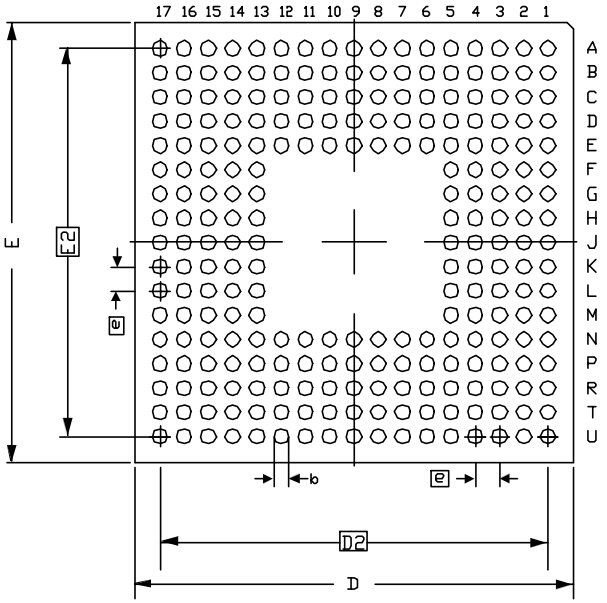
ITU-T G.813 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C155o Clock Output		
1	STM-1 155.52 Mbps	65 kHz to 1.3 MHz	0.1 UI_{PP}	0.643	0.425	ns_{P-P}	
					0.048	ns_{RMS}	
2		500 Hz to 1.3 MHz	0.5 UI_{PP}	3.215	0.548	ns_{P-P}	
					0.063	ns_{RMS}	
					JA77P/N Clock Output		
3	STM-4 622.08 Mbps	250 kHz to 5 MHz	0.1 UI_{PP}	161	20.32	ps_{P-P}	
					1.516	ps_{RMS}	
4		5 kHz to 20 MHz	0.5 UI_{PP}	804	86.36	ps_{P-P}	
					6.8	ps_{RMS}	
					JA19Mo Clock Output		
5	STM-4 622.08 Mbps	250 kHz to 5 MHz	0.1 UI_{PP}	161	81.5	ps_{P-P}	
					6.7	ps_{RMS}	
6		5 kHz to 20 MHz	0.5 UI_{PP}	804	177.8	ps_{P-P}	
					14	ps_{RMS}	
					C19o Clock Output		
7	STM-1 155.52 Mbps	65 kHz to 1.3 MHz	0.1 UI_{PP}	0.643	0.866	ns_{P-P}	
					0.146	ns_{RMS}	
8		500 Hz to 1.3 MHz	0.5 UI_{PP}	3.215	0.973	ns_{P-P}	
					0.151	ns_{RMS}	
					$\overline{C16o}$, C8o, $\overline{C4o}$ and C2o Clock Output		
9	E1 2048 kbps	20 Hz to 100 kHz	0.05 UI_{PP}	24.4	1.26	ns_{P-P}	

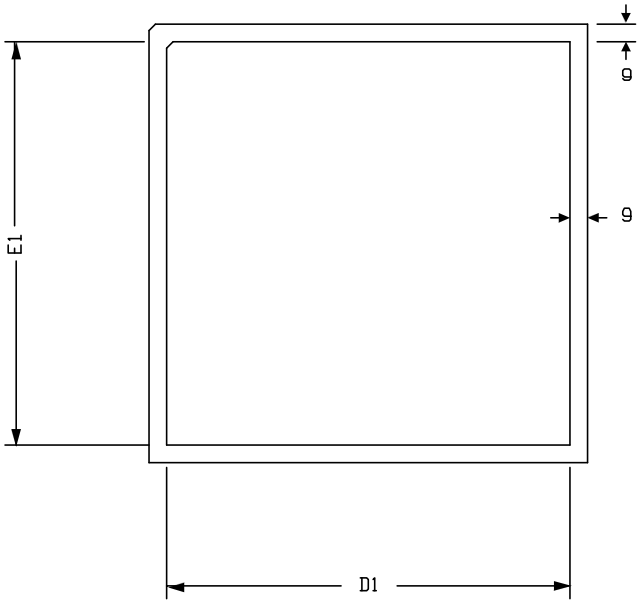
* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - G.813 Conformance - Option 2

ITU-T G.813 Jitter Generation Requirements					ZL30461 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					C155o Clock Output		
1	STM-1 155.52 Mbps	12 kHz to 1.3 MHz	0.1 UI_{PP}	0.643	0.508	ns_{P-P}	
					0.058	ns_{RMS}	
					JA77P/N Clock Output		
2	STM-4 622.08 Mbps	12 kHz to 5 MHz	0.1 UI_{PP}	161	34.9	ps_{P-P}	
					2.8	ps_{RMS}	
					JA19Mo Clock Output		
3	STM-4 622.08 Mbps	12 kHz to 5 MHz	0.1 UI_{PP}	161	91.68	ps_{P-P}	
					7.06	ps_{RMS}	
					C19o Clock Output		
4	STM-1 155.52 Mbps	12 kHz to 1.3 MHz	0.1 UI_{PP}	0.643	0.500	ns_{P-P}	
					0.071	ns_{RMS}	







DIMENSION	MIN	NOM	MAX
A	5.25	5.75	6.25
A1	0.35	——	——
A2	3.80	4.00	4.20
D	22.85	23.00	23.15
D1	21.90	22.00	22.10
D2		20.32 Ref	
E	22.85	23.00	23.15
E1	21.90	22.00	22.10
E2		20.32 Ref	
b	0.60	0.75	0.90
e		1.27 Ref	
g	——	0.50	——
N		240	
Drawing not to JEDEC Standard defined outline			

1. Controlling Dimensions are in mm
2. Dimension 'b' is measured at the maximum solder ball diameter
3. Primary Datum -C- and seating plane are defined by the spherical crowns of the solder balls
4. N is the number of solder balls
5. Not to scale
6. Substrate thickness is 1mm nominal

ISSUE	1			
ACN				
DATE	4-AUG-03			
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code MG

Previous package codes

Package Outline for ZL30461, 240 ball module with BGA (23.00 x 23.00 mm) 1.27 mm pitch

100875

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