Z86C28/E28

CMOS 8-BIT LOW-COST 4K-ROM MICROCONTROLLERS

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86C28	4	237	12	Optional	Optional
Z86E28	4†	237	12	Optional	Optional

Note: * General-Purpose
† One Time Programmable EPROM in DIP only.

- 18-Pin DIP and SOIC Packages (Z86C28)
- 18-Pin DIP Packages (Z86E28)
- 3.0V to 5.5V Operating Range (Z86C28)
  - 3.5V to 5.5V (Z86E28 Std. Temp.)
  - 4.5V to 5.5V (Z86E28 Ext. Temp.)
- Available Temperature Ranges
  - E = –40°C to +105°C (Extended Temperature)
  - S = 0°C to +70°C (Standard Temperature)
- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts from Six Different Sources
- Two On-Board Comparators
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Clock-Free WDT Reset
- Power-On Reset (POR) Timer
- Options:
  - RAM Protect
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator
  - 32 kHz Operation
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonance, LC, or External Clock Drive
- Low-Power Consumption (50 mw)
- Fast Instruction Pointer (1.0 µs @ 12 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered
- Software Enabled Watch-Dog Timer
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection

GENERAL DESCRIPTION

Zilog's Z86C28/E28 are members of the Z8® MCU family and offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the Z86C28/E28's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

Note: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

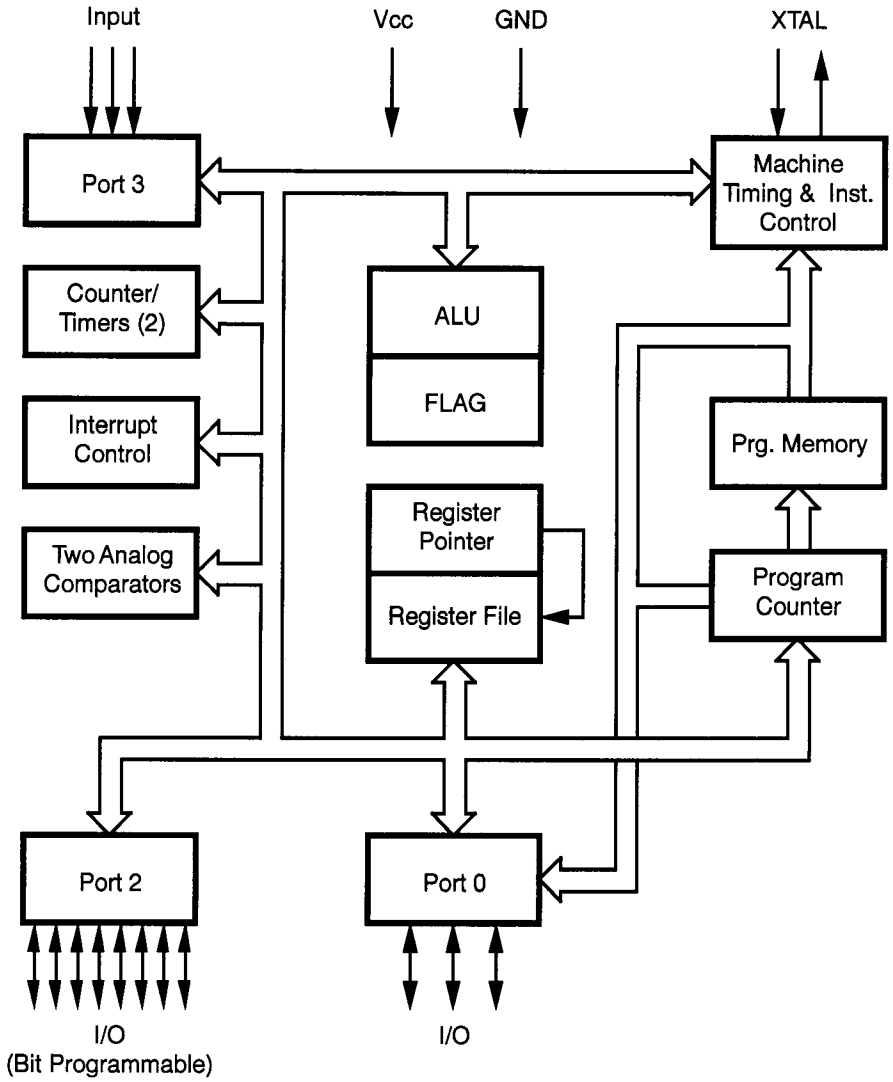

Figure 1. Z86C28/E28 Functional Block Diagram

PIN DESCRIPTIONS

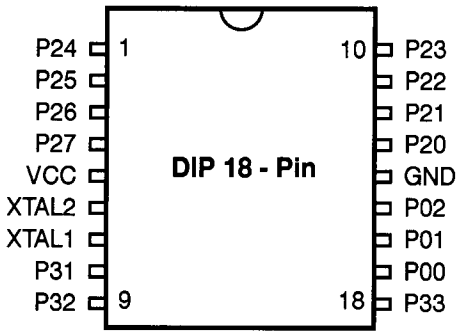

Figure 2. 18-Pin DIP/SOIC

Table 1: 18-Pin DIP and SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1, P32, P33 Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V_{SS}		220	mA
Maximum Allowable Current into V_{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowable Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA

Notes:
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

Total Power Dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})]
+ sum of [(V_{DD} – V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).

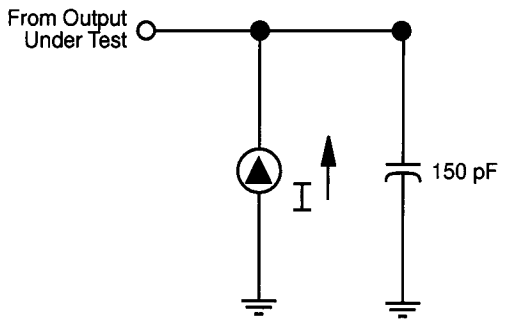

Figure 3. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A= 0 °C to +70 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}	0.9	V	Driven by	
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V	External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}	1.5	V		
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.3	V	I_{OH} = – 0.5 mA	
	Low EMI Mode	5.5V	V_{CC} -0.4		4.8	V		
V_{OH1}	Output High Voltage	3.5V	V_{CC}–0.4		3.3	V	I_{OH} = -2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = -2.0 mA	
V_{OL}	Output Low Voltage	3.5V		0.4	0.2	V	I_{OL} = +1.0 mA	
	Low EMI Mode	5.5V		0.4	0.2	V	I_{OL} = +1.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	I_{OL} = + 4.0 mA	8
		5.5V		0.4	0.1	V	I_{OL} = + 4.0 mA	8
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = + 10 mA	8
		5.5V		1.2	0.5	V	I_{OL} = + 10 mA	8
V_{OFFSET}	Comparator Input	3.5V		25	10	mV		
	Offset Voltage	5.5V		25	10	mV		
V_{ICR}	Input Common Mode	3.5V	0	V_{CC} -1.0V		V		10
	Voltage Range	5.5V	0	V_{CC} -1.0V		V		10
I_{IL}	Input Leakage	3.5V	–1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	0.032	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.5V		15	5	mA	@ 12 MHz	4,5
		5.5V		20	15	mA	@ 12 MHz	4,5
I_{CC1}	Standby Current	3.5V		4	2	mA	V_{IN} = 0V, V_{CC}	4,5
	Halt Mode	5.5V		6	4	mA	@ 12 MHz	4,5
		3.5V		3	1.5	mA	Clock Divide by	4,5
		5.5V		5	3	mA	16 @ 12 MHz	4,5

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A= 0 °C to +70 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC2}	Standby Current	3.5V		10	2	µA	V_{IN} = 0V, V_{CC}	6,11
	Stop Mode	5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	6,11
		3.5V		15	7	µA	V_{IN} = 0V, V_{CC}	6,11,13
		5.5V		30	10	µA	V_{IN} = 0V, V_{CC}	6,11,13
I_{ALL}	Auto Latch	3.5V	0.7	8	2.4	µA	0V <V_{IN}<V_{CC}	9
	Low Current	5.5V	1.4	15	4.7	µA	0V <V_{IN}<V_{CC}	9
I_{ALH}	Auto Latch	3.5V	–0.6	–5	–1.8	µA	0V<V_{IN}<V_{CC}	9
	High Current	5.5V	–1	–8	–3.8	µA	0V<V_{IN}<V_{CC}	9
T_{POR}	Power On Reset	3.5V	3.0	24	7	ms		
		5.5V	2.0	13	4	ms		
V_{LV}	Auto Reset Voltage		2.3	3.0	2.8	V		1,7

Notes:

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Max. temperature is 70°C.
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V and V_{CC} = 3.5V
13. WDT running

T_A=–40 °C to +105 °C

Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External	
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V	Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND-0.3	0.2 V_{CC}	1.5	V		
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = – 0.5 mA	8
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = – 0.5 mA	8
V_{OH1}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = +1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = +1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = + 4.0 mA	8
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = + 12 mA	8
		5.5V		1.2	0.5	V	I_{OL} = + 12 mA	8
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC}-1.5V		V		10
		5.5V	0	V_{CC}-1.5V		V		10
I_{IL}	Input Leakage	4.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	4,5
		5.5V		20	15	mA	@ 12 MHz	4,5

T_A=–40 °C to +105 °C

Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current Halt Mode	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	4,5
		5.5V		6	4	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	4,5
I_{CC2}	Standby Current (Stop Mode)	4.5V		10	2	µA	V_{IN} = 0V, V_{CC}	6,11
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	6,11
		4.5V		40	10	µA	V_{IN} = 0V, V_{CC}	6,11,13
		5.5V		40	10	µA	V_{IN} = 0V, V_{CC}	6,11,13
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	1.4	20	4.7	µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	4.5V	–1.0	–10	–3.8	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	–1.0	–10	–3.8	µA	$0V < V_{IN} < V_{CC}$	9
T_{POR}	Power On Reset	4.5V	2.0	14	4	ms		
		5.5V	2.0	14	4	ms		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		1

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V
13. WDT is not running.

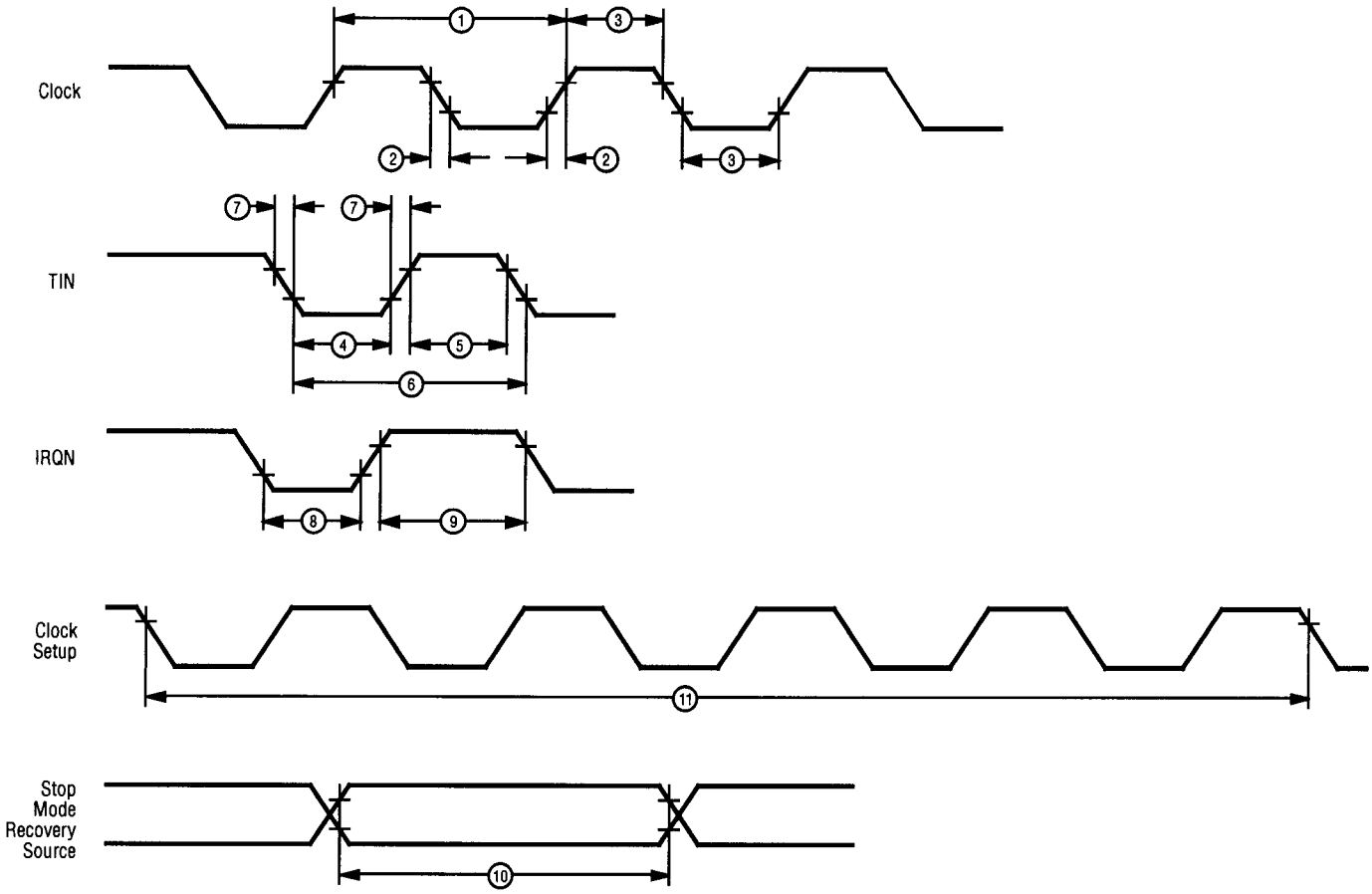

Figure 4. Additional Timing Diagram

Additional Timing Table (Divide-By-One Mode)

				T_A = 0 °C to +70 °C					
				4 MHz		6 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	1,7,8
			5.5V	250	DC	166	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise &	3.5V		25		25	ns	1,7,8
		Fall Times	5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low	3.5V	100		100		ns	1,7,8
		Width	5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High	3.5V	5TpC		5TpC			1,7,8
		Width	5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise	3.5V		100		100	ns	1,7,8
		& Fall Timer	5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low	3.5V	100		100		ns	1,2,7,8
		Time	5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low	3.5V	5TpC		5TpC			1,3,7,8
		Time	5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input	3.5V	5TpC		5TpC			1,2,7,8
		High Time	5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode	3.5V	12		12		ns	4,8
		Recovery Width	5.5V	12		12		ns	4,8
		Spec							
11	Tost	Oscillator Startup	3.5V		5TpC		5TpC		4,8,9
		Time	5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Additional Timing Table (Divide-By-One Mode)

				T_A = -40 °C to +105 °C					
				4 MHz		6 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	1,7,8
			5.5V	250	DC	166	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise &	4.5V		25		25	ns	1,7,8
		Fall Times	5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	4.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low	4.5V	100		100		ns	1,7,8
		Width	5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High	4.5V	5TpC		5TpC			1,7,8
		Width	5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise	4.5V		100		100	ns	1,7,8
		& Fall Timer	5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low	4.5V	100		100		ns	1,2,7,8
		Time	5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low	4.5V	5TpC		5TpC			1,3,7,8
		Time	5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input	4.5V	5TpC		5TpC			1,2,7,8
		High Time	5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode	4.5V	12		12		ns	4,8
		Recovery Width	5.5V	12		12		ns	4,8
		Spec							
11	Tost	Oscillator Startup	4.5V		5TpC		5TpC		4,8,9
		Time	5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Additional Timing Table (Divide by Two Mode)

				T_A = 0 °C to +70 °C						
				12 MHz		4 MHz				
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		1,7,8
			5.5V	62.5	DC	250	DC	ns		1,7,8
2	TrC,TfC	Clock Input Rise &	3.5V		15		25	ns		1,7,8
		Fall Times	5.5V		15		25	ns		1,7,8
3	TwC	Input Clock Width	3.5V	31		31		ns		1,7,8
			5.5V	31		31		ns		1,7,8
4	TwTinL	Timer Input Low	3.5V	70		70		ns		1,7,8
		Width	5.5V	70		70		ns		1,7,8
5	TwTinH	Timer Input High	3.5V	5TpC		5TpC				1,7,8
		Width	5.5V	5TpC		5TpC				1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				1,7,8
			5.5V	8TpC		8TpC				1,7,8
7	TrTin, TfTin	Timer Input Rise	3.5V		100		100	ns		1,7,8
		& Fall Timer	5.5V		100		100	ns		1,7,8
8A	TwIL	Int. Request Low	3.5V	70		70		ns		1,2,7,8
		Time	5.5V	70		70		ns		1,2,7,8
8B	TwIL	Int. Request Low	3.5V	5TpC		5TpC				1,3,7,8
		Time	5.5V	5TpC		5TpC				1,3,7,8
9	TwIH	Int. Request Input	3.5V	5TpC		5TpC				1,2,7,8
		High Time	5.5V	5TpC		5TpC				1,2,7,8
10	Twsm	STOP Mode	3.5V	12		12		ns		4,8
		Recovery Width	5.5V	12		12		ns		4,8
		Spec								
11	Tost	Oscillator Startup	3.5V		5TpC		5TpC			4,8
		Time	5.5V		5TpC		5TpC			4,8
12	Twdt	Watch-Dog Timer	3.5V	10		10		ms	D0 = 0	5,11
		Delay Time Before	5.5V	5		5		ms	D1 = 0	5,11
		Timeout	3.5V	20		20		ms	D0 = 1	5,11
			5.5V	10		10		ms	D1 = 0	5,11
			3.5V	40		40		ms	D0 = 0	5,11
			5.5V	20		20		ms	D1 = 1	5,11
			3.5V	160		160		ms	D0 = 1	5,11
			5.5V	80		80		ms	D1 = 1	5,11

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Reg. WDTMR
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.
10. Standard Mode (not Low EMI output ports)
11. Using internal RC

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com