Dual 5V Synchronous Buck PWM DC-DC and Linear Power Controller

General Description

The RT9212 is a 3-in-one power controller delivers high efficiency and tight regulation from two voltage regulating synchronous buck PWM DC-DC and one linear power controllers.

The RT9212 can control two independent output voltages adjustment in range of 0.8V to 4.0V with 180 degrees channel to channel phase operation to reduce input ripple. In dual power supply application the RT9212 monitors the output voltage of both Channel 1 and Channel 2. An independent PGOOD (power good) signal is asserted for each channel after the soft-start sequence has completed, and the output voltage is within ±15% of the set point. The linear controller drives an external transistor to provide an adjustable output voltage.

Built-in over-voltage protection prevents the output from going above 137.5% of the set point by holding the lower MOSFET on and the upper MOSFET off. Adjustable over-current protection (OCP) monitors the voltage drop across the $R_{DS(ON)}$ of the upper MOSFET for each synchronous buck PWM DC-DC controller individually.

Ordering Information

RT9212□□

- Package Type
  - C : TSSOP-24
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

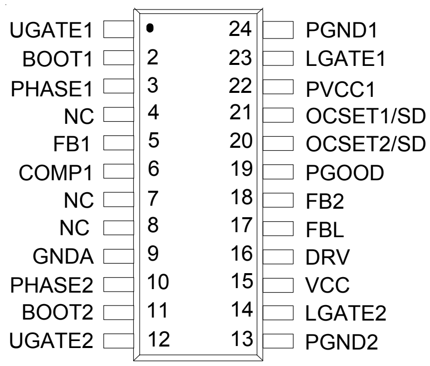
- **Operating with Single 5V Supply Voltage**
- **Drives All Low Cost N-MOSFETs**
- **Voltage Mode PWM Control**
- **300kHz Fixed Frequency Oscillator**
- **Fast Transient Response :**
  Full 0% to 100% Duty Ratio
- **Internal Soft-Start**
- **Adaptive Non-Overlapping Gate Driver**
- **Over-Current Fault Monitor on V_{CC}, No Current Sense Resistor Required**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Graph Card
- Motherboard, Desktop Servers
- IA Equipments
- Telecomm Equipments
- High Power DC-DC Regulators

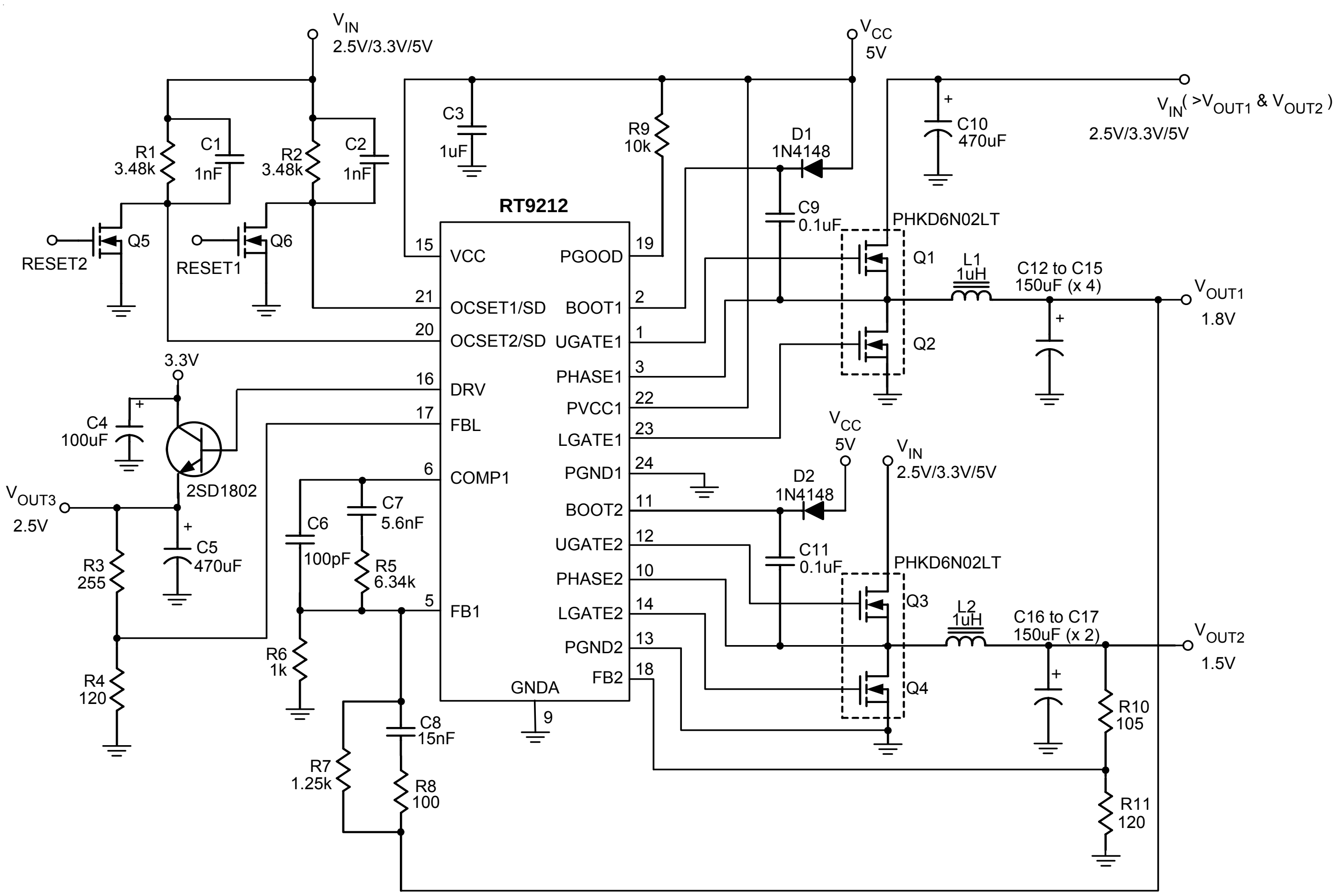
Pin Configurations

(TOP VIEW)



TSSOP-24

Typical Application Circuit



Functional Pin Description

UGATE1 (Pin 1)

Channel 1 upper gate driver output. Connect to gate of the high-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

BOOT1 (Pin 2)

Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BOOT1 pin and the PHASE1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

PHASE1 (Pin 3)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. PHASE1 is used to monitor the Voltage drop across the upper MOSFET of the channel 1 regulator for over-current protection.

NC (Pin 4, 7, 8)

No connection. Don' t connect any component to this pin.

FB1 (Pin 5)

Channel 1 feedback voltage. This pin is the inverting input of the error amplifier. FB1 senses the channel 1 through an external resistor divider network.

COMP1 (Pin 6)

Channel 1 external compensation. This pin internally connects to the output of the error amplifier and input of the PWM comparator. Use a RC + C network at this pin to compensate the feedback loop to provide optimum transient response.

GNDA (Pin 9)

Signal ground for the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to ground plane with the lowest impedance.

PHASE2 (Pin 10)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. PHASE2 is used to monitor the Voltage drop across the upper MOSFET of the channel 2 regulator for over-current protection.

BOOT2 (Pin 11)

Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BOOT2 pin and the PHASE2 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

UGATE2 (Pin 12)

Channel 2 upper gate driver output. Connect to gate of the high-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

PGND2 (Pin 13)

Return pin for high currents flowing in low-side power N-MOSFET. Ties the pin directly to the low-side MOSFET source and ground plane with the lowest impedance.

LGATE2 (Pin 14)

Channel 2 lower gate drive output. Connect to gate of the low-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

VCC (Pin 15)

Connect this pin to a well-decoupled 5V bias supply. It is also the positive supply for the lower gate driver, LGATE2.

DRV (Pin 16)

Connect this pin to the base of an external transistor. This pin provides the drive for the linear regulator's pass transistor.

FBL (Pin 17)

Linear regulator feedback voltage. This pin is the inverting input of the error amplifier and protection monitor. Connect this pin to the external resistor divider network of the linear regulator.

FB2 (Pin 18)

Channel 2 feedback voltage. This pin is the inverting input of the error amplifier. FB2 senses the channel 2 through an external resistor divider network.

PGOOD (Pin 19)

PGOOD is an open-drain output used to indicate that both the channel 1 and channel 2 regulators are within normal operating voltage ranges.

OCSET2/SD (Pin 20), OCSET1/SD (Pin 21)

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET of the supply voltage sets the over-current trip point. R_{OCSET}, an internal 40µA current source , and the upper MOSFET on-resistance, ($R_{DS(ON)}$), set the converter over-current trip point (I_{OCSET}) according to the following equation:

$$I_{OCSET} = \frac{40uA \times R_{OCSET}}{R_{DS(ON)} \text{ of the upper MOSFET}}$$

An over-current trip cycles the soft-start function. Pulling the pin to ground resets the device and all external MOSFETs are turned off allowing the two output voltage power rails to float.

PVCC1 (Pin 22)

Connect this pin to a well-decoupled 5V supply. It is also the positive supply for the lower gate driver, LGATE1.

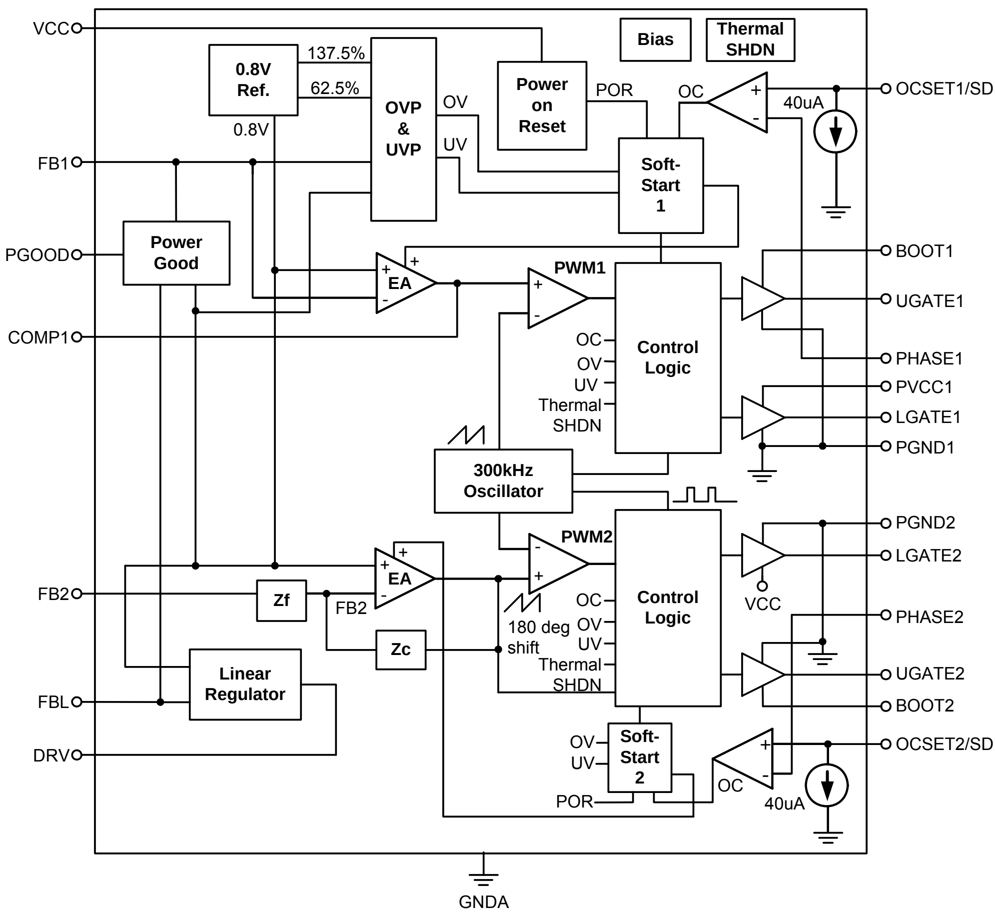
LGATE1 (Pin 23)

Channel 1 power gate drive output. Connect to gate of the low-side power N-Channel MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

PGND1 (Pin 24)

Return pin for high currents flowing in low-side power N-MOSFET. Ties the pin directly to the low-side MOSFET source and ground plane with the lowest impedance.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 7V
- BOOT, V_{BOOT} - V_{PHASE} ---------- 7V
- Input, Output or I/O Voltage ---------- GND-0.3V to 7V
- Package Thermal Resistance
  TSSOP-24, θ_{JA} ---------- 100°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- − 65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 5V ± 5 %
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current						
Nominal Supply Current	I_{CC}	OCSET1/SD, OCSET2/SD = V_{CC}; UGATE1 & 2, LGATE1 & 2 Open	--	5	--	mA
Shutdown Supply	I_{CCSD}	(OCSET1/SD, OCSET2/SD) = 0V	--	3	--	mA
Power-On Reset						
POR Threshold	V_{CCRTH}	$V_{OCSET1/SD,\ OCSET2/SD}$ = 4.5V V_{CC} Rising	3.7	4.1	4.5	V
Hysteresis	V_{CCHYS}	$V_{OCSET1/SD,\ OCSET2/SD}$ = 4.5V	--	0.5	--	V
Reference						
Error Amp Reference Voltage Tolerance	ΔV_{EAR}		--	--	2	%
Error Amp Reference	V_{REF}	V_{CC} = 5V	0.784	0.8	0.816	V
Oscillator						
Free Running Frequency	f_{OSC}	V_{CC} = 5V	275	300	325	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.9	--	V_{P-P}
V1 Error Amplifier (External Compensation)						
DC Gain			--	90	--	dB
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR	COMP = 10pF	--	6	--	V/μs

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V2 Error Amplifier (Internal Compensation)							
DC Gain				--	35	--	dB
Linear Regulator							
DRV Driver Source		I_{DS}		--	100	--	mA
PWM Controller Gate Drivers							
Upper Gate Source (UGATE1 and 2)		R_{UGATE}	BOOT = 10V BOOT – V_{UGATE} = 1V	--	7	--	Ω
Upper Gate Sink (UGATE1 and 2)		R_{UGATE}	V_{UGATE} = 1V	--	5	--	Ω
Lower Gate Source (LGATE1 and 2)		R_{LGATE}	V_{CC} – V_{LGATE} = 1V	--	4	--	Ω
Lower Gate Sink (LGATE1 and 2)		R_{LGATE}	V_{LGATE} = 1V	--	2	--	Ω
Upper Gate Rising Time (UGATE1 and 2)		T_{R_UGATE}	C_{Load} = 3.3nF	--	70	--	ns
Upper Gate Falling Time (UGATE1 and 2)		T_{F_UGATE}	C_{Load} = 3.3nF	--	50	--	ns
Lower Gate Rising Time (LGATE1 and 2)		T_{R_LGATE}	C_{Load} = 3.3nF	--	50	--	ns
Lower Gate Falling Time (LGATE1 and 2)		T_{F_LGATE}	C_{Load} = 3.3nF	--	32	--	ns
Dead Time		T_{DT}		--	--	100	ns
Protection							
FB1 & FB2 Over-Voltage Trip		Δ_{FBOVT}	FB1 & FB2 Rising	125	137.5	--	%
FB1 & FB2 Under-Voltage Trip		Δ_{FBUVT}	FB1 & FB2 Falling	--	62.5	75	%
OCSET1 & OCSET2 Current Source		I_{OCSET}	$V_{OCSET1/SD,\ OCSET2/SD}$ = 4.5V	34	40	46	μA
OCP Blocking Time				--	320	540	ns
OCSET/SD	Logic-Low Voltage	V_{IL}	Shutdown	--	--	0.2	V
	Logic-High Voltage	V_{IH}	Enable	2.0	--	--	
Soft-Start Interval		T_{SS}		--	4	--	ms
Power Good							
Upper Threshold		V_{PG+}	FB1 & FB2 Rising	110	115	120	%
Lower Threshold		V_{PG-}	FB1 & FB2 Rising	80	85	90	%

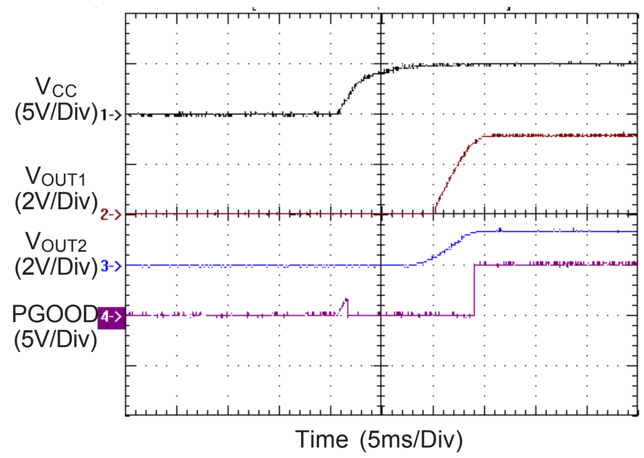
Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

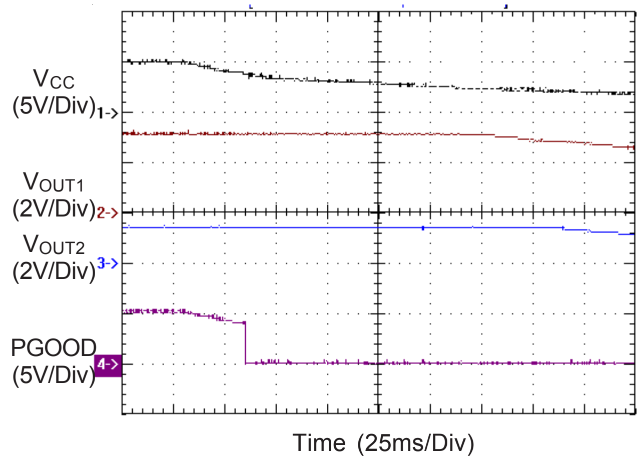
Note 3. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

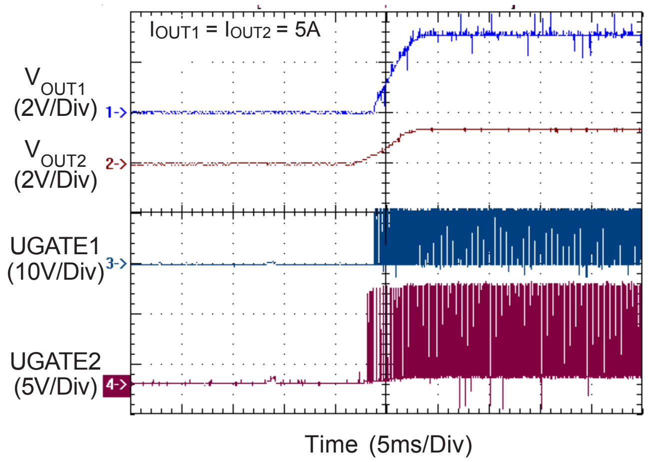
Power Good Rising



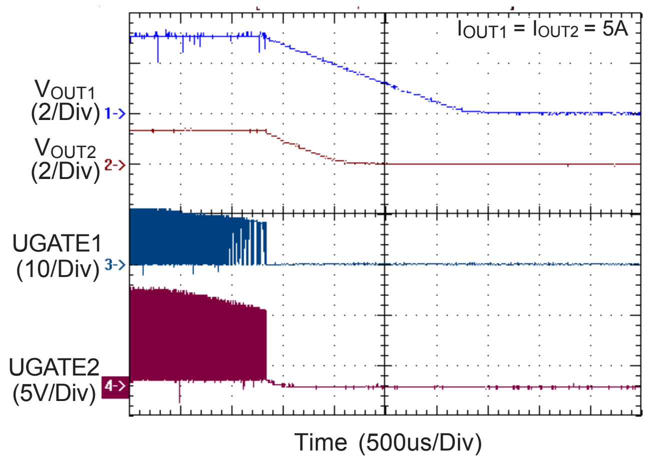
Power Good Falling



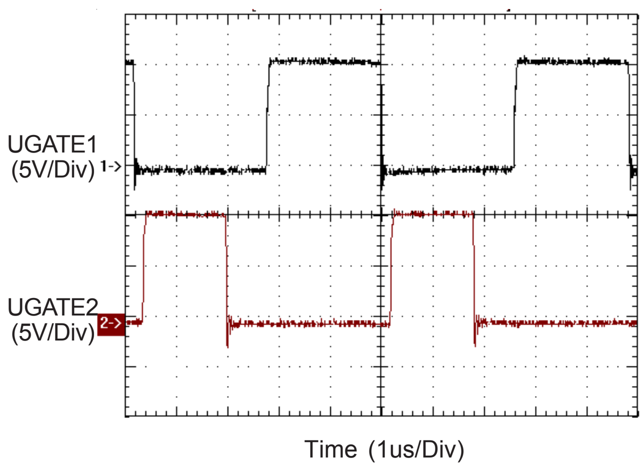
Power On



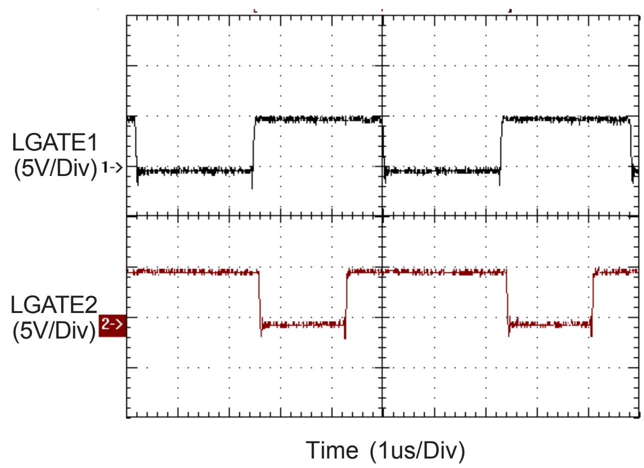
Power Off



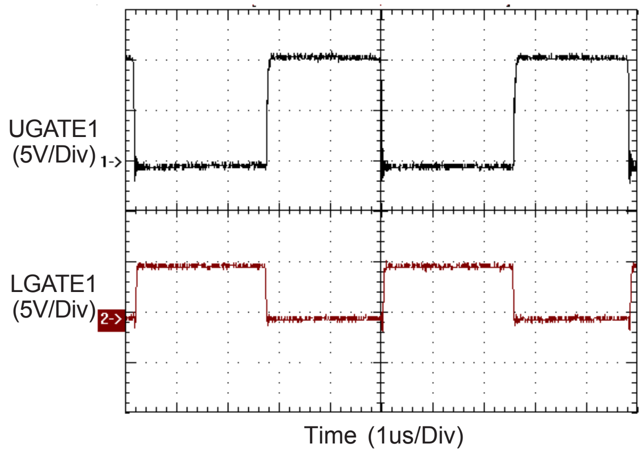
UGATE Phase Shift



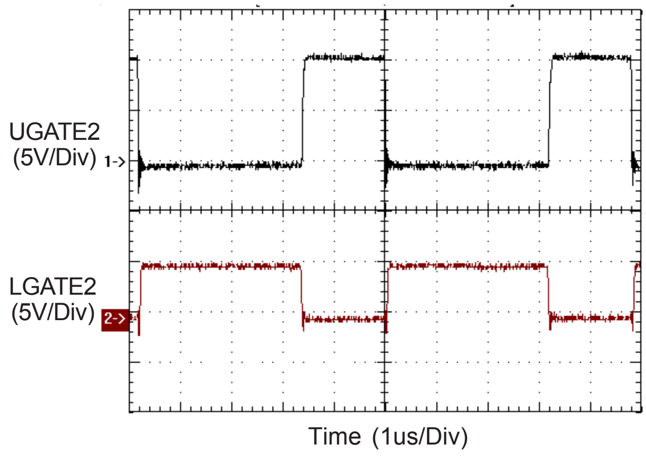
LGATE Phase Shift



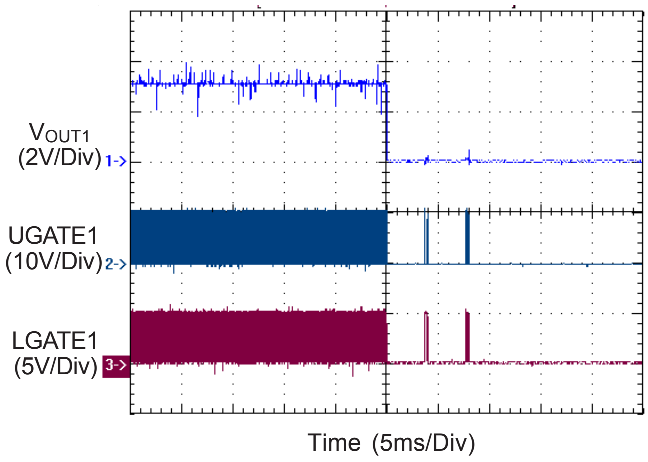
Bootstrap



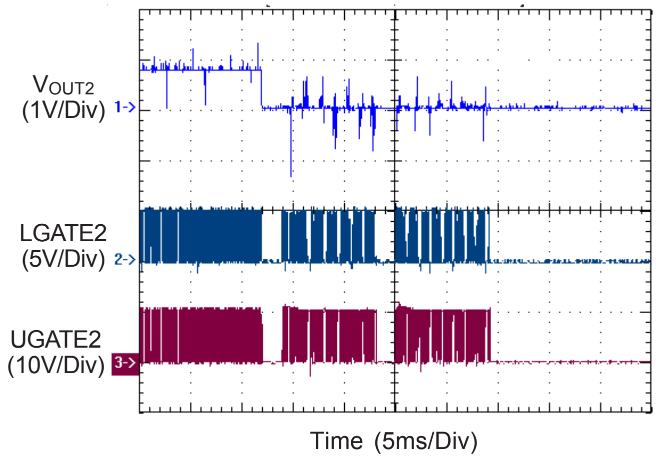
Bootstrap



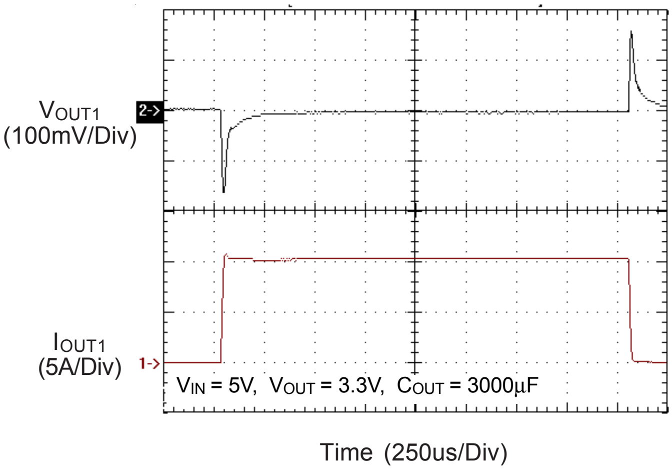
V_{OUT1} Short



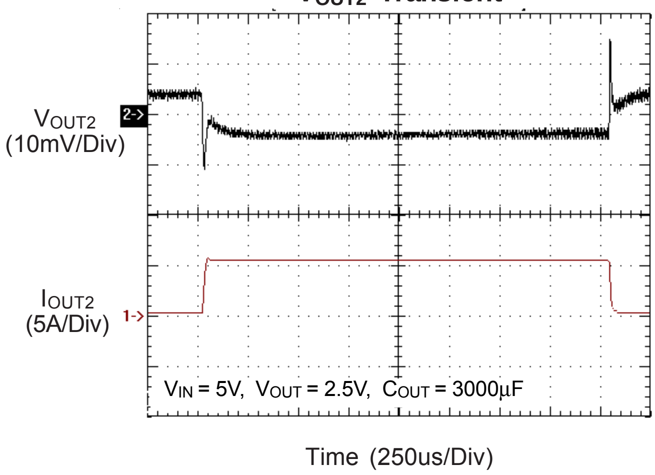
V_{OUT2} Short



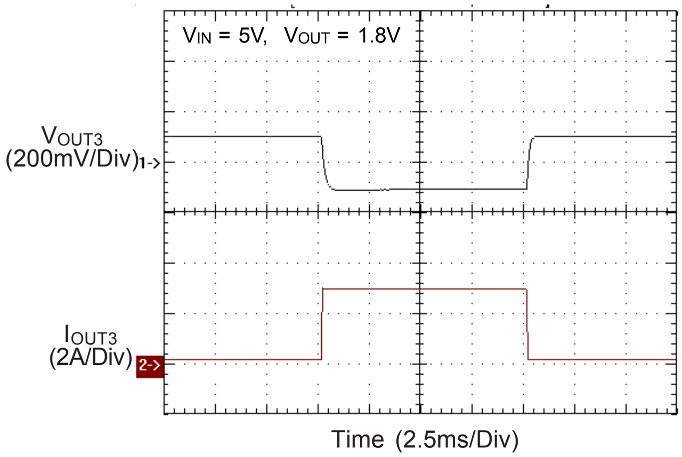
V_{OUT1} Transient



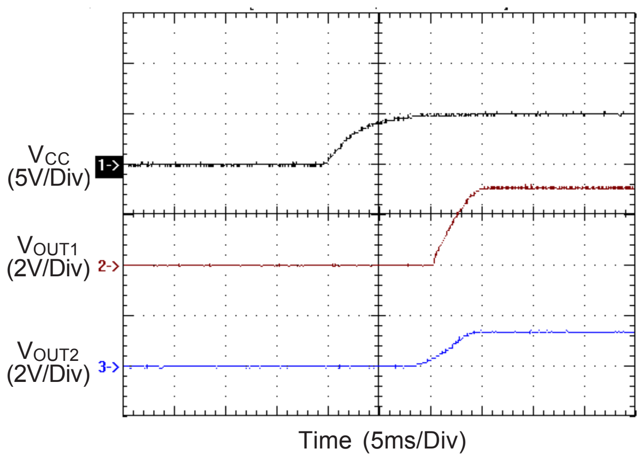
V_{OUT2} Transient



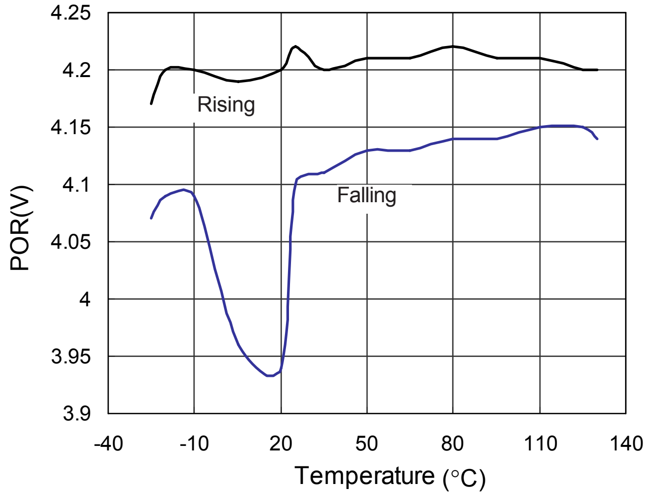
V_{OUT3} Transient



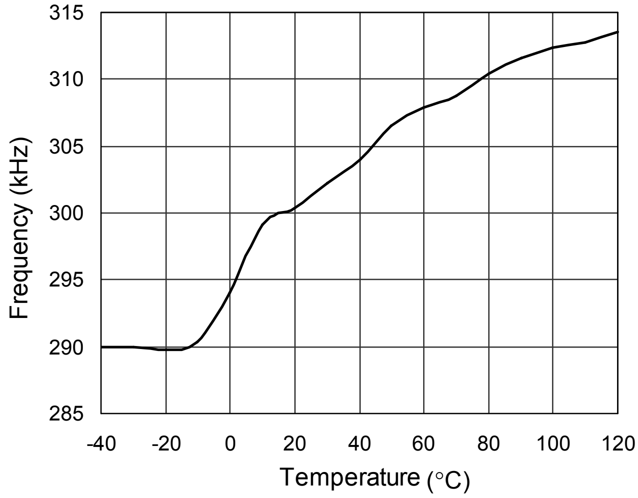
POR (Start Up)



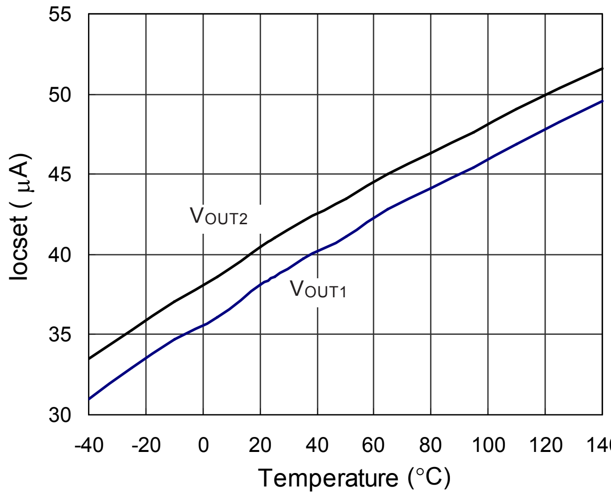
POR (Rising/Falling) vs. Temperature



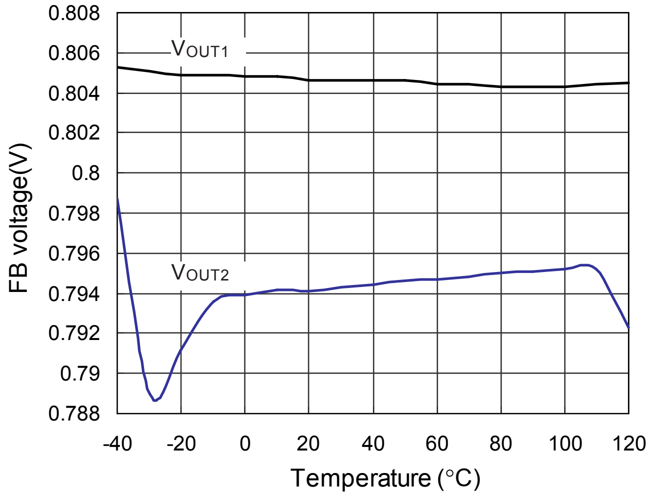
Frequency vs. Temperature



Iocset & Temperature



Reference vs. Temperature



Applications Information

Inductor

The inductor is required to supply constant current to the output load. The inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient.

A larger value of inductance reduces ripple current and voltage. However, the larger value of inductance has a larger physical size, lower output capacitor and slower transient response time.

A good rule for determining the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum output current. The inductance value can be calculated by the following equation :

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_S \times \Delta I_{OUT}}$$

Where

V_{IN} is the input voltage,

V_{OUT} is the output voltage,

F_S is the switching frequency,

ΔI_{OUT} is the peak-to-peak inductor ripple current.

The inductance value determines the converter's ripple current and the ripple voltage. The ripple current is calculated by the following equations :

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_S \times L}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values raise the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the RT9212 will provide 0% to 100% duty cycle in response to a load transient.

The response time is the time required to slew the inductor current from an initial current value to the transient current level. The inductor limit input current slew rate during the load transient. Minimizing the transient response time can minimize the output capacitance required. The response time is different for application of load and removal of load to a transient. The following equations give the approximate response time for application and removal of a transient load :

$$T_{Rise} = \frac{L \times \Delta I_{OUT}}{V_{IN} - V_{OUT}} \quad , \quad T_{Fall} = \frac{L \times \Delta I_{OUT}}{V_{OUT}}$$

Where

T_{Rise} is the response time to the application of load,

T_{Fall} is the response time to the removal of load,

ΔI_{OUT} is the transient load current step.

Input Capacitor

The input capacitor is required to supply the AC current to the Buck converter while maintaining the DC input voltage. The capacitor should be chosen to provide acceptable ripple on the input supply lines. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current. Place the small ceramic capacitors close to the MOSFETs and between the drain of Q1/Q3 and the source of Q2/Q4.

The key specifications for input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and voltage rating of 1.5 times is a conservative guideline. The RMS current rating for the input capacitor of a buck regulator should be greater than approximately 0.5 the DC load current.

Output Capacitor

The output capacitor is required to maintain the DC output voltage and supply the load transient current. The capacitor must be selected and placed carefully to yield optimal results and should be chosen to provide acceptable ripple on the output voltage.

The key specification for output capacitor is its ESR. Low ESR capacitors are preferred to keep the output voltage ripple low. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. For transient response, a combination of low value, high frequency and bulk capacitors placed close to the load will be required. High frequency decoupling capacitors should be placed as close to the power pins of the load as possible. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

The capacitor value must be high enough to absorb the inductor's ripple current. The output ripple is calculated as :

$$\Delta V_{OUT} = \Delta I_{OUT} \times ESR$$

Another concern is high ESR induced output voltage ripple may trigger UV or OV protections will cause IC shutdown.

MOSFET

The MOSFET should be selected to meet power transfer requirements is based on maximum drain-source voltage (V_{DS}), gate-source drive voltage (V_{GS}), maximum output current, minimum on-resistance ($R_{DS(ON)}$) and thermal management.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The losses can be divided into conduction and switching losses.

Conduction losses are related to the on resistance of MOSFET, and increase with the load current. Switching losses occur on each ON/OFF transition. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs.

For the Buck converter the average inductor current is equal to the output load current. The conduction loss is defined as :

P_{CD} (high side switch) = $I_O^2 * R_{DS(ON)} * D$

P_{CD} (low side switch) = $I_O^2 * R_{DS(ON)} * (1-D)$

The switching loss is more difficult to calculate. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turn-off delays and rise and fall times. With a linear approximation, the switching loss can be expressed as :

$P_{SW} = 0.5 * V_{DS(OFF)} * I_O * (T_{Rise} + T_{Fall}) * F$

Where

$V_{DS(OFF)}$ is drain to source voltage at off time,

T_{Rise} is rise time,

T_{Fall} is fall time,

F is switching frequency.

The total power dissipation in the switching MOSFET can be calculate as :

$P_{High\ Side\ Switch}$ =

$I_O^2 * R_{DS(ON)} * D + 0.5 * V_{DS(OFF)} * I_O * (T_{Rise} + T_{Fall}) * F$

$P_{Low\ Side\ Switch} = I_O^2 * R_{DS(ON)} * (1-D)$

For input voltages of 3.3V and 5V, conduction losses often dominate switching losses. Therefore, lowering the $R_{DS(ON)}$ of the MOSFETs always improves efficiency.

Feedback Compensation

The RT9212 is a voltage mode controller; the control loop is a single voltage feedback path including an error amplifier and PWM comparator as Figure 1 shows. In order to achieve fast transient response and accurate output regulation, a adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (greater than 45 degrees) and the highest 0dB crossing frequency. And to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

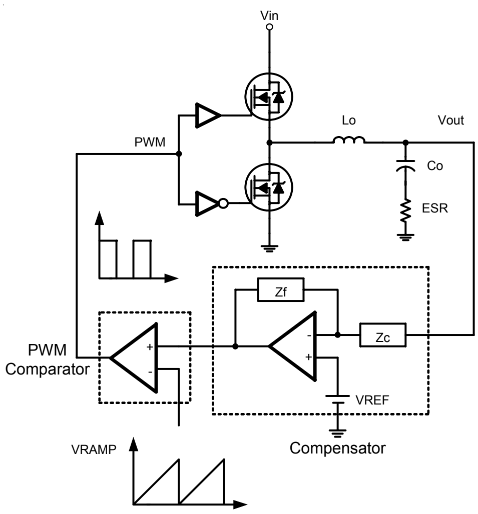


Figure 1

Modulator Frequency Equations

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This transfer function is dominated by a DC gain and the output filter (L_O and C_O), with a double pole frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage V_{RAMP}.

The first step is to calculate the complex conjugate poles contributed by the LC output filter.

The output LC filter introduces a double pole,–40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The Resonant frequency of the LC filter expressed as follows :

$$F_{P(LC)} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}}$$

The next step of compensation design is to calculate the ESR zero. The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor expressed as follows :

$$F_{Z(ESR)} = \frac{1}{2\pi \times C_O \times ESR}$$

Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_F as Figure 2 shows.

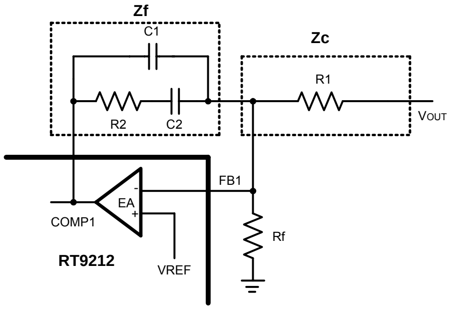


Figure 2

$$F_{P1} = 0$$

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_2}$$

$$F_{P1} = \frac{1}{2\pi \times R_2 (C_1 // C_2)}$$

Figure 3 shows the DC-DC converter's gain vs. frequency. The compensation gain uses external impedance networks Z_C and Z_F to provide a stable, high bandwidth loop.

High crossover frequency is desirable for fast transient response, but often jeopardize the system stability. In order to cancel one of the LC filter poles, place the zero before the LC filter resonant frequency. In the experience, place the zero at 75% LC filter resonant frequency.Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency.

The second pole be place at half the switching frequency.

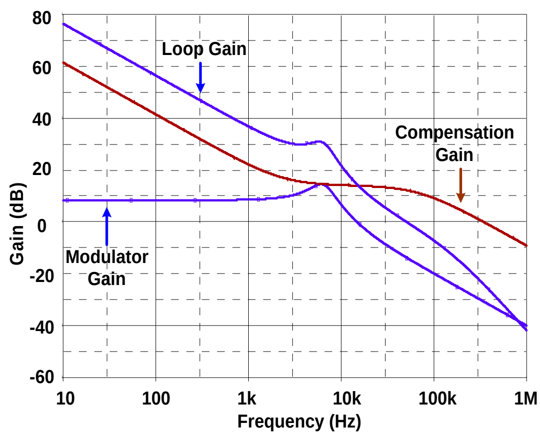


Figure 3

Reference Voltage

Because one of the RT9212 regulators uses a low 35dB gain error amplifier, shown in Figure 4. The voltage regulation is dependent on V_{IN} & V_{OUT} setting.The FB reference voltage of 0.8V is trimmed at V_{IN} = 5V & V_{OUT} = 2.5V condition. In a fixed V_{IN} = 5V application, the FB reference voltage vs. V_{OUT} voltage can be calculated as Figure 5.

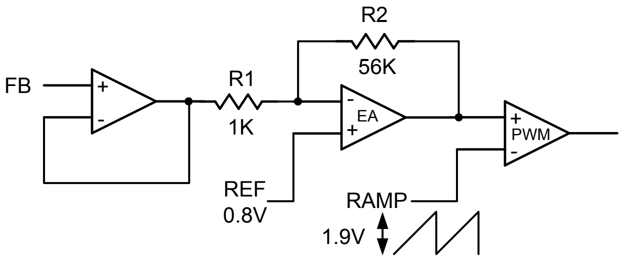


Figure 4

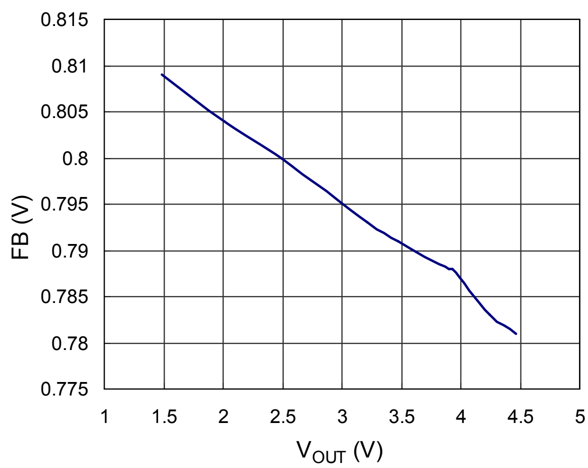


Figure 5

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

1. Even though double-sided PCB is usually sufficient for a good layout, four-layer PCB is the optimum approach to reducing the noise. Use the two internal layers as the power and GND planes, the top layer for power connections with wide, copper filled areas, and the bottom layer for the noise sensitive traces.

2. There are two sets of critical components in a DC-DC converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. The others are the small signal components that connect to sensitive nodes or supply critical bypass current and signal coupling. Make all critical component ground connections with vias to GND plane.

3. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low. Place the output capacitors as close to the load as possible.

4. The inductor, output capacitor and the MOSFET should be as close to each other as possible. This helps to reduce the EMI radiated.

5. Place the switching MOSFET as close to the input capacitors as possible. The MOSFET gate traces to the IC must be as short, straight, and wide as possible. Use copper filled polygons on the top and bottom layers for the PHASE nodes.

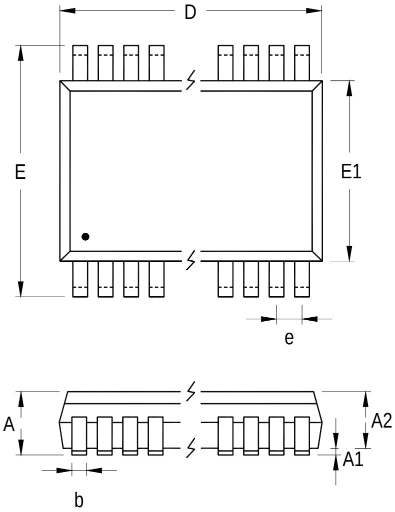
6. Place the C_{BOOT} as close as possible to the BOOT and PHASE pins.

7. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. Connect to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.

8. Minimize the leakage current paths on the OCSET/SD pin and locate the resistor as close to the OCSET/SD pin as possible because the internal current source is only 40µA.

9. In multilayer PCB, use one layer as ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.850	1.200	0.033	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	7.700	7.900	0.303	0.311
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030

24-Lead TSSOP Plastic Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
8F, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com