S12HFAMPP
Rev. 11.1, 17-Aug-2004

16-bit Microcontroller HCS12H Family

Introduction

Designed for automotive instrumentation applications, all members of the MCS12H-Family of microcontroller units (MCU) are composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 256K bytes of Flash EEPROM or ROM, up to 12K bytes of RAM, up to 4K bytes of EEPROM on Flash parts, one or two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 16-channel, 10-bit analog-to-digital converter (ADC), up to six-channel pulse width modulator (PWM), and up to two CAN 2.0 A, B software compatible modules. In addition, they feature a 32x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (MC) consisting of up to 24 high current outputs suited to drive up to six stepper motors, and on selected devices, up to four stepper stall detectors (SSD) to simulataneously calibrate the pointer reset position of each motor. The MCS12H-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 14 I/O ports are available with Key-Wake-Up capability from STOP or WAIT mode.

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Feature Detail

NOTE

*Not all features listed here are available in all configurations. For a quick overview refer to **Table 1**.*

- **HCS12 Core**
  - HCS12 16-bit CPU
    - Upward compatible with M68HC11 instruction set
    - Interrupt stacking and programmer's model identical to M68HC11
    - Instruction queue
    - Enhanced indexed addressing
  - HCS12 MEBI (Multiplexed Expanded Bus Interface)
  - HCS12 MMC (Module Mapping Control)
  - HCS12 INT (Interrupt Control)
  - HCS12 BKP (On-chip Breakpoints)
  - HCS12 BDM (Single-wire Background Debug™ Mode)
- **Memory options**
  - 32K, 64K, 128K, 256K byte Flash EEPROM or 64K, 128K, 192K and 256K byte ROM
  - 2K, 4K, 6K, 8K, 12K byte RAM
  - 2K, 4K byte EEPROM on Flash versions only
- **8-bit and 4-bit ports with Interrupt capability**
  - Digital filtering
  - Programmable rising or falling edge trigger
- **Clock Reset Generator (CRG)**
  - Low current Colpitts or Pierce oscillator (0.5 to 16Mhz reference clock)
  - Phase-locked loop clock frequency multiplier
  - Windowed COP watchdog and Clock Monitor resets
  - Real Time Interrupt
- **Up to 16-channels Analog-to-Digital Converter (ADC)**
  - 10-bit resolution
  - External conversion trigger capability
- **Up to two 1M bit per second, CAN 2.0 A, B software compatible modules (MSCAN12)**
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- **Timer (TIM)**
  - 16-bit main counter with 7-bit prescaler
  - Eight programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- **Up to six Pulse Width Modulator (PWM) channels**

  - Programmable period and duty cycle for each channel
  - Pairs of 8-bit channels can be concatenated as one 16-bit channel
  - Center-aligned or left-aligned outputs
  - Wide range of programmable clock frequencies
  - Fast emergency shutdown input
- **Serial interfaces**
  - Up to two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)
  - Inter-IC Bus Interface (IIC)
- **Liquid Crystal Display (LCD) driver**
  - Up to 32 frontplanes and 4 backplanes
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Programmable frame clock generator and bias voltage level
- **16 or 24 high current drivers suited for PWM motor control**
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Support for sine and cosine drive
  - 11-bit resolution with selectable dithering function
  - Left, right or center aligned outputs
  - Slew rate control
- **Up to four Stepper Stall Detectors (SSD) - available on selected devices**
  - Flexible full step and polarity set up to return the pointer to its reset position in clockwise or counter clockwise direction.
  - Integrator/Sigma Delta converter circuit to measure the induced voltage by the back EMF of unpowered coil during full step (only one of the two motor coils is powered) operation.
  - 16-Bit Down Counter to monitor blanking and integration time to support stepper motors with different gear ratios.
  - 16-Bit accumulator register to read integration value, compare to a threshold at the end of integration time, and decide if the motor is stalled under this value or moving above this value.
- **Operating Frequency**
  - 32Mhz equivalent to 16Mhz Bus Speed (Only 9S12H256)
  - 50Mhz equivalent to 25Mhz Bus Speed (Except 9S12H256)
- **80-Pin, 112-Pin or 144-Pin QFP package**
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs

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Table 1 List of MCS12H-Family members

Flash	ROM	RAM	EEPROM	Device	Package	CAN	SCI	SPI	IIC	A/D	PWM	TIM	LCD	Motor	SSD	KWU	I/O
256K	0	12K	4K	9S12H256	144 LQFP	2	2	1	1	16	6	8	32x4	24/6	0	12	117
256K	0	12K	4K	9S12H256(1)	112 LQFP	2	1	1	0	8	2	8	28x4	24/6	0	0	85
128K	0	6K	2K	9S12H128(1)	112 LQFP	2	1	1	0	8	2	8	28x4	24/6	0	0	85
256K	0	12K	2K	9S12HZ256	112 LQFP	2	2	1	1	16	6	8	32x4	16/4	4	8	85
128K	0	6K	2K	9S12HZ128	112 LQFP	2	2	1	1	16	6	8	32x4	16/4	4	8	85
64K	0	4K	1K	9S12HZ64	112 LQFP	1	1	1	0	8	4	8	24x4	16/4	2	8	69
64K	0	4K	1K	9S12HN64	112 LQFP	0	1	1	0	8	4	8	24x4	16/4	2	8	69
64K	0	4K	1K	9S12HZ64	80 QFP	1	1	0	0	7	4	4	20x4	16/4	2	7	60
64K	0	4K	1K	9S12HN64	80 QFP	0	1	0	0	7	4	4	20x4	16/4	2	7	60
0	256K	12K	0	3S12HZ256	112 LQFP	2	2	1	1	16	6	8	32x4	16/4	4	8	85
0	192K	8K	0	3S12HZ192	112 LQFP	2	2	1	1	16	6	8	32x4	16/4	4	8	85
0	128K	6K	0	3S12HZ128	112 LQFP	1	2	1	1	8	6	8	32x4	16/4	4	8	85
0	128K	6K	0	3S12HN128	112 LQFP	0	2	1	1	8	6	8	32x4	16/4	4	8	85
0	64K	4K	0	3S12HZ64	112 LQFP	1	1	1	0	8	4	8	24x4	16/4	2	8	69
0	64K	4K	0	3S12HN64	112 LQFP	0	1	1	0	8	4	8	24x4	16/4	2	8	69
0	32K	2K	0	3S12HZ32	80 QFP	1	1	0	0	7	4	4	20x4	16/4	2	7	60
0	32K	2K	0	3S12HN32	80 QFP	0	1	0	0	7	4	4	20x4	16/4	2	7	60

NOTES:
1. Not recommended for new designs.

- **Flash emulation of ROM versions**
  - ROM versions 3S12HZ256, 3S12HZ192, 3S12HZ128 and 3S12HN128 should use the 9S12HZ256 for Flash emulation.
  - ROM versions 3S12HZ64, 3S12HN64, 3S12HZ32 and 3S12HN32 should use the 9S12HZ64 for Flash emulation.
- **Pin out explanations:**
  - A/D is the number of A/D channels.
  - PWM is the number of TIM channels.
  - LCD denotes the number of front planes times the number of back planes.
  - Motor denotes the number of high current drive pins / number of stepper motors which can be driven
  - SSD denotes whether this device features a Stepper Stall Detection Circuit
  - Versions with one SCI will use SCI0
  - Versions with one CAN will use CAN0
  - I/O is the sum of ports capable to act as digital input or output.
    144 Pin Package:
    Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 5, L = 8, M = 6, P = 6, S = 8, T = 8, U = 8, V = 8, W = 8, PAD = 16 input only.
    14 inputs provide Interrupt capability (H = 8, J = 4, IRQ, XIRQ).
    112 Pin Package for H Versions:
    Port A = 8, B = 8, E = 6 + 2 input only, K = 5, L = 4, M = 4, P = 2, S = 6, T = 8, U = 8, V = 8, W = 8, PAD = 8 input only.

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2 inputs provide Interrupt capability (IRQ, XIRQ).
112 Pin Package for 9HZ256, 9HZ128, 3HZ128 and 3HN128 Versions:
Port A = 8, B = 8, E = 6 + 2 input only, K = 5, L = 8, M = 5, P = 6, S = 6, T = 8, U = 8, V = 8, PAD = 8.
10 inputs provide Interrupt capability (AD = 8, IRQ, XIRQ).
112 Pin Package for 9HZ64, 9HN64, 3HZ64 and 3HN64 Versions:
Port A = 8, B = 4, E = 4 + 1 input only, K = 5, L = 4, M = 2, P = 4, S = 5, T = 8, U = 8, V = 8, PAD = 8.
9 inputs provide Interrupt capability (AD = 8, XIRQ).
80 Pin Package for 9HZ64, 9HN64, 3HZ32 and 3HN32 Versions:
Port A = 8, B = 4, E = 4 + 1 input only, K = 5, M = 2, P = 4, S = 5, T = 4, U = 8, V = 8, PAD = 7.
8 inputs provide Interrupt capability (AD = 7, XIRQ).

- Compatibility Considerations
  - Pins associated with Motors 0 and 5 should be left unconnected to ensure compatibility with versions featuring 4 Motors.

Block Diagram

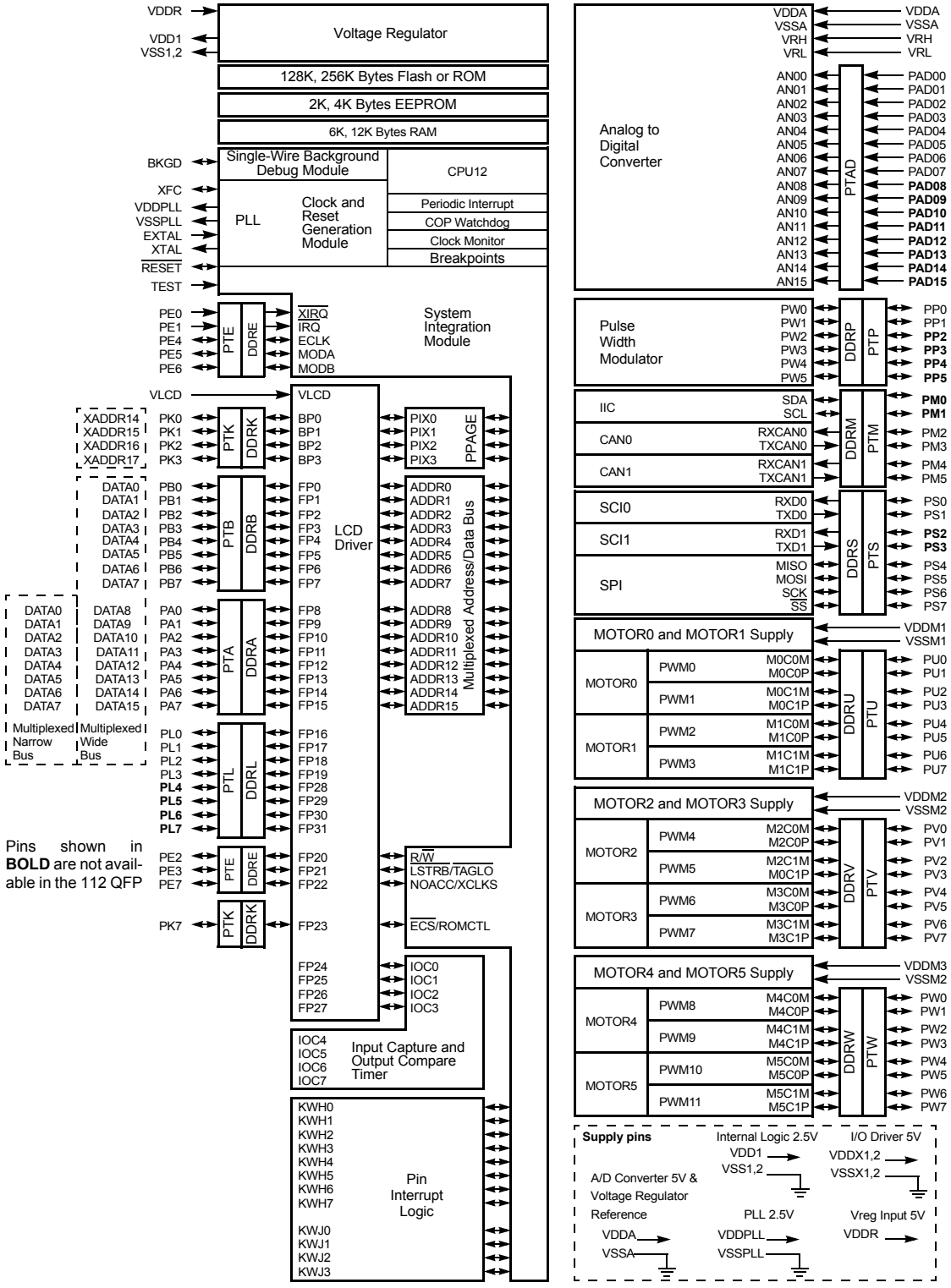

Figure 1. MC9S12H-Family Block Diagram

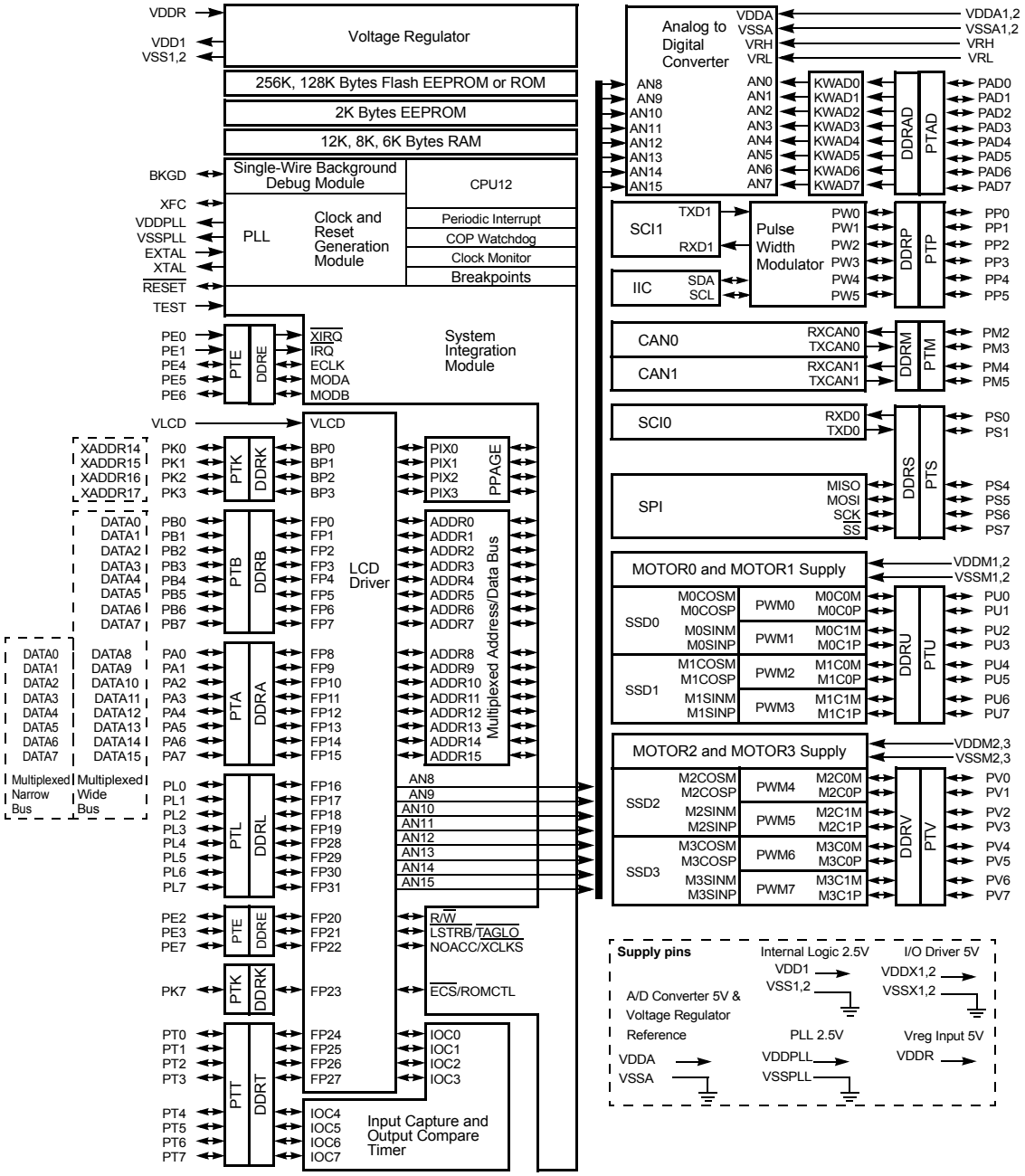

Figure 2. MC9S12H-Family "Z" Version Block Diagram

Pin Assignments

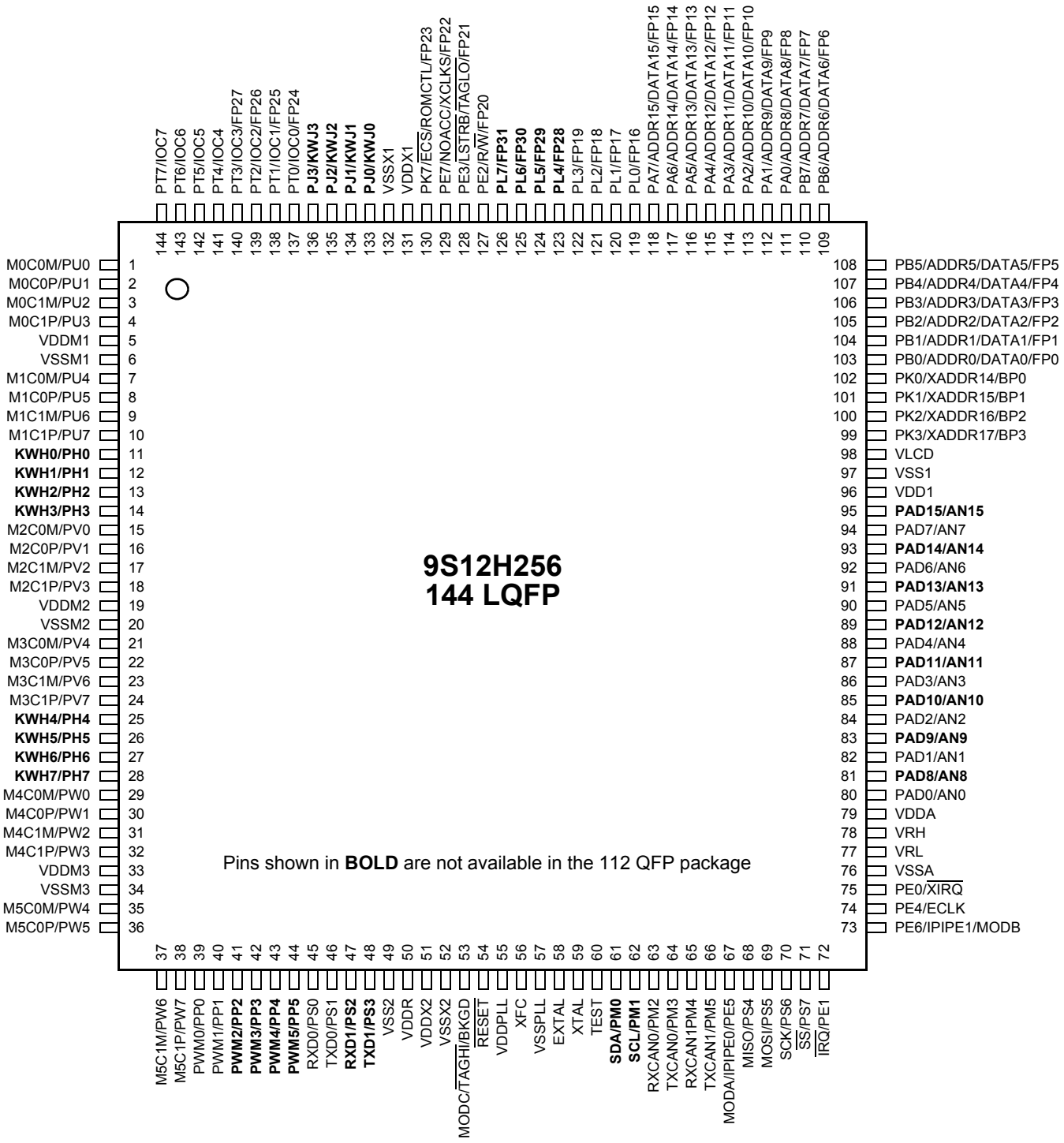

Figure 1. 144-Pin Package Signal Assignments for 9S12H256

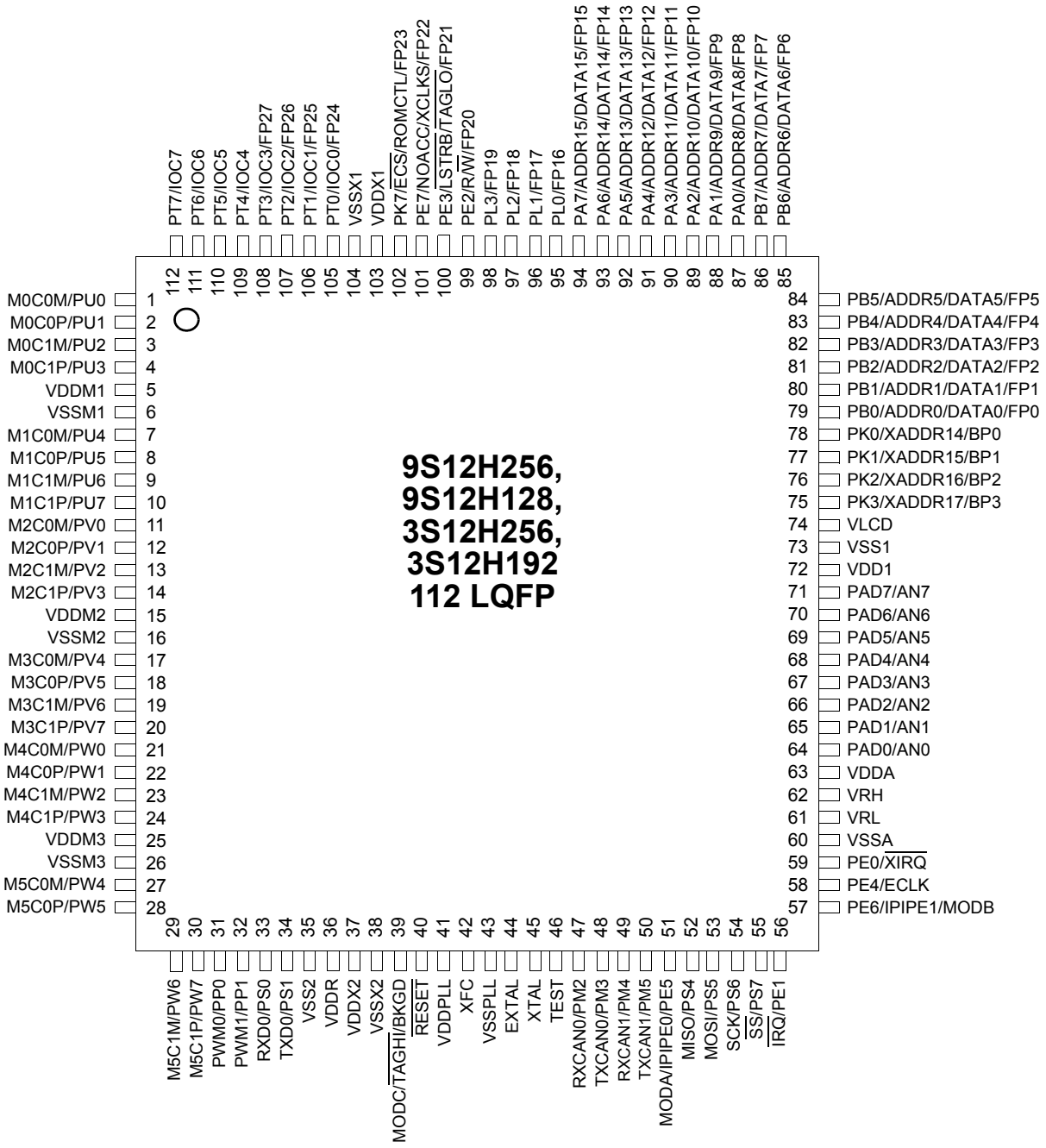

Figure 2. 112-Pin Package Signal Assignments for 9S12H256, 3S12H256 and 3S12H192

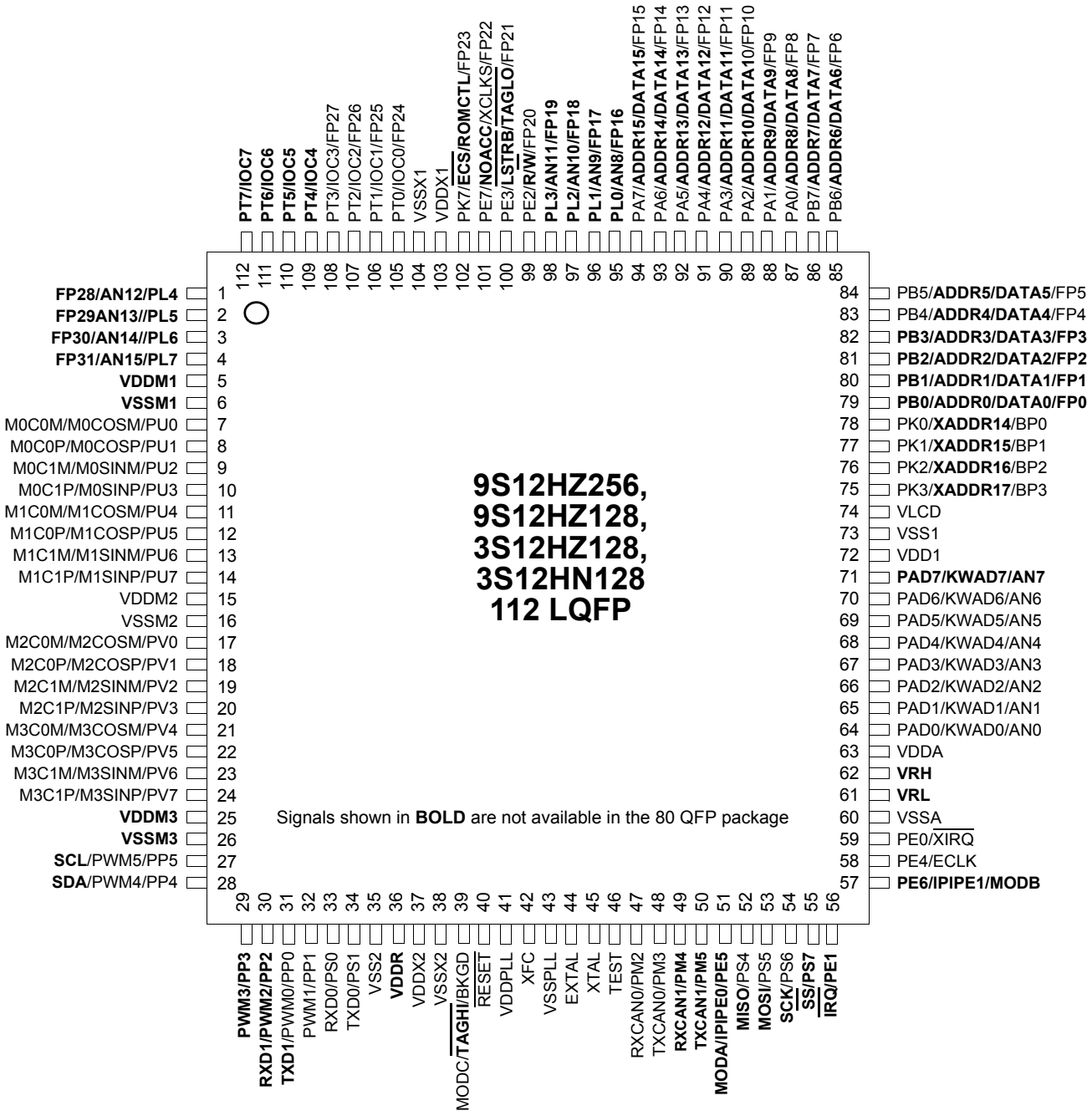

Figure 3. 112-Pin Package Signal Assignments for 9S12HZ256, 9S12HZ128, 3S12HZ128 and 3S12HN128

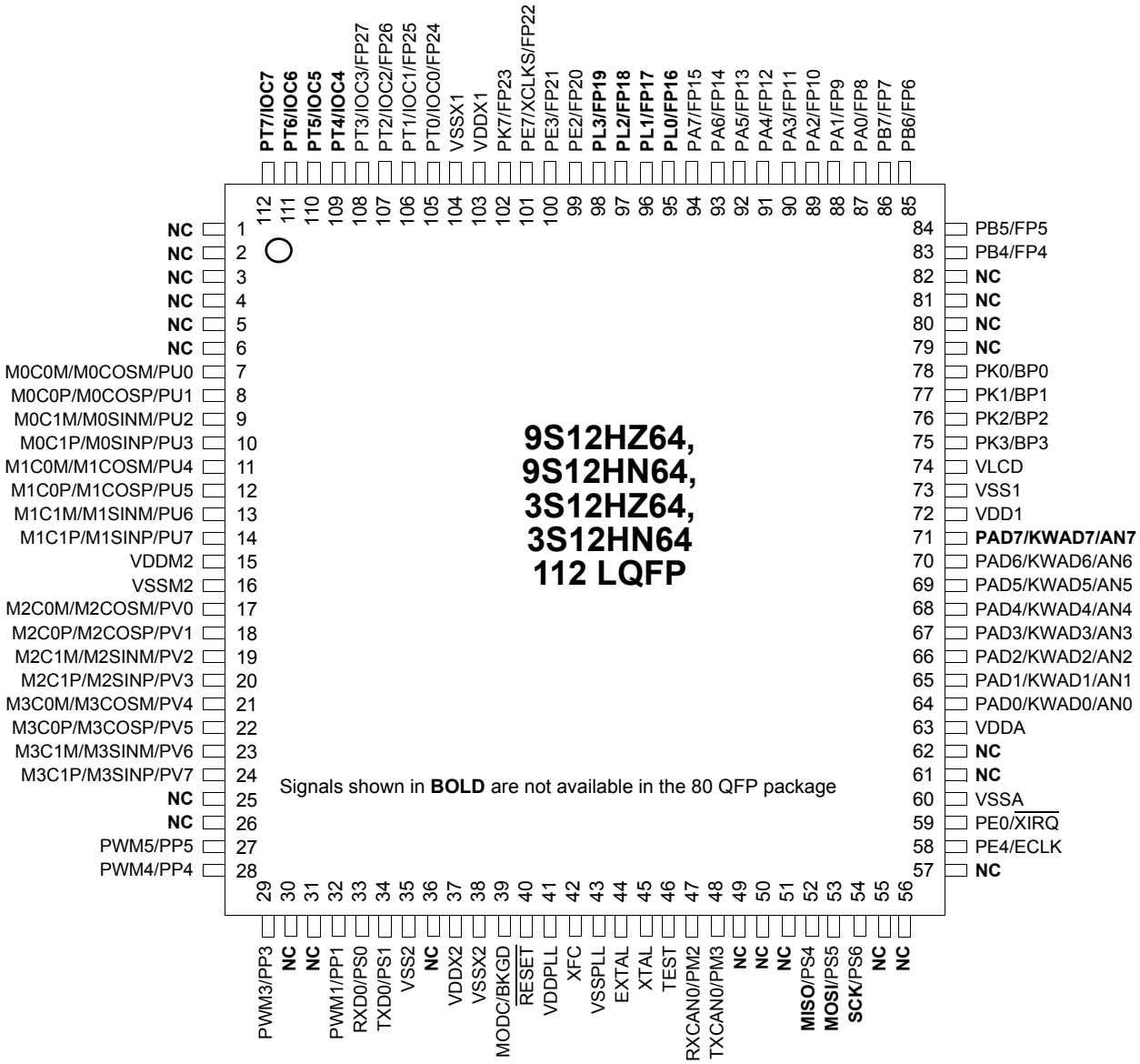

Figure 4. 112-Pin Package Signal Assignments for 9S12HZ64, 9S12HN64, 3S12HZ64 and 3S12HN64

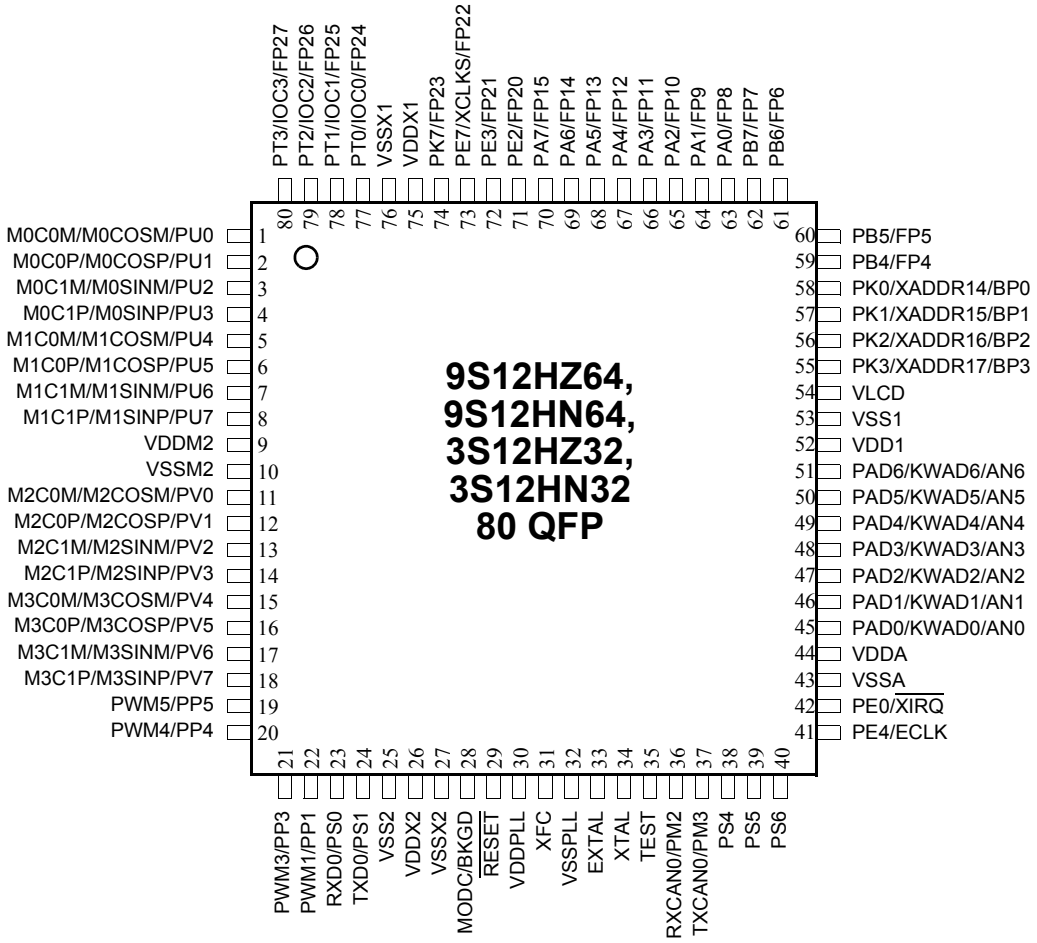

Figure 5. 80-Pin Package Signal Assignments for 9S12HZ64, 9S12HN64, 3S12HZ32 and 3S12HN32

Table 2 Pin Descriptions

Note: Features shown in bold are not available in the 9S12H256 112 pin QFP package.
Note: Features shown in Italics are only available for the "Z" versions

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Description
EXTAL	—	—	—	Crystal driver and external clock input pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output
XTAL	—	—	—	
$\overline{\text{RESET}}$	—	—	—	Active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.
TEST	—	—	—	Test Input
BKGD	$\overline{\text{TAGHI}}$	MODC	—	Function 1: Pseudo-open-drain communication pin for the background debug function. Function 2: In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. Function 3: At the rising edge during reset, the state of this pin is latched to the MODC bit to set the MCU operating mode.
PAD[15:8]	**AN[15:8]**	—	—	**Function 1: Port AD general purpose inputs** **Function 2: Analog inputs (ATD)**
PAD[7:0]	AN[7:0]	*KWAD[7:0]*	—	Function 1: Port AD general purpose inputs Function 2: Analog inputs (ATD) *Function 3: Key wake-up input pins that can generate an interrupt causing the MCU to exit STOP or WAIT mode.*
PA[7:0]	FP[15:8]	ADDR[15:8]/DATA[15:8]	—	Function 1: Port A general purpose input or output pins. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.
PB[7:0]	FP[7:0]	ADDR[7:0]/DATA[7:0]	—	Function 1: Port B general purpose input or output pins. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.
PE7	FP22	$\overline{\text{XCLKS}}$	NOACC	Function 1: Port E general purpose input or output pin Function 2: LCD frontplane segment driver output pin Function 3: The $\overline{\text{XCLKS}}$ signal selects between an external clock or oscillator configuration during reset. This pin should be at a logic high during reset if an external clock is used on the EXTAL input pin. This pin should be at a logic low during reset if an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-down device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL. Function 4: During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or "free" cycle. This signal will assert when the CPU is not using the bus.

Table 2 Pin Descriptions

Note: Features shown in bold are not available in the 9S12H256 112 pin QFP package.
Note: Features shown in Italics are only available for the "Z" versions

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Description
PE6	IPIPE1	MODB	—	Function 1: Port E general purpose input or output pins. Function 2: Instruction queue tracking signals. Function 3: The state of the MODA and MODB pins during reset determine the initial operating mode of the MCU
PE5	IPIPE0	MODA	—	
PE4	ECLK	—	—	Function 1: Port E general purpose input or output pin. Function 2: Internal bus clock output that can be used as a timing reference.
PE3	FP21	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	Function 1: Port E general purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ is used for the low-byte strobe function to indicate the type of bus access. Function 4: When instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.
PE2	FP20	R/$\overline{\text{W}}$	—	Function 1: Port E general purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operations, performs the read/write output signal for the external bus. This pin indicates direction of data on the external bus.
PE1	$\overline{\text{IRQ}}$	—	—	Function 1: Port E general purpose input pin. Function 2: Maskable interrupt request input provides a means of applying asynchronous interrupt requests. Will wake up the MCU from STOP or WAIT mode
PE0	$\overline{\text{XIRQ}}$	—	—	Function 1: Port E general purpose input pin. Function 2: Nonmaskable interrupt request input provides a means of applying asynchronous interrupt requests. Will wake up the MCU from STOP or WAIT mode.
PH[7:0]	**KWH[7:0]**	—	—	**Function 1: Port H general purpose input or output pins. Function 2: Key wake-up input pins that can generate an interrupt causing the MCU to exit STOP or WAIT mode.**
PJ[3:0]	**KWJ[3:0]**	—	—	**Function 1: Port J general purpose input or output pins. Function 2: Key wake-up input pins that can generate an interrupt causing the MCU to exit STOP or WAIT mode.**
PK7	FP23	$\overline{\text{ECS}}$	ROMCTL	Function 1: Port K general purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map. Function 4: During MCU expanded modes of operation, this pin is used as the emulation chip select signal.
PK[3:0]	BP[3:0]	XADDR[17:14]	—	Function 1: Port K general purpose input or output pins. Function 2: LCD backplane segment driver output pins. Function 3: In MCU expanded modes of operation, expanded address pins for the external bus.
PL[7:4]	***FP[31:28]***	***AN[15:12]***	—	***Function 1: Port L general purpose input or output pins. Function 2: LCD frontplane segment driver output pins. Function 3: Analog inputs (ATD).***

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Table 2 Pin Descriptions

Note: Features shown in bold are not available in the 9S12H256 112 pin QFP package.
Note: Features shown in Italics are only available for the "Z" versions

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Description
PL[3:0]	FP[19:16]	*AN[11:08]*	—	Function 1: Port L general purpose input or output pins. Function 2: LCD frontplane segment driver output pins. *Function 3: Analog inputs (ATD).*
PM5	TXCAN1	—	—	Function 1: Port M general purpose input or output pin. Function 2: Transmit pin for the Motorola Scalable Controller Area Network controller 1 (MSCAN1).
PM4	RXCAN1	—	—	Function 1: Port M general purpose input or output pin. Function 2: Receive pin for the Motorola Scalable Controller Area Network controller 1 (MSCAN1).
PM3	TXCAN0	—	—	Function 1: Port M general purpose input or output pin. Function 2: Transmit pin for the Motorola Scalable Controller Area Network controller 0 (MSCAN0).
PM2	RXCAN0	—	—	Function 1: Port M general purpose input or output pin. Function 2: Receive pin for the Motorola Scalable Controller Area Network controller 0 (MSCAN0).
PM1	**SCL**	—	—	**Function 1: Port M general purpose input or output pin. Function 2: Serial clock pin for the Inter-IC Bus Interface (IIC).**
PM0	**SDA**	—	—	**Function 1: Port M general purpose input or output pin. Function 2: Serial data pin for the Inter-IC Bus Interface (IIC).**
PP5	***PWM5***	***SCL***	—	***Function 1: Port P general purpose input or output pins. Function 2: Pulse Width Modulator (PWM) channel output pins. Function 3: Serial clock pin for the Inter-IC Bus Interface (IIC).***
PP4	***PWM4***	***SDA***	—	***Function 1: Port P general purpose input or output pins. Function 2: Pulse Width Modulator (PWM) channel output pins. Function 3: Serial data pin for the Inter-IC Bus Interface (IIC).***
PP3	***PWM3***	—	—	***Function 1: Port P general purpose input or output pins. Function 2: Pulse Width Modulator (PWM) channel output pins. Function 3: Transmit pin of Serial Communication Interface 1 (SCI1).***
PP2	***PWM2***	***RXD1***	—	***Function 1: Port P general purpose input or output pins. Function 2: Pulse Width Modulator (PWM) channel output pins. Function 3: Receive pin of Serial Communication Interface 1 (SCI1).***
PP1	PWM1	—	—	Function 1: General purpose input or output pin. Function 2: Pulse Width Modulator (PWM) channel output pin.
PP0	PWM0	***TXD1***	—	Function 1: General purpose input or output pin. Function 2: Pulse Width Modulator (PWM) channel output pin. ***Function 3: Transmit pin of Serial Communication Interface 1 (SCI1).***

Table 2 Pin Descriptions

Note: Features shown in bold are not available in the 9S12H256 112 pin QFP package.
Note: Features shown in Italics are only available for the "Z" versions

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Description
PS7	$\overline{SS}$	—	—	Function 1: Port S general purpose input or output pin. Function 2: Slave select pin for the Serial Peripheral Interface (SPI).
PS6	SCK	—	—	Function 1: Port S general purpose input or output pin. Function 2: Serial clock pin for the Serial Peripheral Interface (SPI).
PS5	MOSI	—	—	Function 1: Port S general purpose input or output pin. Function 2: Master output (during master mode) or slave input (during slave mode) pin for the Serial Peripheral Interface (SPI).
PS4	MISO	—	—	Function 1: Port S general purpose input or output pin. Function 2: Master input (during master mode) or slave output (during slave mode) pin for the Serial Peripheral Interface (SPI).
PS3	**TXD1**	—	—	**Function 1: Port S general purpose input or output pin. Function 2: Transmit pin of Serial Communication Interface 1 (SCI1).**
PS2	**RXD1**	—	—	**Function 1: Port S general purpose input or output pin. Function 2: Receive pin of Serial Communication Interface 1 (SCI1).**
PS1	TXD0	—	—	Function 1: Port S general purpose input or output pin. Function 2: Transmit pin of Serial Communication Interface 0 (SCI0).
PS0	RXD1	—	—	Function 1: Port S general purpose input or output pin. Function 2: Receive pin of Serial Communication Interface 0 (SCI0).
PT[7:4]	IOC[7:4]	—	—	Function 1: Port T general purpose input or output pins. Function 2: Timer input capture or output compare pins.
PT[3:0]	IOC[3:0]	FP[27:24]	—	Function 1: Port T general purpose input or output pins. Function 2: Timer input capture or output compare pins. Function 3: LCD frontplane segment driver output pins.
PU7	M1C1P	—	—	Function 1: Port U general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state.
PU6	M1C1M	—	—	
PU5	M1C0P	—	—	Function 1: Port U general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state.
PU4	M1C0M	—	—	
PU3	M0C1P	—	—	Function 1: Port U general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 0. PWM output on M0C1M results in a positive current flow through coil 1 when M0C1P is driven to a logic high state.
PU2	M0C1M	—	—	

Table 2 Pin Descriptions

Note: Features shown in bold are not available in the 9S12H256 112 pin QFP package.
Note: Features shown in Italics are only available for the "Z" versions

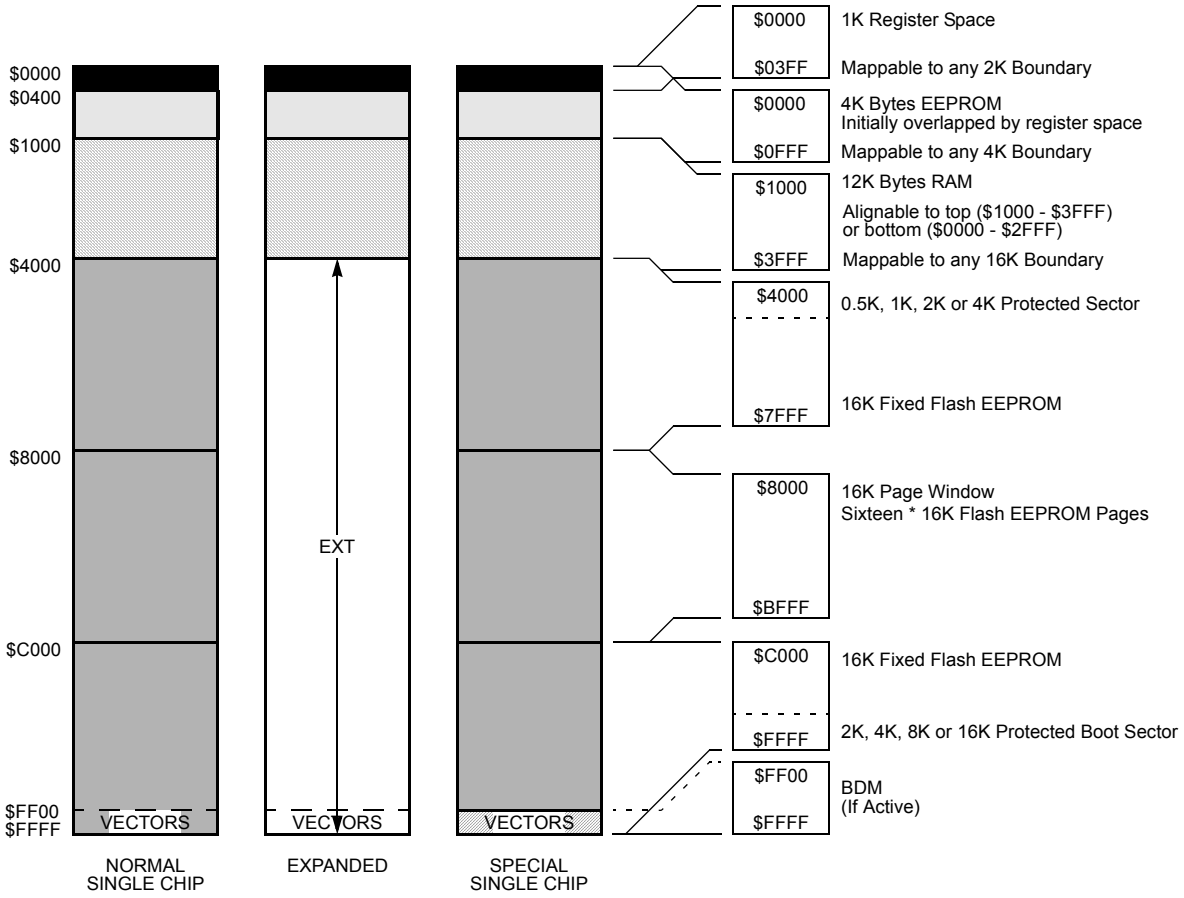
Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Description
PU1	M0C0P	—	—	Function 1: Port U general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 0. PWM output on M0C0M results in a positive current flow through coil 0 when M0C0P is driven to a logic high state.
PU0	M0C0M	—	—	
PV7	M3C1P	—	—	Function 1: Port V general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state.
PV6	M3C1M	—	—	
PV5	M3C0P	—	—	Function 1: Port V general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state.
PV4	M3C0M	—	—	
PV3	M2C1P	—	—	Function 1: Port V general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state.
PV2	M2C1M	—	—	
PV1	M2C0P	—	—	Function 1: Port V general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven to a logic high state.
PV0	M2C0M	—	—	
PW7	M5C1P	—	—	Function 1: Port W general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C1M results in a positive current flow through coil 1 when M5C1P is driven to a logic high state.
PW6	M5C1M	—	—	
PW5	M3C0P	—	—	Function 1: Port W general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C0M results in a positive current flow through coil 0 when M5C0P is driven to a logic high state.
PW4	M5C0M	—	—	
PW3	M4C1P	—	—	Function 1: Port W general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C1M results in a positive current flow through coil 1 when M4C1P is driven to a logic high state.
PW2	M4C1M	—	—	
PW1	M4C0P	—	—	Function 1: Port W general purpose input or output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C0M results in a positive current flow through coil 0 when M4C0P is driven to a logic high state.
PW0	M4C0M	—	—	
VLCD	—	—	—	Supply input pin for the LCD driver. Adjusting the voltage on this pin will change the display contrast.

Table 2 Pin Descriptions

Note: Features shown in bold are not available in the 9S12H256 112 pin QFP package.
Note: Features shown in Italics are only available for the "Z" versions

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Description
VDDA	—	—	—	Supply input pins for the voltage regulator and the analog to digital converter. Tolerance = 5V ± 5%.
VSSA	—	—	—	
VRH	—	—	—	Reference voltage input pins for the analog to digital converter.
VRL	—	—	—	
VDDM1	—	—	—	Supply input pins for motor 0 and motor 1 output drivers. Tolerance = 5 V ± 10%.
VSSM1	—	—	—	
VDDM2	—	—	—	Supply input pins for motor 2 and motor 3 output drivers. Tolerance = 5 V ± 10%.
VSSM2	—	—	—	
VDDM3	—	—	—	Supply input pins for motor 4 and motor 5 output drivers. Tolerance = 5 V ± 10%.
VSSM3	—	—	—	
VDDPLL	—	—	—	PLL supply output pins. No load allowed except for bypass capacitors.
VSSPLL	—	—	—	
VDDX1	—	—	—	Supply input pins for input/output drivers. Tolerance = 5V ± 5%.
VSSX1	—	—	—	
VDDX2	—	—	—	
VSSX2	—	—	—	
VDD1	—	—	—	Core supply output pins. No load allowed except for bypass capacitors.
VSS1	—	—	—	
VSS2	—	—	—	
VDDR	—	—	—	Power supply input pin for voltage regulator. Nominal 5V

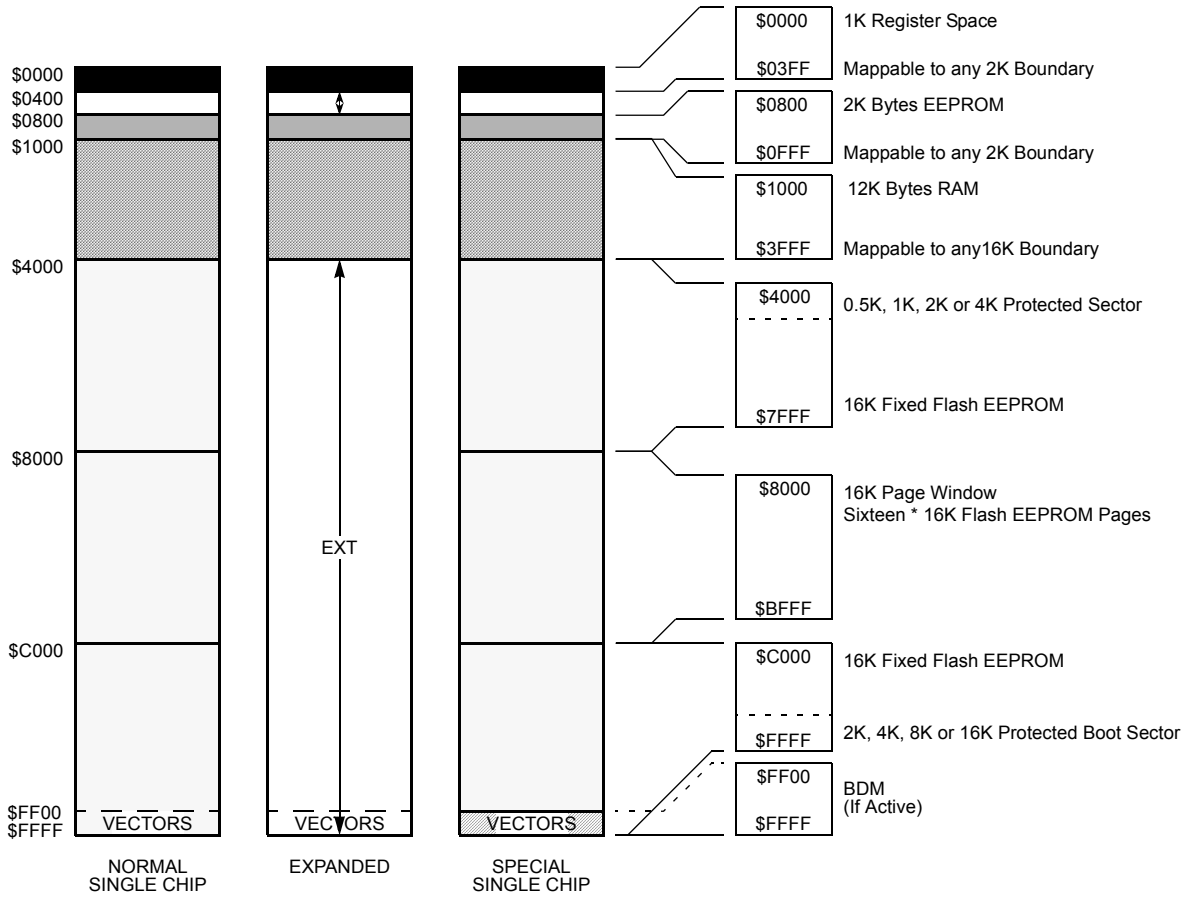
Memory Maps



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$1000 - $3FFF: 12K RAM for MC9S12H256
$0000 - $0FFF: 4K EEPROM (1K not visible) on MC9S12H256 only.
There is no mapping of EEPROM Flash on MC3S12H256.

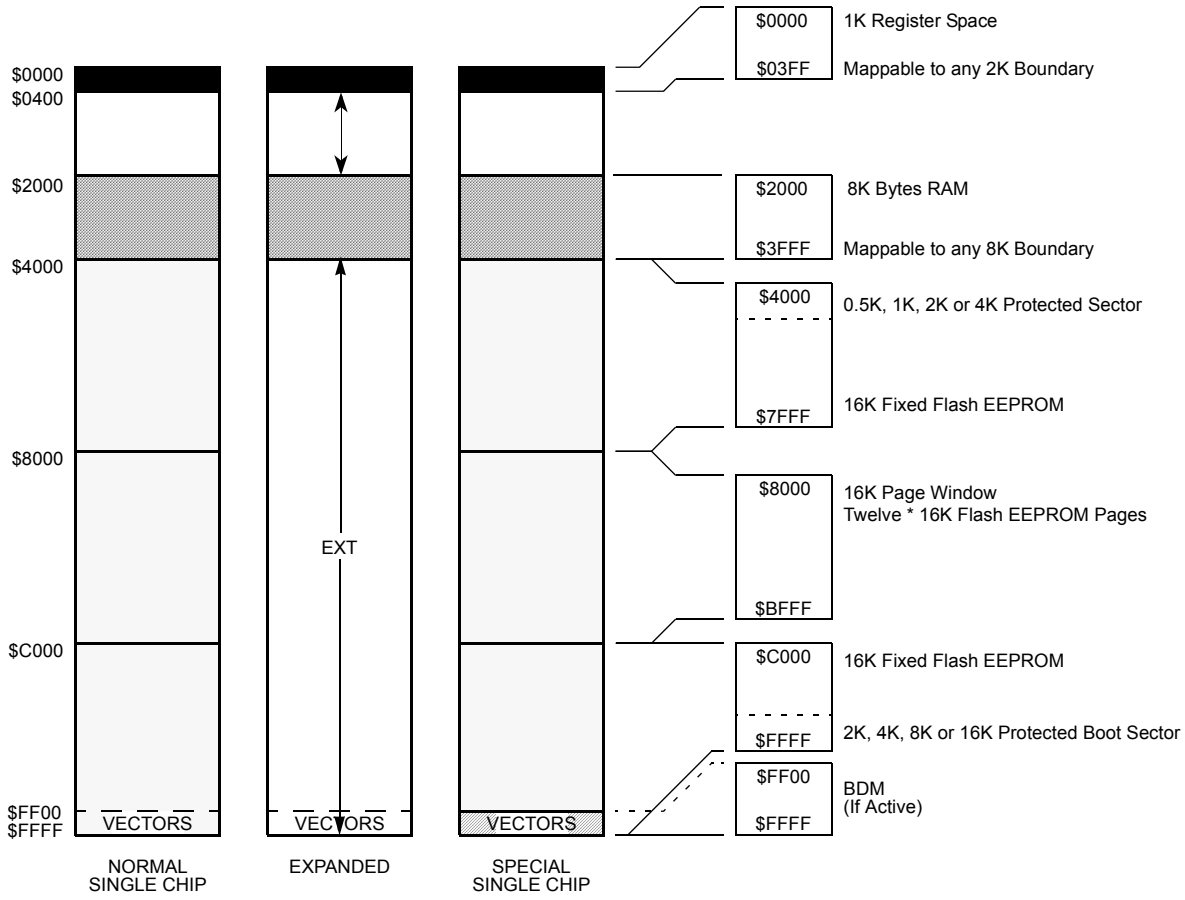
Figure 6. MC9(3)S12H256 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$1000 - $3FFF: 12K RAM
$0000 - $07FF: 2K EEPROM (1K not visible)
There is no mapping of EEPROM Flash on MC3S12HZ256.

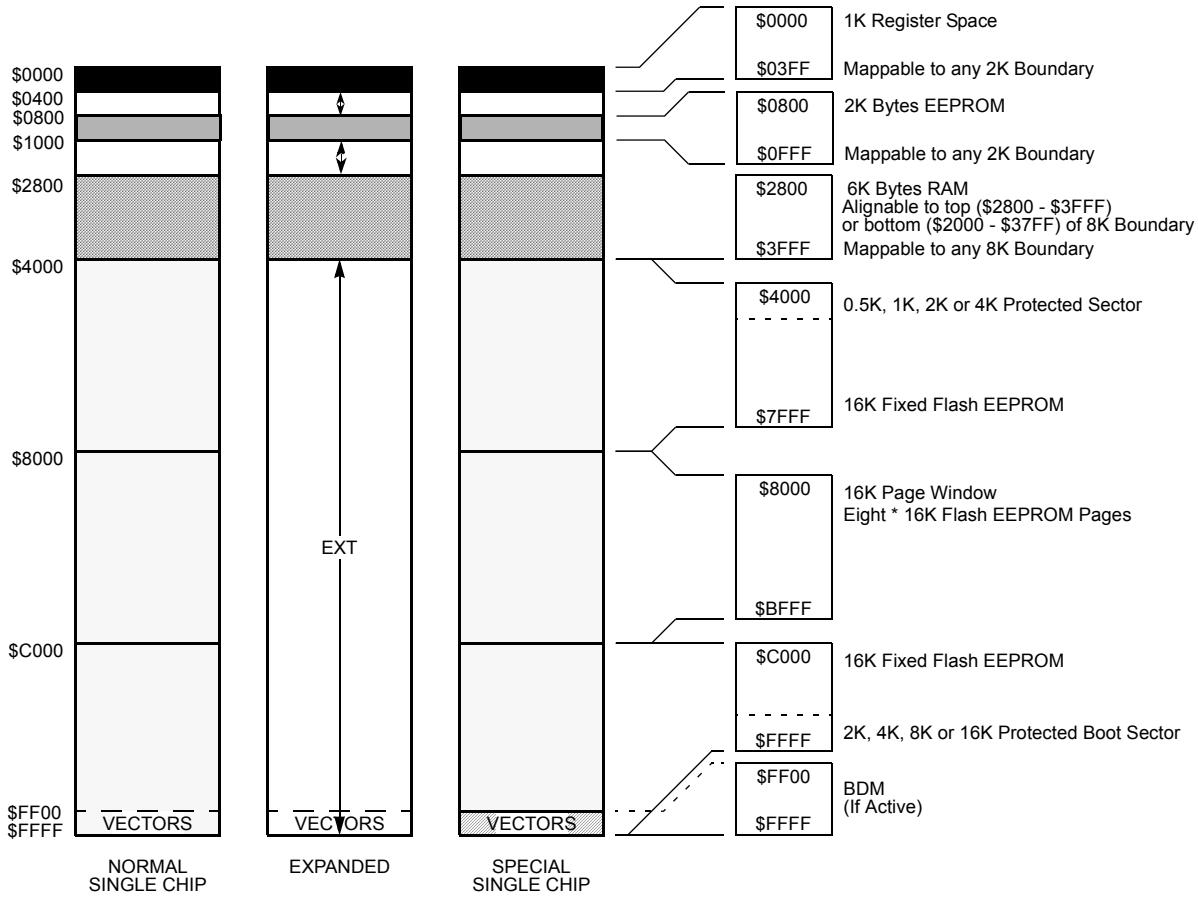
Figure 7. MC9(3)S12HZ256 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM (1K not visible)

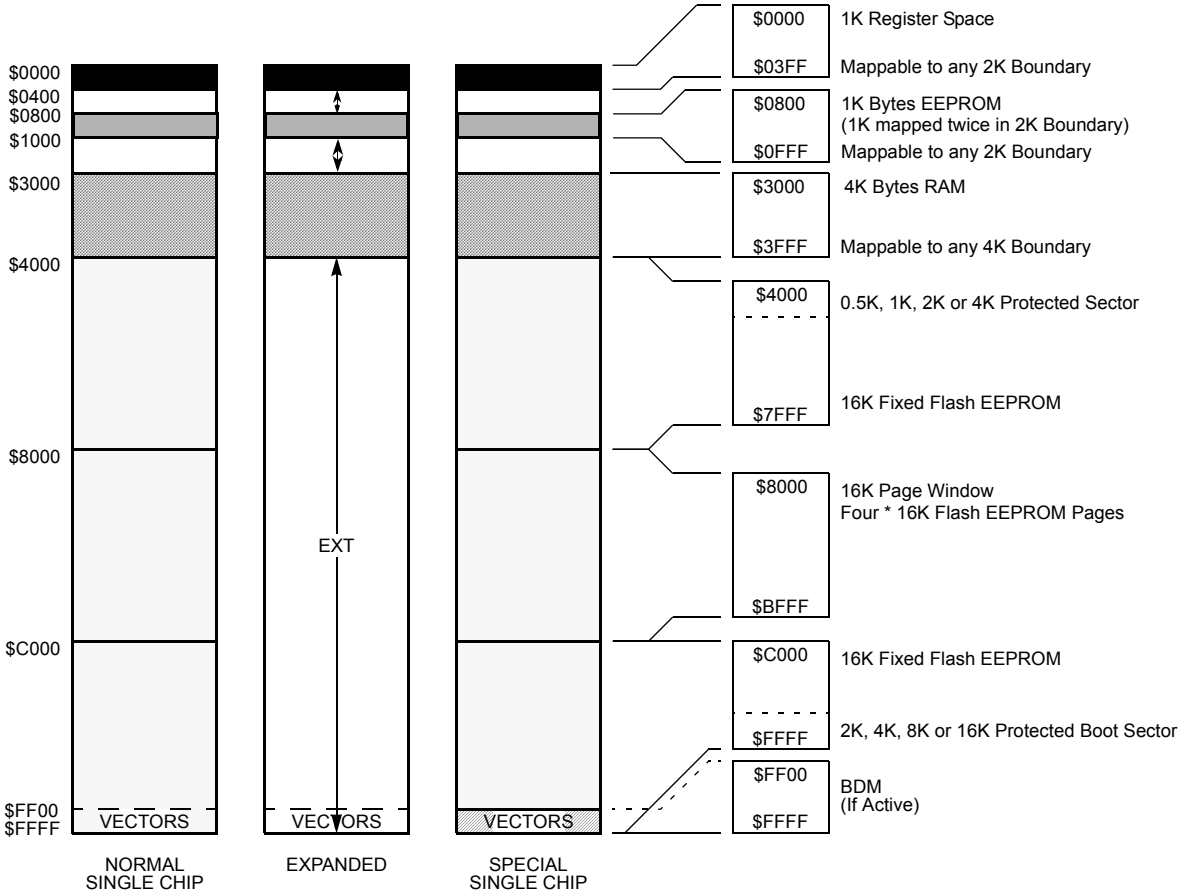
Figure 8. MC3S12HZ192 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0800 - $1FFF: 6K RAM
$0000 - $07FF: 2K EEPROM (1K not visible)
There is no mapping of EEPROM Flash on MC3S12HZ(N)128.

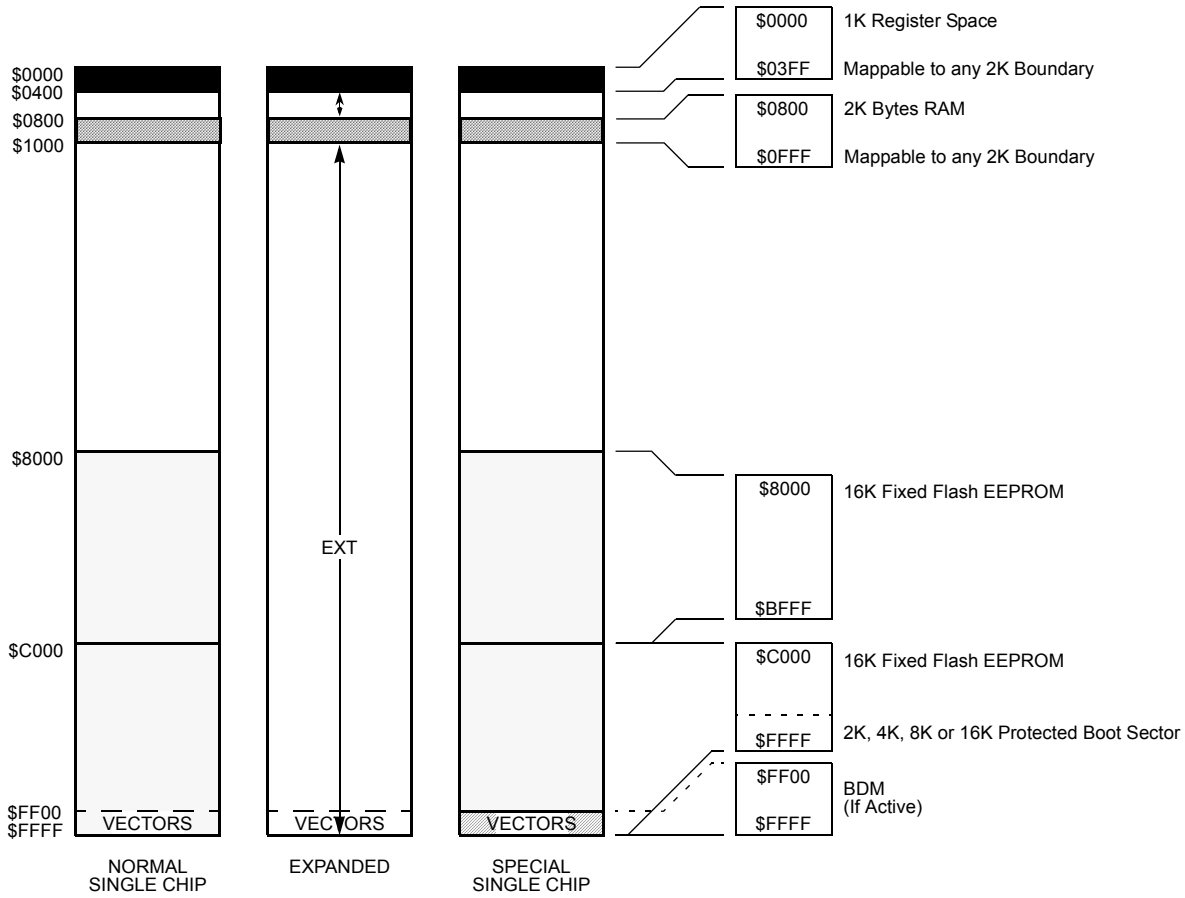
Figure 9. MC9(3)S12HZ(N)128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $0FFF: 4K RAM (1K not visible)
$0000 - $07FF: 1K EEPROM mapped twice (not visible)
There is no mapping of EEPROM Flash on MC3S12HZ(N)64

Figure 10. MC9(3)S12HZ(N)64 User Configurable Memory Map



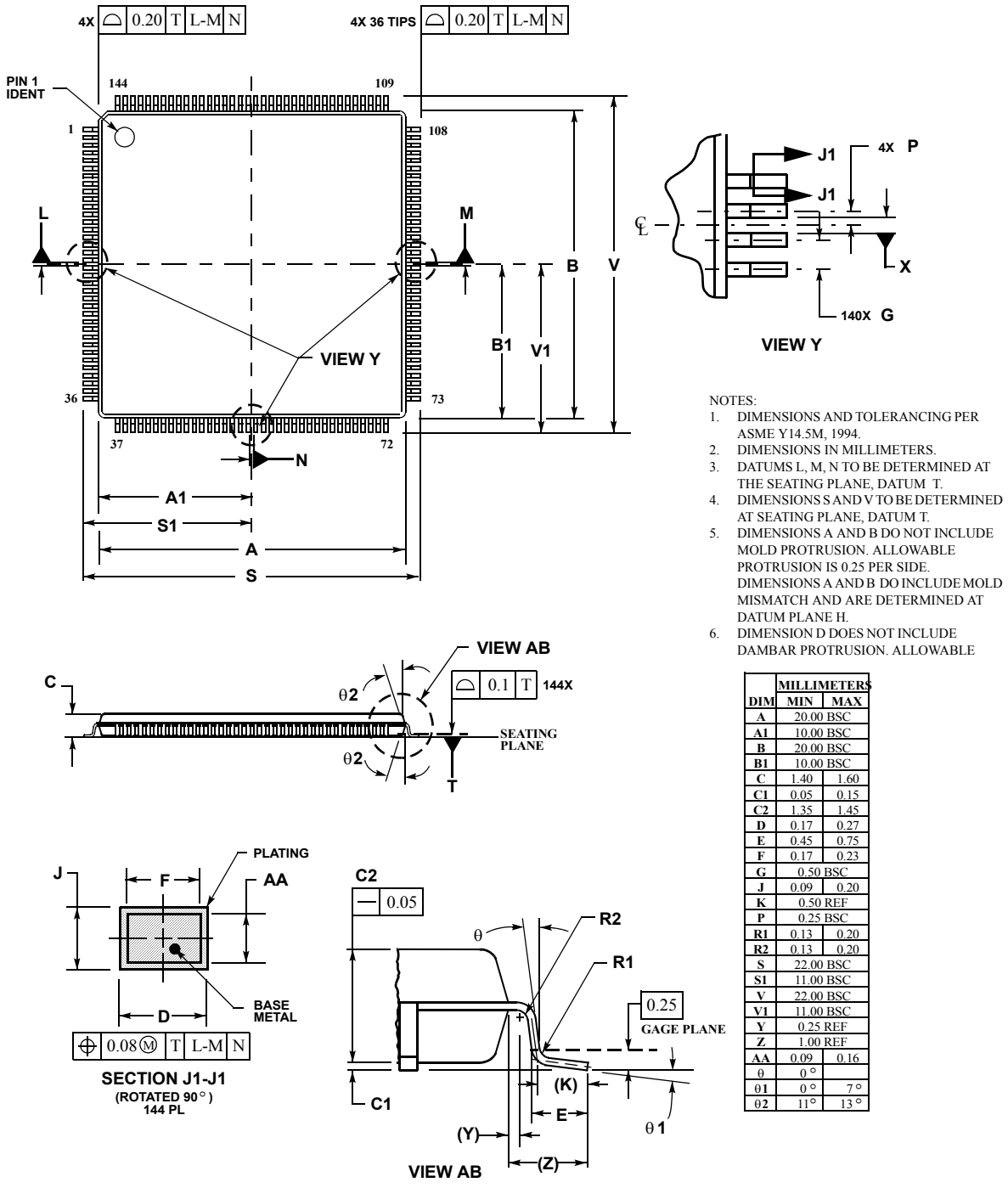
The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0800 - $0FFF: 2K RAM

Figure 11. MC3S12HZ(N)32 User Configurable Memory Map

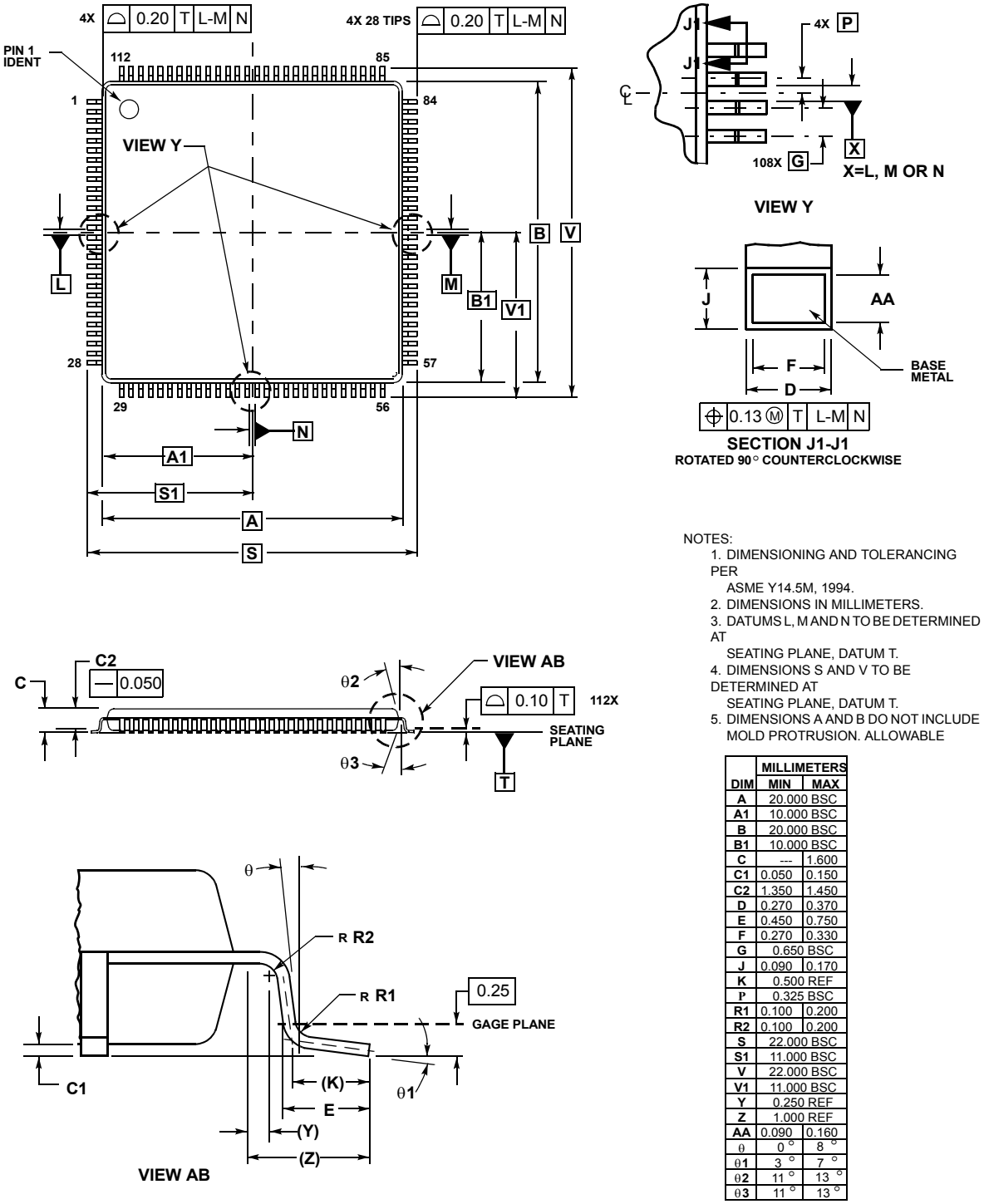
PRELIMINARY

Mechanical Package Dimensions



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

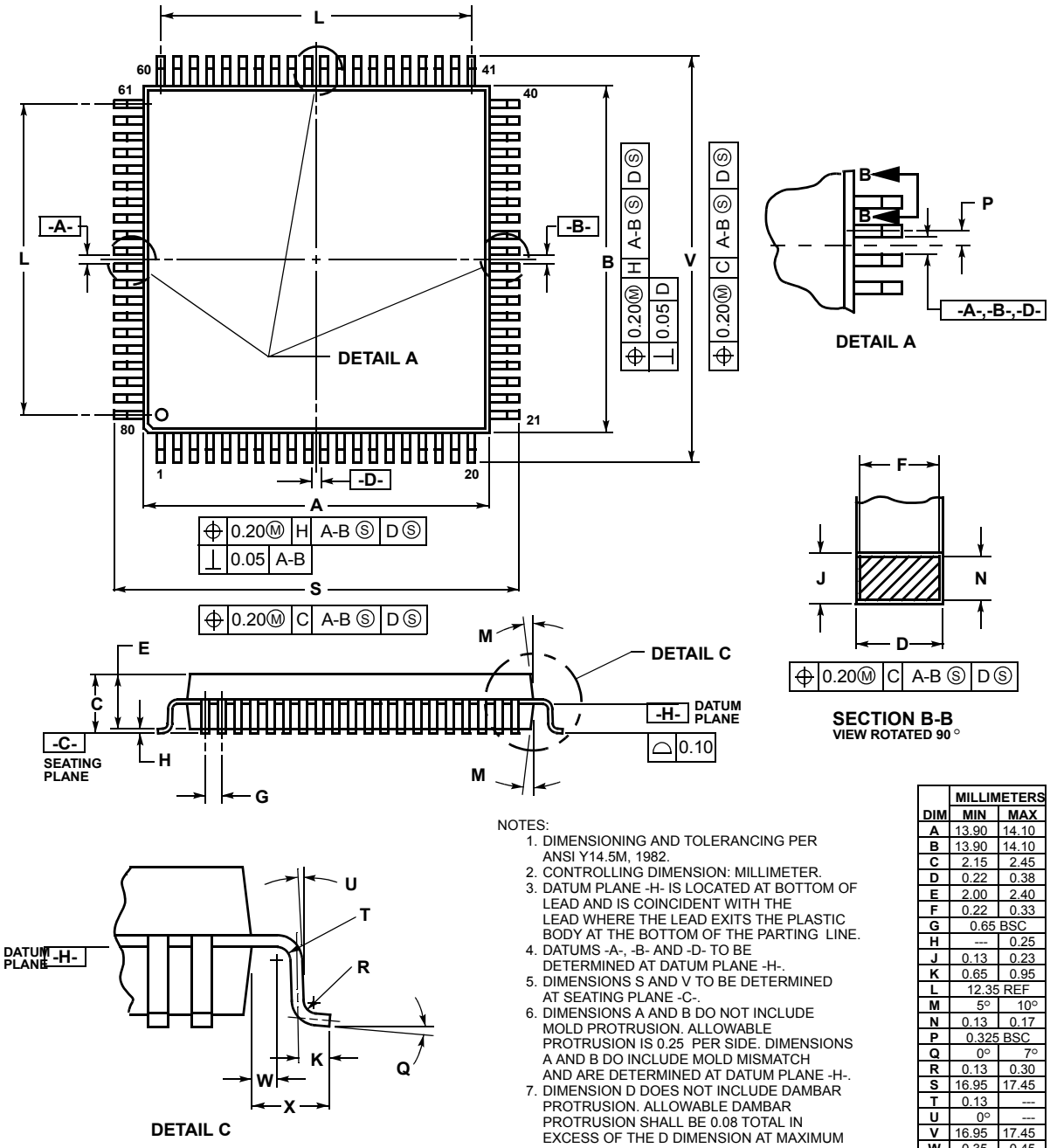
Figure 3. 144-pin LQFP Mechanical Dimensions (case no. 918-03)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 4. 112-pin LQFP Mechanical Dimensions (case no. 987)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 5. 80-pin QFP Mechanical Dimensions (case no. 841B)

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