Microchip

AY8930

Enhanced Programmable Sound Generator

FEATURES

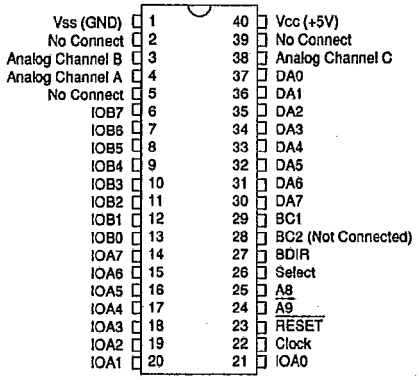
- Two Modes Available On-Chip
  - AY8930 Expanded Mode
  - AY38910A-Compatible Mode
- Improved Frequency Range
- Three Independently Programmable Analog Output Channels with Separate Frequency, Duty Cycle and Envelope Controls for Each Channel
- 5 Bits of Logarithmic Digital-to-Analog Conversion Per Channel
- Bus Interface Independent of Clock Frequency
- Input Clock Frequency: 2 or 4MHz
- Two 8-Bit General Purpose I/O Ports

PIN CONFIGURATION

40 LEAD DUAL INLINE

AY8930

Top View



DESCRIPTION

The AY8930 Enhanced Programmable Sound Generator (EPSG) is an LSI circuit that can produce a wide variety of complex sounds under software control. The AY8930 is manufactured in the Microchip Technology Inc. n-channel silicon gate process. The AY8930 is an enhanced version of the company's industry standard AY38910A sound generator. Enhanced features include improved frequency range and noise synthesis and independent control of each channel's envelope and duty cycle.

The PSG is easily interfaced to any bus-oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling, and personal computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable analog sound output channels available in the device. These analog sound output channels can each provide five bits of logarithmic digital-to-analog conversion, greatly enhancing the dynamic range of the sounds produced.

All circuit control signals are digital in nature and can be provided directly by a microprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

DEVICE ARCHITECTURE

The AY8930 is a register oriented PSG. Communication between the microprocessor and the PSG is based on the concept of memory mapped I/O. Control commands are issued to the PSG by writing to these memory mapped registers. Each of the registers within the PSG is readable so that the microprocessor can determine, as necessary, present states or stored data values.

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PIN FUNCTIONS

DA7-DA0 (Input /Output/High Impedance)
Data/Address Bits 7-0: Pins 30-37

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG, and to receive data from the PSG. In the address mode, DA3-DA0 select the internal register address (0-Fn) and DA7-DA4 in conjunction with address inputs $\overline{A9}$ and A8, form the chip select function. When the high order address bits are "incorrect," the bidirectional buffers are forced to a high impedance state.

$\overline{\text{Address 9}}$, Address 8
A8 (input): Pin 25
$\overline{A9}$ (input): Pin 24

High order address bits $\overline{A9}$ and A8 are fixed to recognize a "01" code. They may be left unconnected, as each is provided with either an on chip pull-down ($\overline{A9}$) or pull-up (A8) resistor. In noisy environments, however, it is recommended that $\overline{A9}$ and A8 be tied to external ground and +5V respectively, if they are not to be used.

RESET (Input): Pin 23

For initialization/power-on purposes, applying a low level input to the $\overline{\text{RESET}}$ pin will reset all registers to 0. (See following table). The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor.

Register (In Hex)	B7	B6	B5	B4	B3	B2	B1	B0
R0/R0A	0	0	0	0	0	0	0	0
R1/R1A	0	0	0	0	0	0	0	0
R2/R2A	0	0	0	0	0	0	0	0
R3/R3A	0	0	0	0	0	0	0	0
R4/R4A	0	0	0	0	0	0	0	0
R5/R5A	0	0	0	0	0	0	0	0
R6/R6A	0	0	0	0	0	0	0	0
R7/R7A	0	0	0	0	0	0	0	0
R8/R8A	#	#	0	0	0	0	0	0
R9/R9A	#	#	0	0	0	0	0	0
RA/RAA	#	#	0	0	0	0	0	0
RB/RBA	0	0	0	0	0	0	0	0
RC/RCA	0	0	0	0	0	0	0	0
RD/RDA/RDB	0	0	0	0	0	0	0	0
RE/REA	0	0	0	0	0	0	0	0
RF/RFA	0	0	0	0	0	0	0	0
R0B	0	0	0	0	0	0	0	0
R1B	0	0	0	0	0	0	0	0
R2B	0	0	0	0	0	0	0	0
R3B	0	0	0	0	0	0	0	0
R4B	#	#	#	#	X	X	X	X
R5B	#	#	#	#	X	X	X	X
R6B	#	#	#	#	X	X	X	X
R7B	#	#	#	#	X	X	X	X
R8B	#	#	#	#	X	X	X	X
R9B	0	0	0	0	0	0	0	0
RAB	X	X	X	X	X	X	X	X
RFB	0	0	0	0	0	0	0	0

- X indicates a don't care.
- # indicates that there is no physical memory element for a bit; if read, a 0 will be returned.
- All counter work registers will be initialized to zeros.
- The noise generator 17-bit shift register will be initialized to ones.
- The noise value register will be initialized to zeros.

CLOCK (Input): Pin 22

This TTL compatible input supplies the timing reference for the Tone, Noise, and Envelope Generators.

CLOCK DIVIDE - SELECT (Input): Pin 26

Select = 0 Input Clock = 4 MHz max. (Divided internally by 2)
Select = 1 Input Clock = 2 MHz max.
The select pin is provided with an internal pull-up resistor such that the pin default condition is Select = 1.

BDIR, BC2, BC1 (Inputs): Pins 27, 28, 29

Bus Direction, Bus Control 2*, Bus Control 1
* Not connected

Analog Channel A, B, C (Outputs): Pins 4, 3, 38

Each of these signals is the output of its corresponding digital-to-analog converter, and provides 1 V peak-peak (max) signal representing the complex sound wave-shape generated by the PSG.

No Connect: Pins 2, 5, 39

These pins are for Microchip Technology test purposes only and should be left open. Do not use as tie-points.

Vcc: Pin 40, Nominal +5 Volt power supply to the PSG.

Vss: Pin 1, Ground reference for the PSG.

INPUT CONTROL SIGNALS

Interfacing to the AY8930 requires the generation of only two of the three AY38910A input control signals, BDIR and BC1. BC2 is shown on the pinout diagram for reference only; the pin is not internally connected.

INPUT CONTROL SIGNALS

BDIR	BC1	Function
0	0	INACTIVE: The PSG/CPU bus is inactive. DA7-DA0 are in a high impedance state.
0	1	READ FROM PSG: This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7-DA0 are in the output mode.
1	0	WRITE TO PSG: This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7-DA0 are in the input mode.
1	1	LATCH ADDRESS: This signal indicates that the bus contains a register address which should be latched by the PSG. DA7- DA0 are in the input mode.

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REGISTER ARRAY

The principal element of the AY8930 is an array of 27 control registers arranged in one bank of 16 and one bank of 11 registers. These registers occupy 16 address locations of the 1,024-word memory space in which the PSG resides.

The configuration of this register array is shown on the following pages. Note the two modes of operation: 8910A-compatibility mode and 8930 expanded mode.

The registers are addressed via the combination of the bidirectional data bus (DA0-DA7) and address input pins A8 and $\overline{A9}$.

$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	X	X	X	X

DA0-DA3 These four low-order address bits are used to select one of the internal registers within a bank.

DA4-DA7, A8, $\overline{A9}$ These six high-order address bits function as chip selects and are used to position the register bank(s) within the 1,024-word memory space. In the deselected state, the data bus is in the high impedance state.

The address enable code for bits DA4-DA7 is all zeros.

Inputs A8 and $\overline{A9}$ are enabled by a high on A8 and a low on $\overline{A9}$; all other input level combinations result in a deselected condition. Pins A8 and $\overline{A9}$ have an on-chip pull-up and pull-down resistor, respectively, and will assume the correct logic level if left unconnected.

Address bits DA7-DA0 are latched internally. This internally latched address is updated and modified on every "latch address" signal presented to the PSG via the BDIR and BC1 control lines.

The AY8930 initializes in the AY38910A-compatibility mode. To utilize the expanded features of the AY8930, an access code must be input to register R15 upon program initialization.

Entering a "101" code in bits B7-B5 of register R15 selects the 8930 expanded mode. In the 8930 expanded mode, bit B4 = 0 (R15) selects BANK A and B4 = 1 selects BANK B. All other bit selections are defined as 8910A-compatibility mode. Registers R15A and R15B are mapped into the same physical register.

Switching modes causes loss of all register data from the previous mode. All registers will be initialized except for the Mode Select code of R15.

Shown on the next page is the register configuration for the AY8930. Note that Bank A of the expanded mode is virtually identical to the single register array of the 8910A-compatibility mode.

T-77-13

AY8930 REGISTER ARRAY: AY38910A-COMPATIBILITY MODE

Register		Function	Bit							
Hex	Octal		B7	B6	B5	B4	B3	B2	B1	B0
R0	R0	Channel A Tone Period	8-Bit Fine Tune							
R1	R1						4-Bit Coarse Tune			
R2	R2	Channel B Tone Period	8-Bit Fine Tune							
R3	R3						4-Bit Coarse Tune			
R4	R4	Channel C Tone Period	8-Bit Fine Tune							
R5	R5						4-Bit Coarse Tune			
R6	R6	Noise Period				5-Bit Period Control				
R7	R7	Enable	IN/OUT		NOISE			TONE		
			IOB	IOA	C	B	A	C	B	A
R8	R10	Channel A Amplitude				M	L3	L2	L1	L0
R9	R11	Channel B Amplitude				M	L3	L2	L1	L0
RA	R12	Channel C Amplitude				M	L3	L2	L1	L0
RB	R13	Envelope Period	8-Bit Fine Tune							
RC	R14		8-Bit Coarse Tune							
RD	R15	Envelope Shape/Cycle	MODE SELECT				CONT.	ATT.	ALT.	HOLD
RE	R16	I/O Port A	8-Bit Parallel I/O on Port A							
RF	R17	I/O Port B	8-Bit Parallel I/O on Port B							

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AY8930 REGISTER ARRAY: EXPANDED CAPABILITY MODE - BANK A

Register		Function	Bit							
Hex	Octal		B7	B6	B5	B4	B3	B2	B1	B0
R0A	R0A	Channel A	8-Bit Fine Tune							
R1A	R1A	Tone Period	8-Bit Coarse Tune							
R2A	R2A	Channel B	8-Bit Fine Tune							
R3A	R3A	Tone Period	8-Bit Coarse Tune							
R4A	R4A	Channel C	8-Bit Fine Tune							
R5A	R5A	Tone Period	8-Bit Coarse Tune							
R6A	R6A	Noise Period	8-Bit Noise Period							
			IN/OUT		NOISE			TONE		
R7A	R7A	Enable	IOB	IOA	C	B	A	C	B	A
R8A	R10A	Channel A Amplitude			M	L4	L3	L2	L1	L0
R9A	R11A	Channel B Amplitude			M	L4	L3	L2	L1	L0
RAA	R12A	Channel C Amplitude			M	L4	L3	L2	L1	L0
RBA	R13A	Channel A	8-Bit Fine Tune							
RCA	R14A	Envelope Period	8-Bit Coarse Tune							
RDA	R15A	Bank A/B: Envelope A	1	0	1	0	CONT.	ATT.	ALT.	HOLD
REA	R16A	I/O Port A	8-Bit Parallel I/O on Port A							
RFA	R17A	I/O Port B	8-Bit Parallel I/O on Port B							

AY8930 REGISTER ARRAY: EXPANDED CAPABILITY MODE - BANK B

Register		Function	Bit							
Hex	Octal		B7	B6	B5	B4	B3	B2	B1	B0
R0B	R0B	Channel B	8-Bit Fine Tune							
R1B	R1B	Envelope Period	8-Bit Coarse Tune							
R2B	R2B	Channel C	8-Bit Fine Tune							
R3B	R3B	Envelope Period	8-Bit Coarse Tune							
R4B	R4B	Envelope Shape/Cycle B					CONT.	ATT.	ALT.	HOLD
R5B	R5B	Envelope Shape/Cycle C					CONT.	ATT.	ALT.	HOLD
R6B	R6B	Channel A Duty Cycle					4-Bit			
R7B	R7B	Channel B Duty Cycle					4-Bit			
R8B	R10B	Channel C Duty Cycle					4-Bit			
R9B	R11B	Noise "And" Mask	8-Bit							
RAB	R12B	Noise "Or" Mask	8-Bit							
RBB	R13B*									
RBC	R14B*									
RBD	R15B	Bank A/B: Envelope A	1	0	1	1	CONT.	ATT.	ALT.	HOLD
RBC	R16B*									
RBF	R17B*	TEST	NOT TO BE ACCESSED BY THE USER							

* Not accessible in AY8930 mode.

NOTE: All unused bits will be read back as "0".

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SOUND GENERATING BLOCKS

The basic blocks in the PSG that produce the programmed sounds include:

Tone Generators - Produce the basic pulse tone frequencies for each channel (A, B, C).

Noise Generator - Produces a frequency modulated pseudorandom noise output.

Mixers - Combine the outputs of the tone generators and the noise generator. One for each channel (A, B, C).

Amplitude Control - Provides the D/A converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the envelope generators, one for each channel (A, B, C).

Envelope Generators - Produce an envelope pattern that can be used to amplitude modulate the output of the mixer, one for each channel (A, B, C).

D/A Converters - The three D/A converters each produce up to a 32-level output signal as determined by the amplitude control.

OPERATION

Since all functions of the PSG are controlled by a host processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers*	Function
Tone Generator Control	R0A-R5A	Program tone periods
Duty Cycle Control	R6B-R8B	Select duty cycle
Noise Generator Control	R6A, R9B-RAB	Program noise period
Mixer Control	R7A	Enable tone/noise on selected channels
Amplitude Control	R8A-RAA	Select "fixed" or "variable" amplitudes
Envelope Generator Control	RBA-RDA, R0B-R5B	Program envelope period and envelope pattern
D/A Converters		Produces a 32-bit output signal

*All registers referenced are for the AY8930 Expanded Mode.

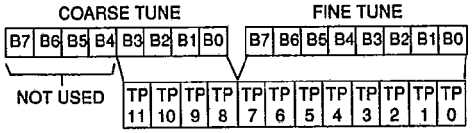
TONE GENERATOR CONTROL

Each analog output channel has associated with it two registers which specify the tone period for that channel, the coarse tune and the fine tune registers. The tone period for each channel is obtained by combining the coarse and fine tune registers as shown.

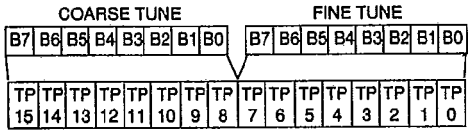
Note that the value programmed in the combined coarse and fine tune registers is a *period* value- the higher the value in the registers, the lower the resultant frequency.

Coarse Tune Registers	Channel	Fine Tune Register
R1A	A	R0A
R3A	B	R2A
R5A	C	R4A

12-BIT TONE PERIOD (TP) VALUE: AY38910A-COMPATIBILITY MODE



16-BIT TONE PERIOD (TP) VALUE: AY8930 EXPANDED MODE



PERIOD OF OUTPUT = 16 x TP x P
WHERE P = PERIOD OF INPUT CLOCK AND
TP = DECIMAL EQUIVALENT OF TONE PERIOD BITS TP15-TP0

If the coarse and fine tune registers are both set to 00h, the resulting period will be minimum, i.e. the generated tone period will be as if the coarse tune register were set to 00h and the fine tune register were set to 01h. The counter will count the period value down to zero. When zero is reached, the period value will be reloaded into the counter.

DUTY CYCLE CONTROL

The duty cycle of each pulse generated by the three tone generators is controlled by an associated 4-bit duty cycle register (R6B, R7B, and R8B).

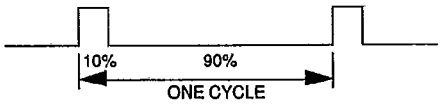
The following duty cycles are selectable:

% Duty Cycle	Duty Cycle	Register Value
3.125%	0	0000
6.25 %	1	0001
12.50%	2	0010
25.00%	3	0011
50.00%	4	0100
75.00%	5	0101
87.50%	6	0110
93.75%	7	0111
96.875%	8*	1000

* NOTE: Any value greater than 8_{10} decodes as an 8_{10}.

NOTE:

The percent duty cycles refers to the high (logic high) portion of the duty cycle. The low portion is then 100% duty cycle. For example, a 10% duty cycle is then 10% up and 90% down, as shown below.



In AY8910A-compatibility mode, the duty cycle is fixed at 50%. The capability for a variable duty cycle exists only in the expanded AY8930 mode.

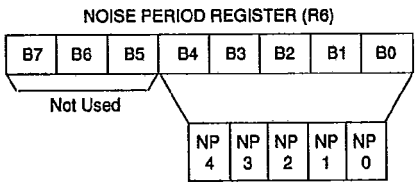
In order to change a duty cycle, the appropriate duty cycle register must be updated. The new duty cycle will then remain constant at this value until the duty cycle register is modified. The new duty cycle value will take effect immediately. This may result in one period with a "random" duty cycle at the time the register is updated.

NOISE GENERATOR CONTROL

AY38910A-COMPATIBILITY MODE:

Noise is generated by a 17-bit polynominal shift register. The period of the clock to this shift register is specified by the 8-bit binary value NP.

The noise period value is derived from the lower five bits (B4-B0) of the noise period register (R6) as shown.



NOTE:

As with the tone period, the lowest period value is 01h (divide by 1), an entry of 00h will have the same value as 01h; the highest period value is 1Fh (divide by 31_{10}).

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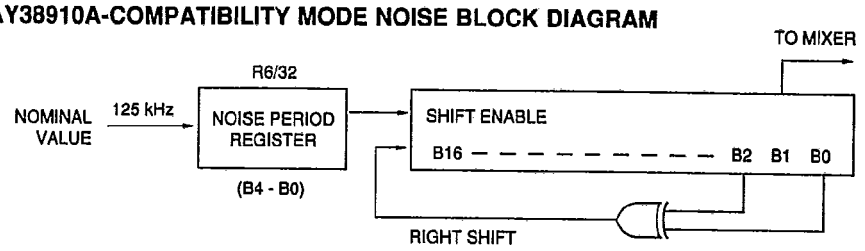
AY38910A-COMPATIBILITY MODE NOISE BLOCK DIAGRAM



AY8930 EXPANDED MODE:

In the AY8930 expanded mode, noise is generated using a 17-bit polynomial shift register, an "AND" mask, an "OR" mask, and an 8-bit noise period value. The least significant byte of the polynomial shift register is logically AND'ed with the "AND" mask specified in Register 11B, then logically OR'ed with the "OR" mask specified in Register 12B. The result is stored in a temporary register which is clocked each time the counter associated with the 8-bit noise period register (R6A) reaches zero. When the noise value reaches zero, a new value is fetched from the polynomial shift register and the process is repeated. The noise output is toggled each time the noise value reaches zero.

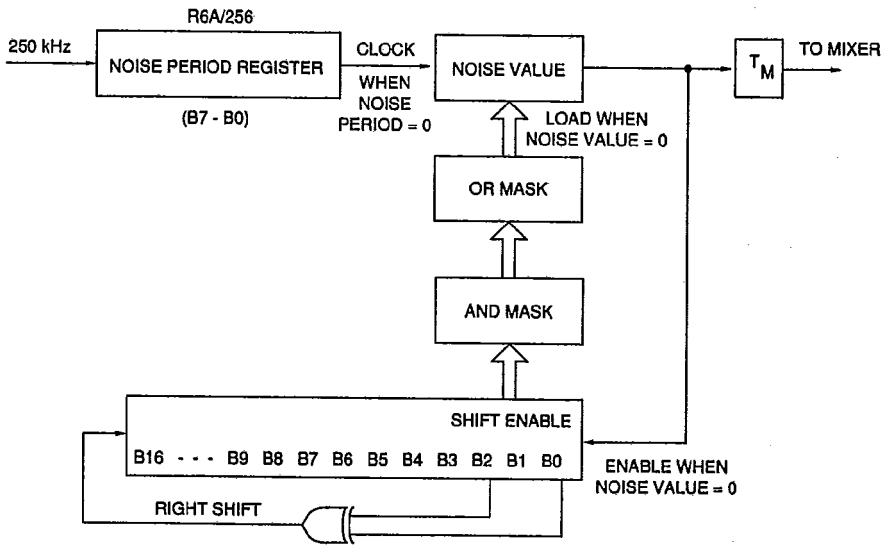
NOISE PERIOD REGISTER (R6A)

B7	B6	B5	B4	B3	B2	B1	B0
NP 7	NP 6	NP 5	NP 4	NP 3	NP 2	NP 1	NP 0

8 BIT NOISE PERIOD (NP) VALUE

The lowest period value is 01h (divide by 1), an entry 00h will have the same value as 01h; the highest period value is FFh (divide by 255$_{10}$.)

AY8930 EXPANDED MODE NOISE BLOCK DIAGRAM



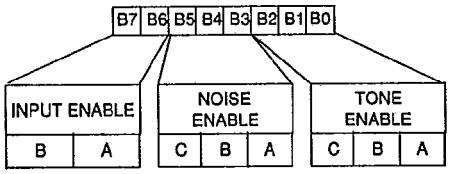
MIXER CONTROL - I/O ENABLE

Register 7A is a multi-function $\overline{\text{Enable}}$ register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports. The mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5-B0 of R7A.

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7A.

These functions are illustrated in the following:

MIXER CONTROL - I/O ENABLE REGISTER (R7A)



Noise Enable Truth Table

R7A Bits B5	B4	B3	Noise Enabled On Channel		
0	0	0	C	B	A
0	0	1	C	B	-
0	1	0	C	-	A
0	1	1	C	-	-
1	0	0	-	B	A
1	0	1	-	B	-
1	1	0	-	-	A
1	1	1	-	-	-

Tone Enable Truth Table

R7A Bits B2	B1	B0	Tone Enabled On Channel		
0	0	0	C	B	A
0	0	1	C	B	-
0	1	0	C	-	A
0	1	1	C	-	-
1	0	0	-	B	A
1	0	1	-	B	-
1	1	0	-	-	A
1	1	1	-	-	-

The direction of the I/O Port(s) is determined as follows:

I/O Port Truth Table

R7A Bits B7	B6	I/O Direction IOB	IOA
0	0	In	In
0	1	In	Out
1	0	Out	In
1	1	Out	Out

Note: The Mixer - I/O Control function is identical in both modes of operation.

Disabling noise and tone does not turn off a channel. Turning off a channel can only be accomplished by writing all zeros into corresponding amplitude control register.

I/O PORT DATA STORE

Registers REA and RFA function as intermediate data storage registers between the PSG/CPU data bus (DA0-DA7) and the two I/O ports (IOA0-IOA7, IOB0-IOB7). Both I/O ports are available on the AY8930.

Using registers REA and RFA for the transfer of I/O data has no effect on sound generation.

To output data from the CPU Bus to a peripheral device connected to I/O port A:

1. Address the enable register (R7A).
2. Set the port A direction bit to output (write "1" to bit B6 of R7A).
3. Address the I/O port A register (REA).
4. Write data to I/O port A register. The data will pass through the PSG I/O port A register to the I/O port bus.

To input data from I/O port A to the CPU bus:

1. Address the enable register (R7A).
2. Set the port A direction bit to input (write a "0" to bit B6 of R7A).
3. Address the I/O port A register (REA). The contents of the port register will follow the signals applied to the I/O port.
4. Read data from I/O port A register. The data will be transferred from the PSG I/O port A register to the CPU bus as in a normal read operation.

If a logic 1 has been written to any bit position of register REA or register RFA and the corresponding I/O pins of port A or port B are externally pulled below the logic 0, (V_{IL}) level, a subsequent CPU read instruction of registers REA or RFA will actually contain a logic 0 in the pulled down bit positions. The output pins will return to logic 1 if the pull down condition is removed.

If a logic 0 has been written to any bit position of the I/O registers and the external world wishes to pull these pins to a 1, the user should be aware that an impedence conflict will exist between the pull down transistor and the external driver.

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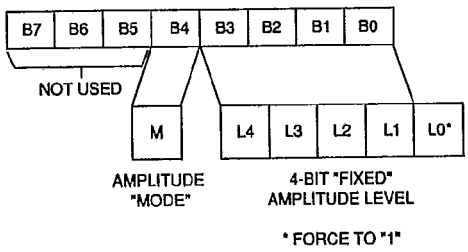
AMPLITUDE CONTROL

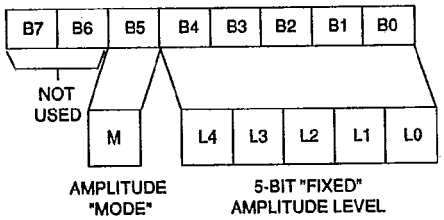
The amplitudes of the signals generated by each of the three D/A converters (one each for channels A, B, and C) are determined by the contents of the amplitude control registers as illustrated in the following:

Amplitude Control Register #	Channel
R8A	A
R9A	B
RAA	C

AY38910A-COMPATIBILITY MODE:



AY8930 EXPANDED MODE:



The amplitude "mode" (bit M) selects either fixed level amplitude (M = 0) or variable level amplitude (M = 1). It follows that bits L4 - L0, defining the value of a "fixed" level amplitude, are only active when M = 0. The amplitude is only "fixed" in the sense that the amplitude level is under the direct control of the system processor via an address latch/write data sequence.

When "variable amplitude" is selected (M = 1), the amplitude of each channel is determined by the envelope pattern as defined by the envelope generators 5-bit output (E4 - E0). The amplitude "mode" bit (bit M) can also be thought of as an envelope enable bit, i.e. when M = 1, the envelope is enabled.

The following is a chart describing all combinations of the 6-bit Amplitude Control.

M	L4	L3	L2	L1	L0	
0	0	0	0	0	0*	The amplitude is fixed at 1 of 31
0	0	0	0	0	1*	levels as determined by L4, L3,
•	•	•	•	•	•	L2, L1, L0.
•	•	•	•	•	•	
0	1	1	1	1	1	
1	X	X	X	X	X	The amplitude is variable at 31 levels as determined by the output of the Envelope Generator.

(X = Don't care)

NOTE:

In the AY38910A-compatibility mode, the externally driven "fixed" amplitude is limited to a total of 16 possible levels determined by amplitude bits L4-L1.

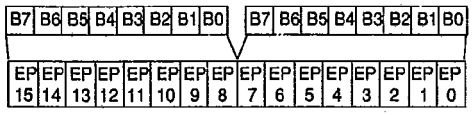
ENVELOPE GENERATOR CONTROL

ENVELOPE PERIOD CONTROL

The period of the sound envelope, in the AY38910A-compatibility mode, is controlled by two 8-bit registers, RB and RC (the envelope fine and coarse tune, respectively). In the 8930 expanded mode, each analog output channel has its own independent sound envelope. Changes to the envelope period counter will occur at envelope period boundary or when envelope shape/cycle register is loaded.

Coarse Tune Register	Channel	Fine Tune Register
RCA	A	RBA
R1B	B	R0B
R3B	C	R2B

16-BIT ENVELOPE PERIOD TO ENVELOPE GENERATOR



Note that the value programmed in the combined coarse and fine tune registers is a period value - the higher the value in the registers, the lower the resultant frequency.

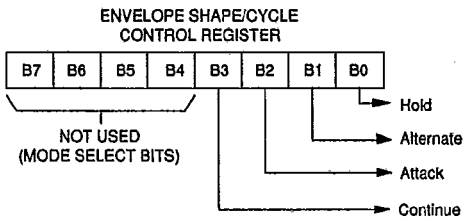
Note also, that as with the tone period, the lowest period value is 0001h (divided by 1); the highest period value is FFFFh (divided by 65,535$_{10}$).

ENVELOPE SHAPE/CYCLE CONTROL

The AY8930 envelope generator further counts down the envelope frequency by 32, producing a 32-state per cycle envelope pattern defined by its 5-bit counter output, E4, E3, E2, E1, and E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/ count down) of the 5-bit counter and by defining a single cycle repeat-cycle pattern. The AY38910A mode envelope generator further divides the envelope period by 16, producing a 16-state per cycle envelope pattern as defined by the 4-bit counter output, E3, E2, E1 and E0.

Loading of the envelope shape/cycle control register will reset the associated counter to the appropriate initial state and reset the envelope period counter for that channel.

The envelope shape/cycle control is contained in the lower 4 bits (B3-B0) of the respective envelope control registers. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following:



The definition of each function is as follows:

Hold - When set to logic "1" in AY38910A mode, limits the envelope to one cycle, holding the last count of the envelope counter (E3 - E0 = 0000 or 1111, depending on whether the envelope counter was in a count-down or count-up mode, respectively).

Alternate - When set to logic "1", the envelope counter reverses count direction (up-down) after each cycle.

NOTE: When both the hold bit and the alternate bit are ones, the envelope counter is reset to its initial count before holding.

Attack - When set to logic "1" in AY38910A mode, the envelope counter will count up (attack) from E3, E2, E1, E0 = 0000 to E3, E2, E1, E0 = 1111; when set to logic "0", the envelope counter will count down (decay) from 1111 to 0000.

Continue - When set to logic "1", the cycle pattern will be as defined by the hold bit; when set to logic "0", the envelope generator will be reset to 0000 after one cycle and hold at that count.

Further description of the above functions could be accomplished by numerous charts of the binary count sequence of E3, E2, E1, E0 for each combination of hold, alternate, attack and continue. However, since these ouputs are used (when selected by the amplitude control registers) to amplitude modulate the output of the mixers, a better understanding of their effect can be accomplished via a graphic representation of their value for each condition selected, as illustrated in the Envelope Shape/Cycle Control figure to the right and the Detail of Two Cycles figure below.

For AY8930 mode, hold, alternate, attack and continue is the same, however the pattern is defined by 5 bits (E4, E3, E2, E1, E0.)

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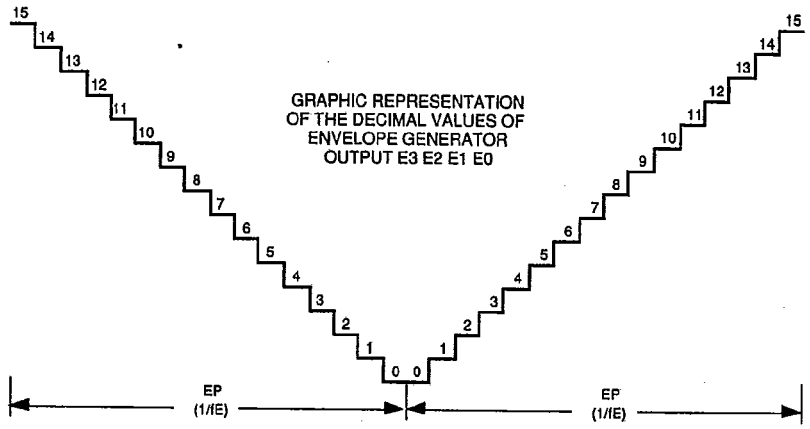
ENVELOPE SHAPE/CYCLE CONTROL

RD BITS B3	B2	B1	B0	AY38910A MODE
CONTINUE	ATTACK	ALTERNATE	HOLD	GRAPHIC REPRESENTATION OF ENVELOPE GENERATOR OUTPUT E3 E2 E1 E0.
0	0	X	X	
0	1	X	X	
1	0	0	0	
1	0	0	1	(SEE FIG. BELOW FOR DETAIL)
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

EP — EP IS THE ENVELOPE PERIOD (DURATION OF ONE CYCLE)

DETAIL OF TWO CYCLES - AY38910A MODE

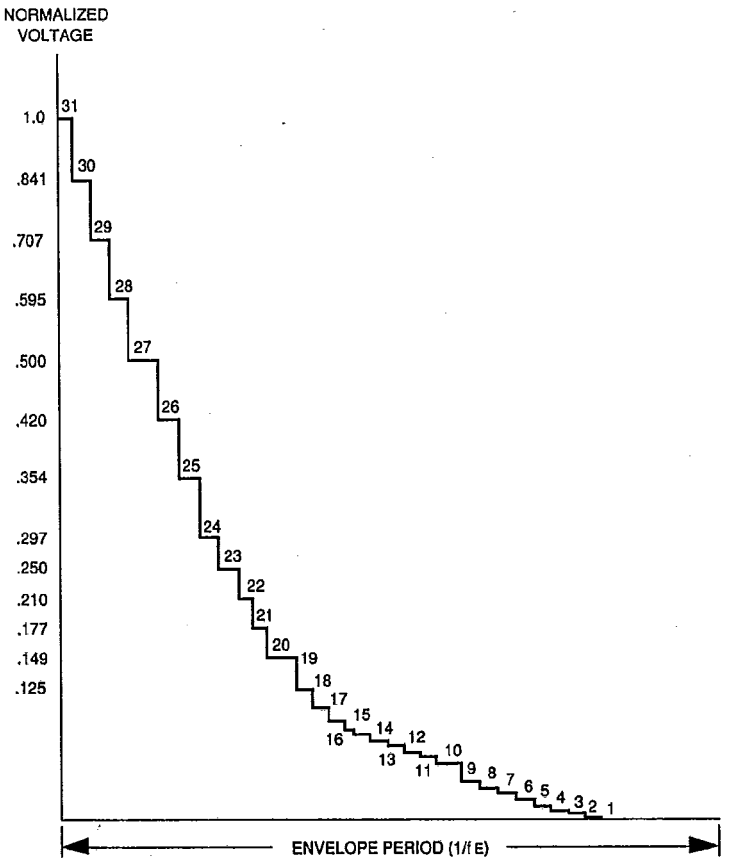


DIGITAL TO ANALOG CONVERTER

The Digital to Analog conversion is performed in logarithmetic steps with a normalized voltage range of 0V to 1.0V. The specified amplitude of each converter is controlled by a 5-bit word from either the amplitude control register* or the envelope generator. The signal of the output is the Noise/Tone specified for that channel.

* Except in the 8910A-compatibility mode, which only allows for 4 bits of external amplitude control.

D/A CONVERTER OUTPUT - AY8930 EXPANDED MODE



THIS FIGURE ILLUSTRATES THE D/A CONVERTER OUTPUT WHICH WOULD RESULT IF NOISE AND TONES WERE DISABLED AND AN ENVELOPE CONTROLLED VARIABLE AMPLITUDE WERE SELECTED.

NOTE: THE RESET CONDITION IS ZERO CURRENT.

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ELECTRICAL CHARACTERISTICS

Maximum Ratings*
Storage temperature.....-55°C to +150°C
Maximum temperature under bias ..... +125°C
VDD and all other input/output
voltages with respect to Vss.....-0.3V to +7.0V

Standard Conditions (Unless otherwise noted)
Free air ambient operating
temperature ..... 0°C to +70°C
VDD ..... +4.5V to +5.5V
Vss ..... 0.0V (Ground)

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Logic Levels						
Logic 0	VIL	-0.3	-	+0.4	Volts	
Logic 1	VIH	+ 2.4		VDD	Volts	
Input Leakage						
Clock	-	-	-	10	µA	
BC1, BDIR	-	-	-	10	µA	
Inputs with Pullups	IIL	10	-	100	µA	VIN = +0.4V
A8, RESET, Select						
Inputs with Pulldowns	IIH	10	-	50	µA	VIN = +2.4V
$\overline{A9}$						
I/O with Pullups						
A7-A0, B7-B0	IIL	20	-	150	µA	VIN = +0.4V
	VOH	+2.4	-	VDD	Volts	IOH = 100 µA w/100pF
	VOL	0.0	-	+0.4	Volts	IOL = 1.6 mA w/100pF
Data/Address						
DA7-DA0	VOH	+2.4	-	VDD	Volts	IOH = 100 µA w/100pF
	VOL	0.0	-	+0.4	Volts	IOL = 1.6 mA w/100pF
Power Supply	IDD	-	-	85	mA	All inputs and outputs tied to Vss or VDD.

AC CHARACTERISTICS *

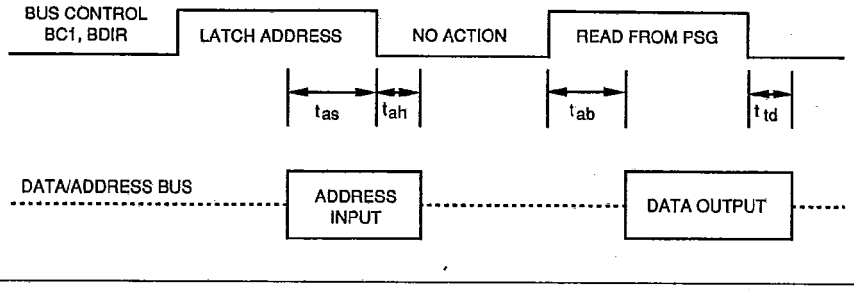
Parameters	Sym	Min	Typ	Max	Units	Conditions
Clock Input						
Frequency	-	1	-	4	MHz	40/60 asymmetry
Rise/Fall Time	tr, tf	0	-	50	ns	allowed
Master Reset						
$\overline{\text{RESET}}$	tms	*	-	-	ns	*Two Clock Periods
Control Signals						
BC1, BC2, BDIR						
Skew	tcs	-	-	40	ns	
Valid	tccs	300	-	-	ns	
Data Address Bus						
DA7-DA0, A8, $\overline{\text{A9}}$						
Address Setup Time	tas	300	-	-	ns	
Address Hold Time	tah	65	-	-	ns	
Read Mode						
Data Setup Time	tab	-	-	200	ns	
Data Hold Time	ttd	20	-	100	ns	
Write Mode						
Data Setup Time	tds	300	-	-	ns	
Data Hold Time	tdh	65	-	-	ns	
Input/Output Port						
IOA7-IOA0, IOB7-IOB0						
Output Mode						
Data Setup Time	tpw	500	-	-	ns	
Input Mode						
Data Setup Time	tprs	200	-	-	ns	
Data Hold Time	tprh	65	-	-	ns	

* The address/data read cycle is latch address followed by an inactive state then the read command. The address/data write cycle would be the same with the substitution of the write command in place of the read. An inactive state is required between each cycle (or active command).

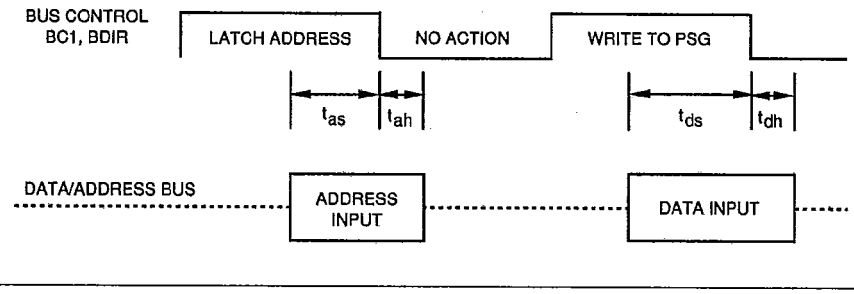
5

TIMING DIAGRAMS

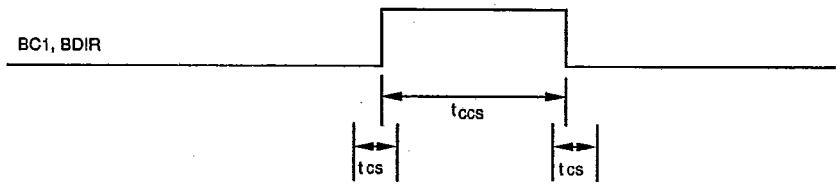
READ MODE



WRITE MODE



BUS CONTROL SIGNALS



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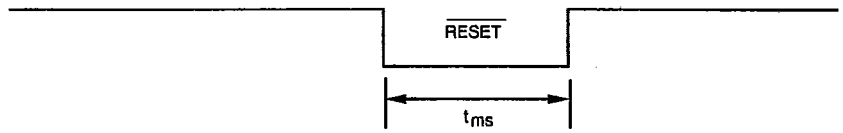
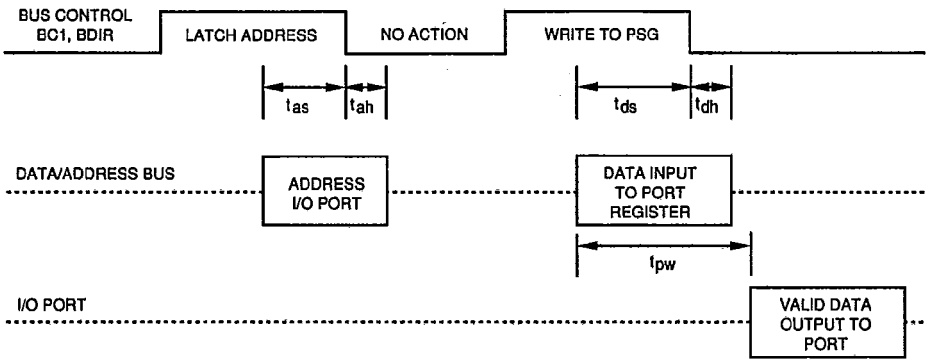
TIMING DIAGRAMS (Cont.)

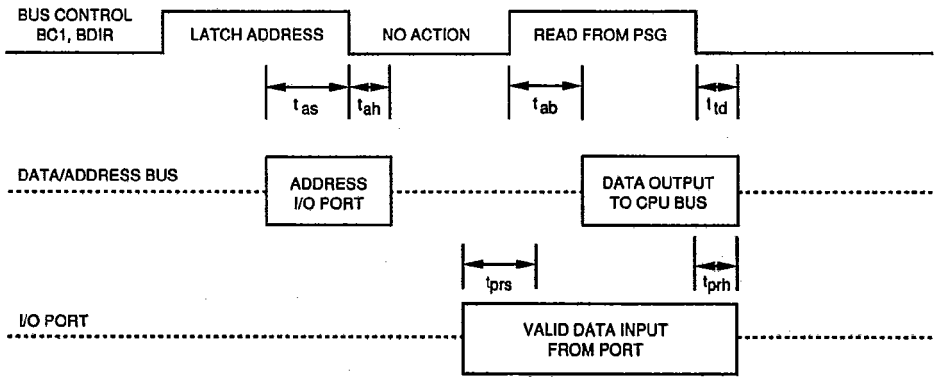
MASTER RESET



I/O PORT OUTPUT MODE: WRITE DATA FROM CPU BUS TO I/O PORT*



I/O PORT INPUT MODE: WRITE DATA FROM I/O PORT TO CPU BUS*



* Assume the direction of the I/O port has already been determined via a write to the Enable register (R7A).

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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

AY8930 - /P

Package	P	40-Pin Plastic DIP
Temperature Range	Blank	0° C to 70° C
Device	AY8930	Enhanced Programmable Sound Generator