XC25BS5 Series

PLL Clock Generator ICs with Built-In Divider/Multiplier Circuits (For Low Frequency Range)

◆CMOS Low Power Consumption
◆Input Frequency : 12kHz to 35MHz
◆Divider Ratio : 1, 3~2047 Divisions (Laser Trimming)
◆Multiplier Ratio : 6~2047 Multiplications (Laser Trimming)
◆Comparative Frequency : 12kHz~500kHz
◆Output Frequency : 3MHz ~30MHz

■APPLICATIONS

●Crystal oscillation modules
●Personal computers
●PDAs
●Portable audio systems
●Various system clocks

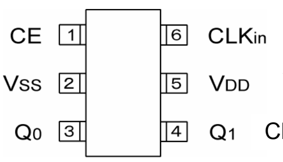
■GENERAL DESCRIPTION

The XC25BS5 series are high frequency, low power consumption PLL clock generator ICs with divider circuit & multiplier PLL circuit.
Laser trimming gives the option of being able to select from divider ratios (M) of 1,3 to 2047 and multiplier ratios (N) of 6 to 2047.
Output frequency (Q0) is equal to reference oscillation (fCLKin) multiplied by N/M, within a range of 3MHz to 30MHz. Q1 output is selectable from input reference frequency (f0), input reference frequency/2 (f0/2), ground (GND), and comparative frequency (f0/M). Further, comparative frequencies, within a range of 12KHz to 500KHz, can be obtained by dividing the reference oscillation. By halting operation via the CE pin, consumption current can be controlled and output will be one of high-impedance.

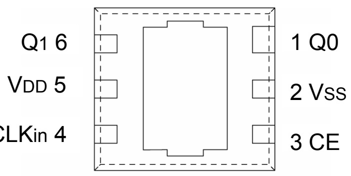
■FEATURES

Output Frequency : 3MHz ~ 30MHz (Q0=fCLKin × N/M)
Reference Oscillation (fCLKin) : 12kHz ~ 35MHz
Divider Ratio (M) : Selectable from divisions of 1, 3~2047
Multiplier Ratio (N) : Selectable from multiplications of 6~2047
Output : 3-State
Q1 output selectable from input reference oscillation, input reference oscillation/2, GND, comparative frequency.
Operating Voltage Range : 2.97V ~ 5.5V
Low Power Consumption : CMOS (stand-by function included)*1
Ultra Small Package: SOT-26, USP-6B
*1 High output impedance during standby

■PIN CONFIGURATION



SOT-26
(TOP VIEW)



USP-6B
(BOTTOM VIEW)

*The dissipation pad for the USP-6B package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release.
If the pad needs to be connected to other pins, it should be connected to the VDD pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-26	USP-6B		
1	3	CE	Chip Enable
2	2	VSS	GND
3	1	Q0	PLL Output
4	6	Q1	Reference Oscillation, Reference Oscillation/2, GND, or Comparative Frequency Output
5	5	VDD	Power Supply
6	4	CLKin	Reference Clock Input

■FUNCTION LIST

●CE, Q0/Q1 Pin Function

C E	FUNCTION
"H"	Q0, Q1 Clock Output
"L"	Stand-by. Output Pin = High Impedance
Open	Stand-by. Output Pin = High Impedance (VSS Pin Pull-Down Due to IC's Internal Resistor)

"H" = High level
"L" = Low level

■PRODUCT CLASSIFICATION

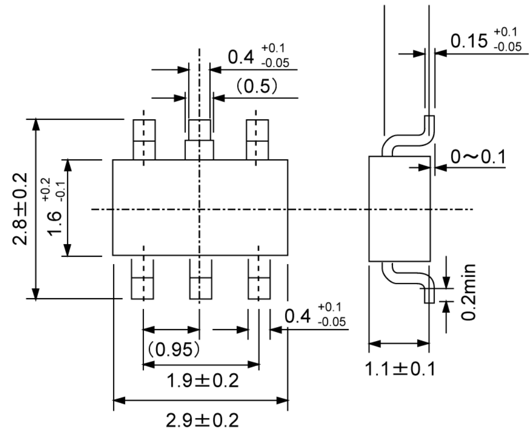
●Ordering Information

XC25BS5 ①②③④⑤

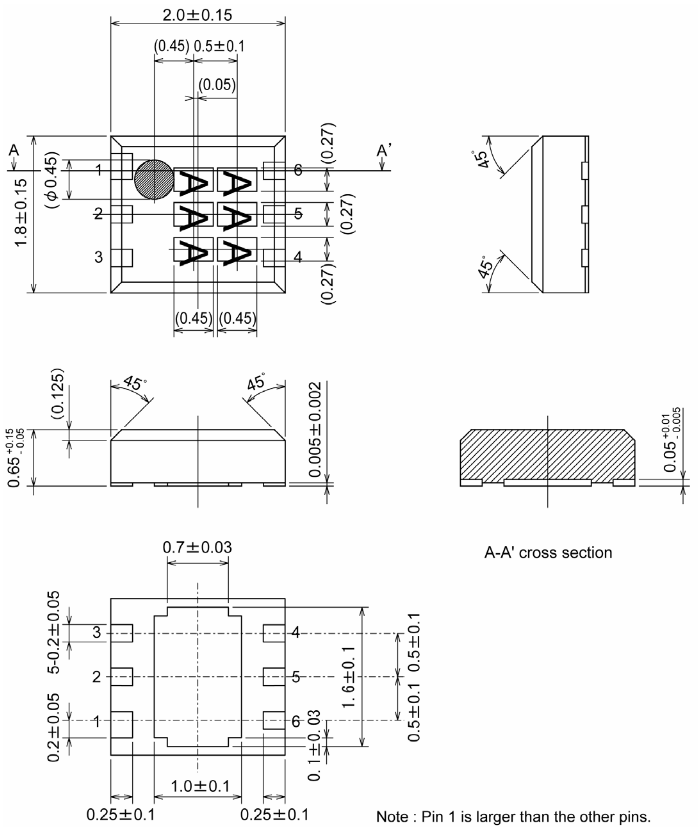
DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
① ② ③	Product Number	Integer	: Based on internal standards e.g. Product number 001 → ①②③ = 001
④	Package	M	: SOT-26
		D	: USP-6B
⑤	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed

■PACKAGING INFORMATION

●SOT-26

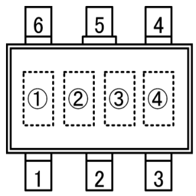


●USP-6B



■ MARKING RULE

●SOT-26



SOT-26
(TOP VIEW)

① Represents product series

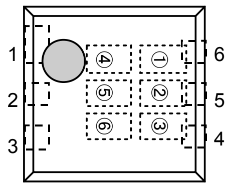
MARK	PRODUCT SERIES
5	XC25BS51xxMx

②③ Represents ② and ③ of ordering information

MARK		PRODUCT SERIES
②	③	
0	7	XC25BS5107Mx

④ Represents assembly lot number
(Based on internal standards)

●USP-6B



USP-6B
(TOP VIEW)

①,②,③ Represents product series

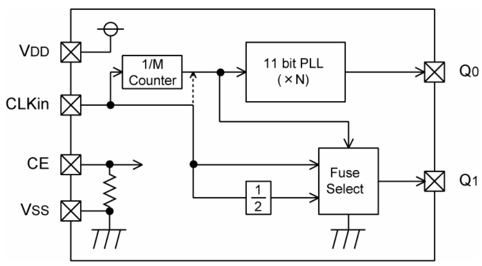
MARK			PRODUCT SERIES
①	②	③	
B	S	0	XC25BS50xxDx
S	5	S	XC25BS5SxxDx

④,⑤ Represents ② and ③ of ordering information (ex.)

MARK		PRODUCT SERIES
④	⑤	
0	7	XC25BS5007Dx
0	1	XC25BS5S01Dx

⑥ Represents production lot number
0 to 9,A to Z repeated (G, I, J, O, Q, W excepted)
Note: No character inversion used.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

PARAMETER		SYMBOL	CONDITIONS	UNITS
Supply Voltage		VDD	VSS-0.3 ~ VSS+7.0	V
CLKin Pin Voltage		VCK	VSS-0.3 ~ VDD+0.3	V
CE Pin Voltage		VCE	VSS-0.3 ~ VDD+0.3	V
Q0 Pin Voltage		VQ0	VSS-0.3 ~ VDD+0.3	V
Q1 Pin Voltage		VQ1	VSS-0.3 ~ VDD+0.3	V
Q0 Output Current		IQ0	±50	mA
Q0 Output Current		IQ1	±50	mA
Power Dissipation	SOT-26	Pd	150	mW
	USP-6B		100	
Operating Temperature Range		Topr	- 30 ~ + 80	℃
Storage Temperature Range		Tstg	- 40 ~ +125	℃

■ FREQUENCY CONFIGURATION: EXAMPLE 1

XC25BS51XXMR

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Frequency	f CLKin	11.0000	-	16.9344	MHz
Multiplier/Divider Ratio	N/M	-	1.594	-	-
PLL Output Frequency	fQ0	17.5383	-	27.0000	MHz
Q1 Output Frequency	Q1	GND			-

● Electrical Characteristics (DC)
XC25BS51xxMR

fCLKin = 16.9344MHz, Multiplier/Divider Ratio = 1.594, Ta = 25℃, No Load

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		2.97	3.30	3.63	V
Input Voltage "High"	V_{IH}		2.7	-	-	V
Input Voltage "Low"	V_{IL}		-	-	0.6	V
Input Current "High"	I_{IH}	V_{CK} = 3.3V	-	-	3.0	μA
Input Current "Low"	I_{IL}	V_{CK} = 0V	-3.0	-	-	μA
Output Voltage "High"	V_{OH}	V_{DD} = 2.97V, I_{OH} = -8mA	2.5	-	-	V
Output Voltage "Low"	V_{OL}	V_{DD} = 2.97V, I_{OL} = 8mA	-	-	0.4	V
Supply Current 1	I_{DD1}	CE = 3.3V	-	3.0	6.0	mA
Supply Current 2	I_{DD2}	CE = 0V	-	-	5.0	μA
CE "High" Voltage	V_{CEH}		2.7	-	-	V
CE "Low" Voltage	V_{CEL}		-	-	0.45	V
CE Pull-Down Resistance 1	Rp1	CE = 3.3V	0.5	1.5	2.5	MΩ
CE Pull-Down Resistance 2	Rp2	CE = 0.3V	20.0	50.0	80.0	kΩ

● Electrical Characteristics (AC)
XC25BS51xxMR

fCLKin=16.9344MHz, Multiplier/Divider Ratio=1.594, Ta=25℃, CL=15pF

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time	T_{TLH}	V_{DD}=3.3V(20% to 80%) (*1)	-	5.0	-	Ns
Output Fall Time	T_{THL}	V_{DD}=3.3V(20% to 80%) (*1)	-	5.0	-	Ns
Duty Ratio	DUTY		40	50	60	%
Output Start Time	Ton	(*1)	-	-	20	ms
PLL Output Jitter	Tj	1σ (*1)	-	40	-	ps

*1 R&D guarantee

■ FREQUENCY CONFIGURATION: EXAMPLE 2

XC25BS51XXMX

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Frequency	f CLKin	52.0000	-	78.0000	kHz
Multiplier/Divider Ratio	N/M	-	256.000	-	-
PLL Output Frequency	fQ0	13.312	-	19.968	MHz
Q1 Output Frequency	Q1	GND			-

●Electrical Characteristics (DC)
XC25BS51xxMR

fCLKin=78kHz, Multiplier/Divider Ratio=256, Ta=25℃, No Load

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		2.97	3.30	3.63	V
Input Voltage "High"	V_{IH}		2.7	-	-	V
Input Voltage "Low"	V_{IL}		-	-	0.6	V
Input Current "High"	I_{IH}	V_{CK}=3.3V	-	-	3.0	μA
Input Current "Low"	I_{IL}	V_{CK}=0V	-3.0	-	-	μA
Output Voltage "High"	V_{OH}	V_{DD}=2.97V, I_{OH}= - 8mA	2.5	-	-	V
Output Voltage "Low"	V_{OL}	V_{DD}=2.97V, I_{OL}=8mA	-	-	0.4	V
Supply Current 1	I_{DD1}	CE=0.3V	-	2.0	4.0	mA
Supply Current 2	I_{DD2}	CE=0V	-	-	5.0	μA
CE " High " Voltage	V_{CEH}		2.7	-	-	V
CE "Low" Voltage	V_{CEL}		-	-	0.45	V
CE Pull-Down Resistance 1	Rp1	CE=3.3V	0.5	1.5	2.5	MΩ
CE Pull-Down Resistance 2	Rp2	CE=0.3V	20.0	50.0	80.0	KΩ

● Electrical Characteristics (AC)
XC25BS51xxMR

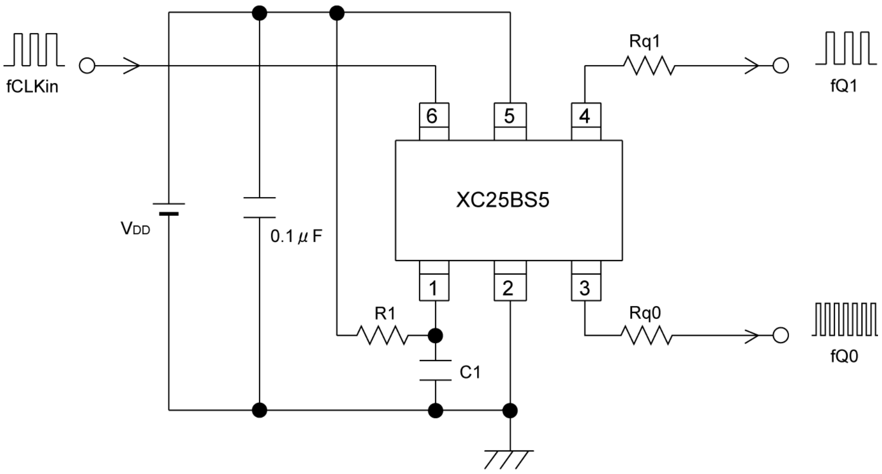
fCLKin=78kHz, Multiplier/Divider Ratio=256, Ta=25℃, CL=15pF

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time	T_{TLH}	V_{DD}=3.3V(20% to 80%) (*1)	-	5.0	-	Ns
Output Fall Time	T_{THL}	V_{DD}=3.3V(20% to 80%) (*1)	-	5.0	-	Ns
Duty Ratio	DUTY		40	50	60	%
Output Start Time	Ton	(*1)	-	-	20	ms
PLL Output Jitter	Tj	1σ (*1)	-	20	-	ps

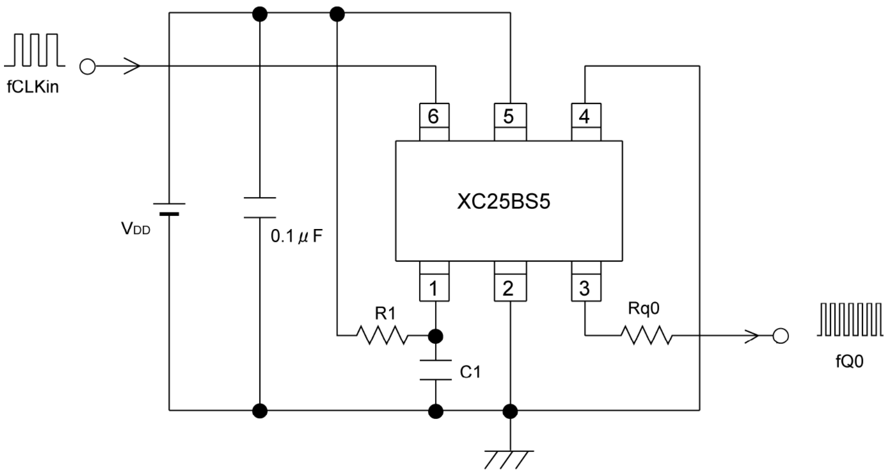
*1 R&D guarantee

■TYPICAL APPLICATION CIRCUITS

① Q1 Pin - reference oscillation, reference oscillation/2, comparative frequency



② Q1 Pin - GND

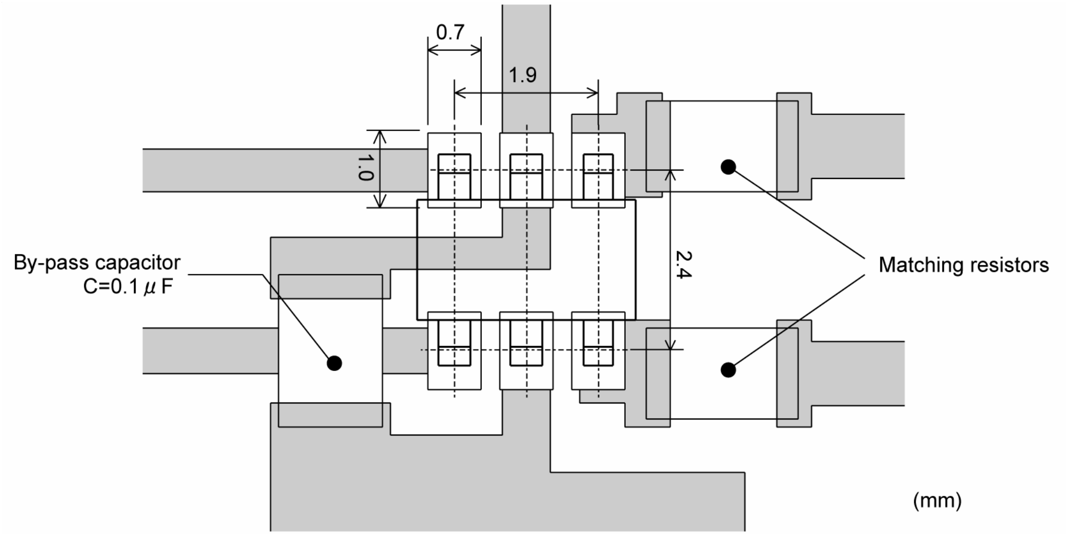


■NOTE

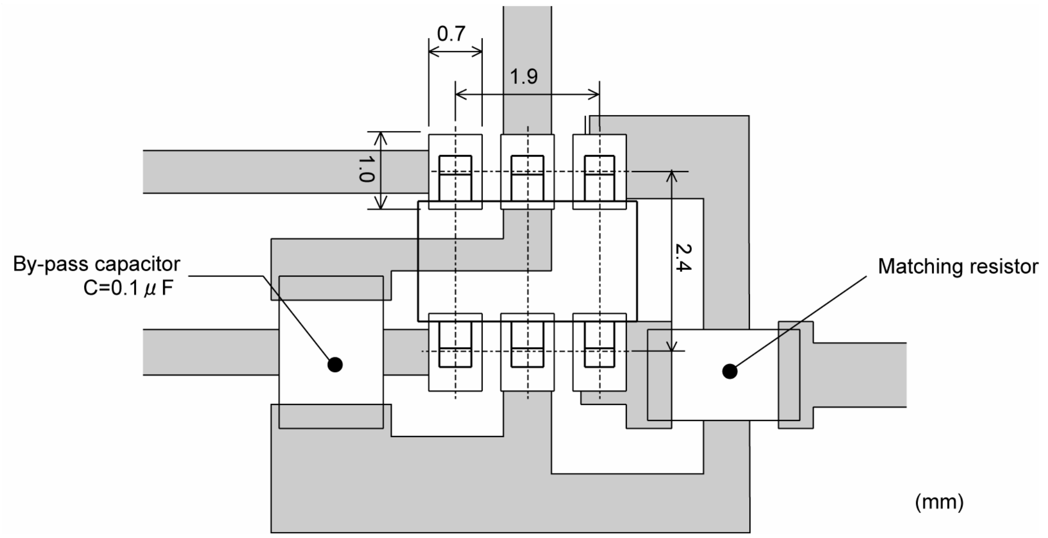
(1) Please insert a by-pass capacitor of 0.1μF.
(2) Rq0 and Rq1 are matching resistors. Their use is recommended in order to counter unwanted radiations.
(3) Please place a by-pass capacitor and matching resistors as close to the IC as possible. It may be that the output cannot be locked if the by-pass capacitor is not close enough to the IC. Further, there is a possibility of unwanted radiation occurrence between the resistor and the IC pin if the matching resistor is not close enough to the IC.
(4) When selecting GND for the Q1 pin, although the output of Q1 pin is GND level, it is also recommended that the Q1 pin be connected to GND pattern on the PCB.
(5) When the CE pin is not controlled by external signals, it is recommended that a time constant circuit of R1=1kΩ ×C1 = 0.1μF be added for stability.
(6) With this IC, output is achieved by dividing and multiplying the reference oscillation by means of the PLL circuit. In cases where this output is further used as a reference oscillation of another PLL circuit, it may be that the final output signal's jitter increases, so all necessary precautions should be taken to avoid this.
(7) It is recommended that a low noise power supply, such as a series regulator, be used for the supply voltage. Using a power supply such as a switching regulator might lead to a larger jitter, which in turn may lead to an inability to lock due to the ripple of the switching regulator.
(8) As for this IC, synchronization of input and output signal's edge is not guaranteed though the input frequency operates to the output frequency multiply.

■REFERENCE LAND PATTERN

① Q1 Pin - reference oscillation, reference oscillation/2, comparative frequency

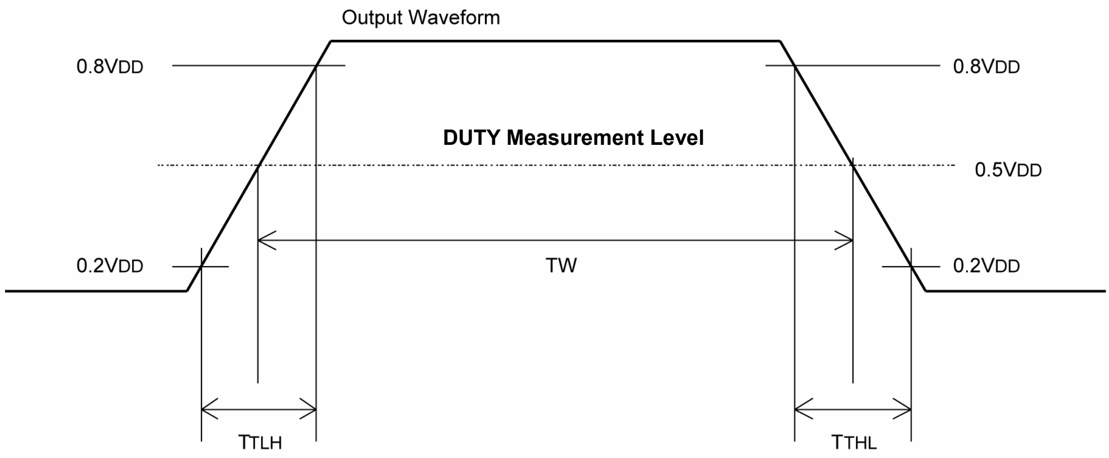


② Q1 Pin - GND

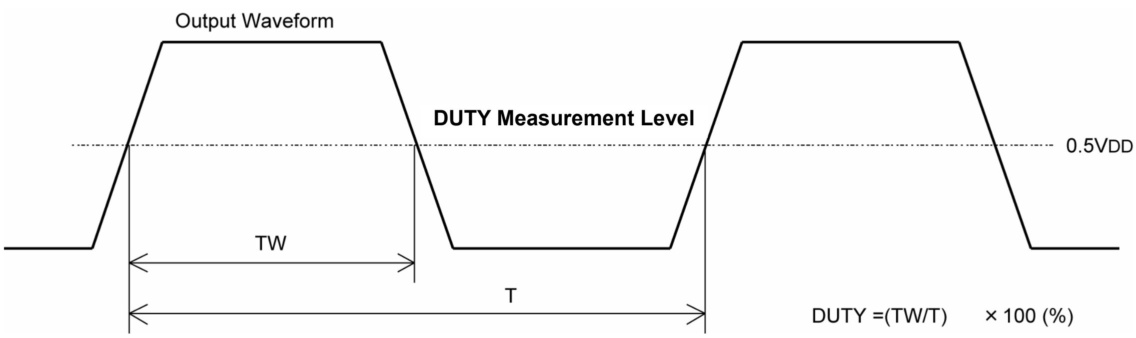


■AC CHARACTERISTIC WAVEFORMS

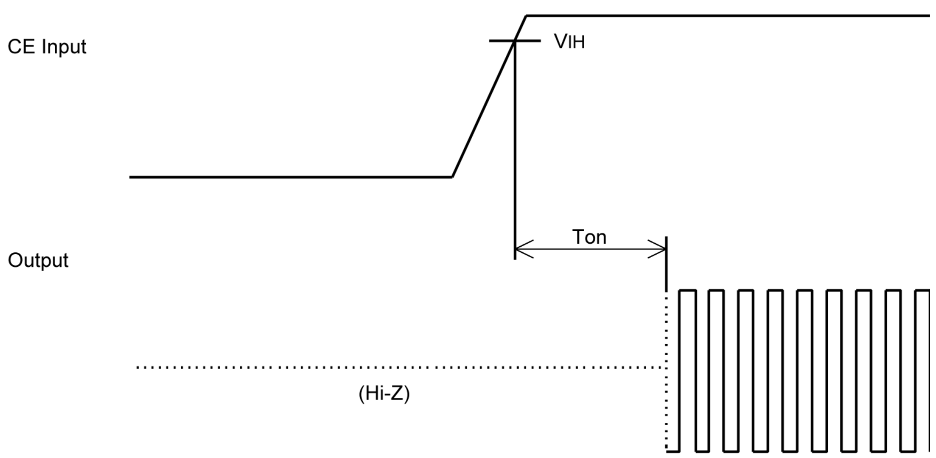
1) Output Rise Time / Output Fall Time



2) Duty Ratio



3) Output Start Time



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