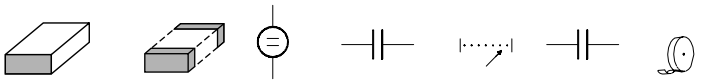
Multilayer ceramic capacitors

Chip capacitors, X8R

Date: October 2006

Ordering code system



B37541 K 5 102 K 0 60

Packaging

60 ≙ cardboard tape, 180-mm reel
62 ≙ blister tape, 180-mm reel
70 ≙ cardboard tape, 330-mm reel
72 ≙ blister tape, 330-mm reel

Internal coding

Capacitance tolerance

J ≙ ± 5%
K ≙ ± 10% (standard)
M ≙ ± 20%

Capacitance, coded (example)
102 ≙ 10 · 10^2 pF = 1 nF
103 ≙ 10 · 10^3 pF = 10 nF

Rated voltage

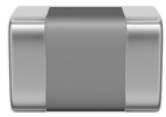
Rated voltage [VDC]	50
Code	5

Termination
Standard: K ≙ nickel barrier for all case sizes
On request: J ≙ silver-palladium for conductive adhesion for all case sizes

Type and size	
Chip size (**inch** / mm)	Temperature characteristic X8R
0603 / 1608 **0805** / 2012 **1206** / 3216 **1210** / 3225	B37540 B37541 B37472 B37550

X8R

SMD



Features

- Max. relative capacitance change up to 150 °C is ±15%
- Non-linear capacitance change
- High insulation resistance
- High pulse strength
- To AEC-Q200

Applications

- Automotive
- Blocking
- Coupling
- Decoupling
- Interference suppression

Termination

- For soldering: Nickel barrier terminations (Ni)

Options

- Alternative capacitance tolerances available on request

Delivery mode

- Cardboard and blister tape (blister tape for chip thickness ≥1.2 ±0.1 mm and case size 1210) 180-mm and 330-mm reel available

Electrical data

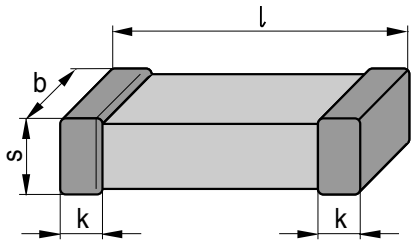
Temperature characteristic		X8R	
Max. relative capacitance change within –55 °C to +150 °C	$\Delta C/C$	±15	%
Climatic category (IEC 60068-1)		55/150/56	
Standard		EIA	
Dielectric		Class 2	
Rated voltage[1)]	V_R	50	VDC
Test voltage	V_{test}	$2.5 \cdot V_R$/5 s	VDC
Capacitance range / E series	C_R	100 pF … 150 nF (E6)	
Dissipation factor (limit value)	tan δ	$<25 \cdot 10^{-3}$	
Insulation resistance[2)] at + 25 °C	R_{ins}	$>10^5$	MΩ
Insulation resistance[2)] at +125 °C	R_{ins}	$>10^4$	MΩ
Time constant[2)] at + 25 °C	τ	>1000	s
Time constant[2)] at +125 °C	τ	>100	s
Operating temperature range	T_{op}	–55 … +150	°C
Ageing[3)]		yes	

1) Note: No operation on AC line.
2) For C_R >10 nF the time constant $\tau = C \cdot R_{ins}$ is given.
3) Refer to chapter “General technical information”, “Ageing”.

Capacitance tolerances

Code letter	J	K (standard)	M
Tolerance	±5%	±10%	±20%

Dimensional drawing



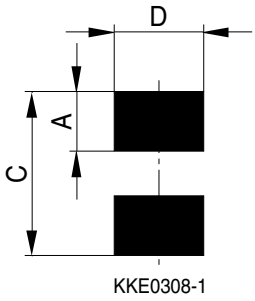
KKE0329-N

Dimensions (mm)

Case size (inch) (mm)	0603 1608	0805 2012	1206 3216	1210 3225
l	1.6 ±0.15	2.00 ±0.20	3.2 ±0.20	3.2 ±0.30
b	0.8 ±0.10	1.25 ±0.15	1.6 ±0.15	2.5 ±0.30
s	0.8 ±0.10	1.30 max.	1.30 max.	1.30 max.
k	0.1 –0.40	0.13 –0.75	0.25 –0.75	0.25 –0.75

Tolerances to CECC 32101-801

Recommended solder pad



KKE0308-1

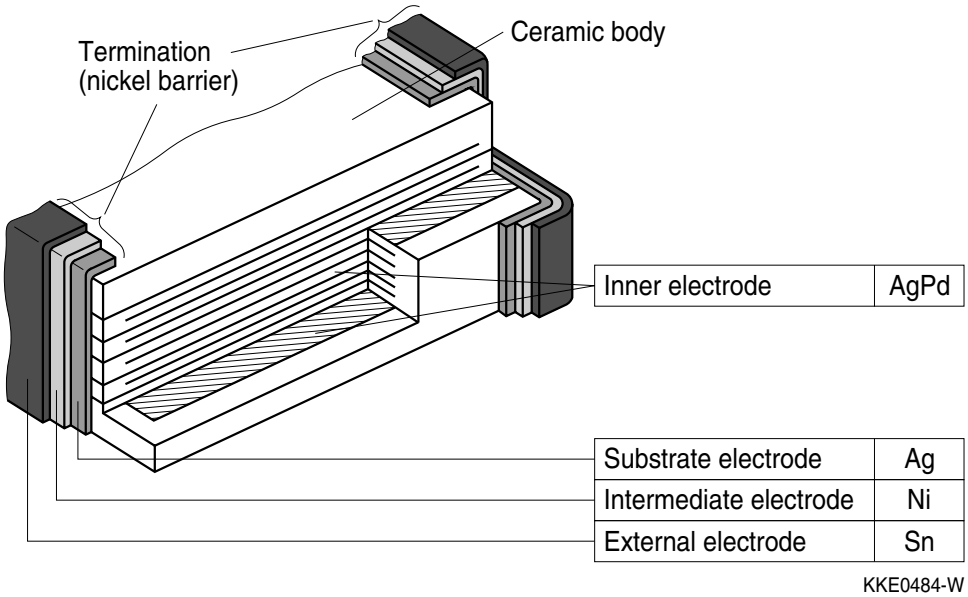
Recommended dimensions (mm) for reflow soldering

Case size	(inch/mm)	Type	A	C	D
	0603/1608	single chip	0.6 … 0.7	1.8 … 2.20	0.6 … 0.8
	0805/2012	single chip	0.6 … 0.7	2.2 … 2.60	0.8 … 1.1
	1206/3216	single chip	0.8 … 0.9	3.8 … 4.32	1.0 … 1.4
	1210/3225	single chip	1.0 … 1.2	4.0 … 4.80	1.8 … 2.3

Recommended dimensions (mm) for wave soldering

Case size	(inch/mm)	Type	A	C	D
	0603/1608	single chip	0.8 … 0.9	2.2 … 2.8	0.6 … 0.8
	0805/2012	single chip	0.9 … 1.0	2.8 … 3.2	0.8 … 1.1
	1206/3216	single chip	1.0 … 1.1	4.2 … 4.8	1.0 … 1.4

Termination



KKE0484-W

Product range chip capacitors, X8R

Size[1)] **inch** mm	**0603** 1608		**0805** 2012		**1206** 3216		**1210** 3225	
Type	B37540		B37541		B37472		B37550	
V_R (VDC) / C_R	50		50		50		50	
100 pF	■							
150 pF	■							
220 pF	■							
330 pF	■							
470 pF	■		■					
680 pF	■		■					
1.0 nF	■		■		■			
1.5 nF	■		■		■			
2.2 nF	■		■		■			
3.3 nF	■		■		■			
4.7 nF	■		■		■			
6.8 nF			■		■			
10 nF			■		■		■	
15 nF			■		■		■	
22 nF			■		■		■	
33 nF					■		■	
47 nF					■		■	
68 nF					■		■	
100 nF					■		■	
150 nF							■	

1) l × b (inch) / l × b (mm)

Ordering codes and packing for X8R, 50 VDC, nickel barrier terminations

C_R[1]	Ordering code[2]	Chip thickness mm	Cardboard tape, ∅ 180-mm reel ** ≙ 60 pcs/reel	Cardboard tape, ∅ 330-mm reel ** ≙ 70 pcs/reel
Case size 0603, 50 VDC				
100 pF	B37540K5101K0**	0.8 ± 0.1	4000	16000
150 pF	B37540K5151K0**	0.8 ± 0.1	4000	16000
220 pF	B37540K5221K0**	0.8 ± 0.1	4000	16000
330 pF	B37540K5331K0**	0.8 ± 0.1	4000	16000
470 pF	B37540K5471K0**	0.8 ± 0.1	4000	16000
680 pF	B37540K5681K0**	0.8 ± 0.1	4000	16000
1.0 nF	B37540K5102K0**	0.8 ± 0.1	4000	16000
1.5 nF	B37540K5152K0**	0.8 ± 0.1	4000	16000
2.2 nF	B37540K5222K0**	0.8 ± 0.1	4000	16000
3.3 nF	B37540K5332K0**	0.8 ± 0.1	4000	16000
4.7 nF	B37540K5472K0**	0.8 ± 0.1	4000	16000
Case size 0805, 50 VDC				
470 pF	B37541K5471K0**	0.6 ± 0.1	5000	20000
680 pF	B37541K5681K0**	0.6 ± 0.1	5000	20000
1.0 nF	B37541K5102K0**	0.6 ± 0.1	5000	20000
1.5 nF	B37541K5152K0**	0.6 ± 0.1	5000	20000
2.2 nF	B37541K5222K0**	0.6 ± 0.1	5000	20000
3.3 nF	B37541K5332K0**	0.6 ± 0.1	5000	20000
4.7 nF	B37541K5472K0**	0.6 ± 0.1	5000	20000
6.8 nF	B37541K5682K0**	0.6 ± 0.1	5000	20000
10 nF	B37541K5103K0**	0.6 ± 0.1	5000	20000
15 nF	B37541K5153K0**	0.6 ± 0.1	5000	20000
22 nF	B37541K5223K0**	0.6 ± 0.1	5000	20000

1) Other capacitance values on request.
2) The table contains the ordering codes for the standard capacitance tolerance. For other available capacitance tolerances see page 4.

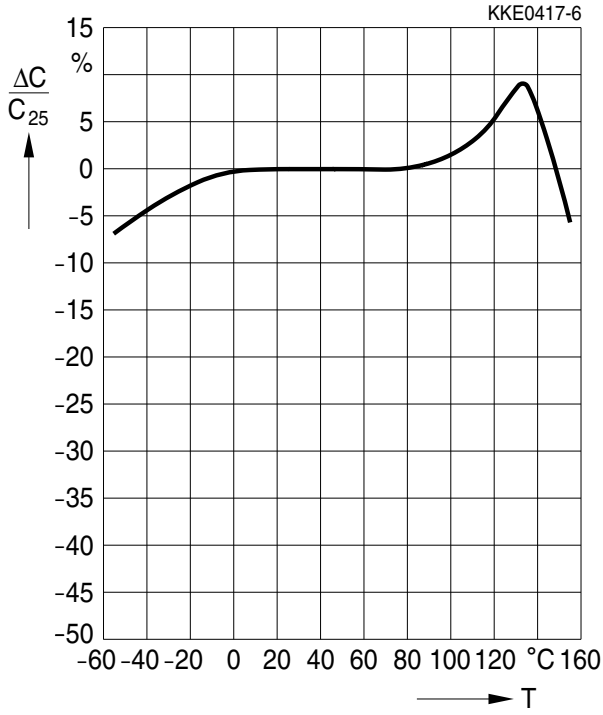
Ordering codes and packing for X8R, 50 VDC, nickel barrier terminations

C_R[1]	Ordering code[2]	Chip thickness mm	Cardboard tape, ∅ 180-mm reel ** ≙ 60 pcs/reel	Cardboard tape, ∅ 330-mm reel ** ≙ 70 pcs/reel
Case size 1206, 50 VDC				
1.0 nF	B37472K5102K0**	0.8 ± 0.1	4000	16000
1.5 nF	B37472K5152K0**	0.8 ± 0.1	4000	16000
2.2 nF	B37472K5222K0**	0.8 ± 0.1	4000	16000
3.3 nF	B37472K5332K0**	0.8 ± 0.1	4000	16000
4.7 nF	B37472K5472K0**	0.8 ± 0.1	4000	16000
6.8 nF	B37472K5682K0**	0.8 ± 0.1	4000	16000
10 nF	B37472K5103K0**	0.8 ± 0.1	4000	16000
15 nF	B37472K5153K0**	0.8 ± 0.1	4000	16000
22 nF	B37472K5223K0**	0.8 ± 0.1	4000	16000
33 nF	B37472K5333K0**	0.8 ± 0.1	4000	16000
47 nF	B37472K5473K0**	0.8 ± 0.1	4000	16000
68 nF	B37472K5683K0**	1.2 ± 0.1	3000[3]	12000[4]
100 nF	B37472K5104K0**	1.2 ± 0.1	3000[3]	12000[4]
			Blister tape, ∅ 180-mm reel ** ≙ 62 pcs/reel	Blister tape, ∅ 330-mm reel ** ≙ 72 pcs/reel
Case size 1210, 50 VDC				
10 nF	B37550K5103K0**	0.8 ± 0.1	4000	16000
15 nF	B37550K5153K0**	0.8 ± 0.1	4000	16000
22 nF	B37550K5223K0**	0.8 ± 0.1	4000	16000
33 nF	B37550K5333K0**	0.8 ± 0.1	4000	16000
47 nF	B37550K5473K0**	0.8 ± 0.1	4000	16000
68 nF	B37550K5683K0**	0.8 ± 0.1	4000	16000
100 nF	B37550K5104K0**	0.8 ± 0.1	4000	16000
150 nF	B37550K5154K0**	1.2 ± 0.1	3000	12000

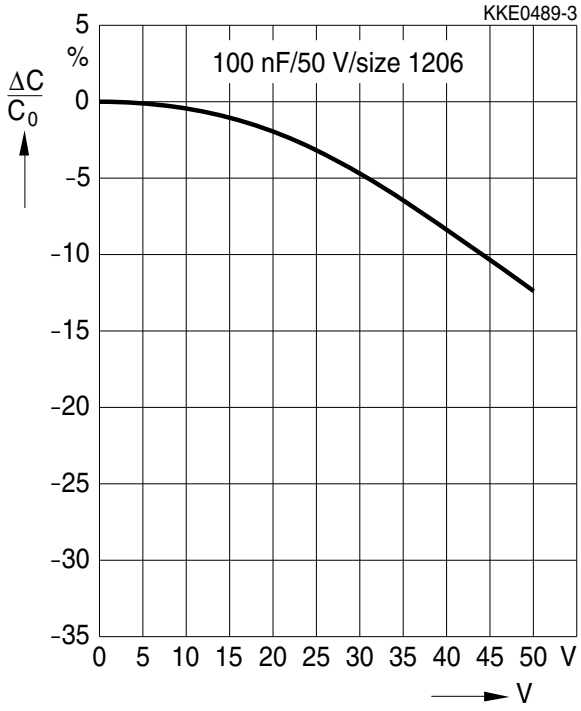
1) Other capacitance values on request.
2) The table contains the ordering codes for the standard capacitance tolerance. For other available capacitance tolerances see page 4.
3) Blister tape, 180-mm reel, ordering code ** ≙ 62
4) Blister tape, 330-mm reel, ordering code ** ≙ 72

Typical characteristics[1)]

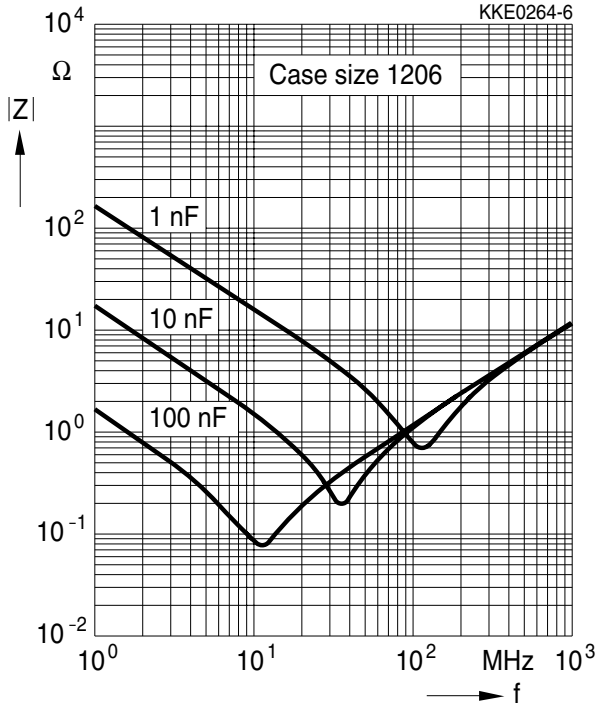
Capacitance change $\Delta C/C_{25}$ versus temperature T



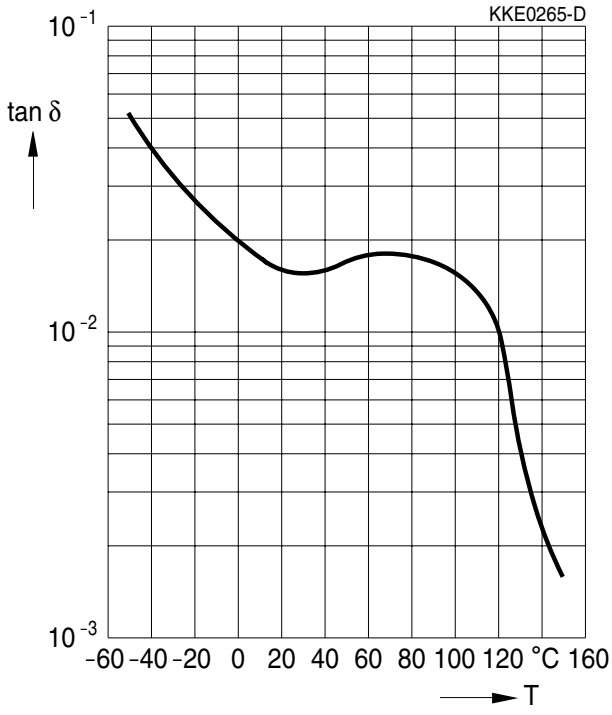
Capacitance change $\Delta C/C_0$ versus superimposed DC voltage V



Impedance |Z| versus frequency f



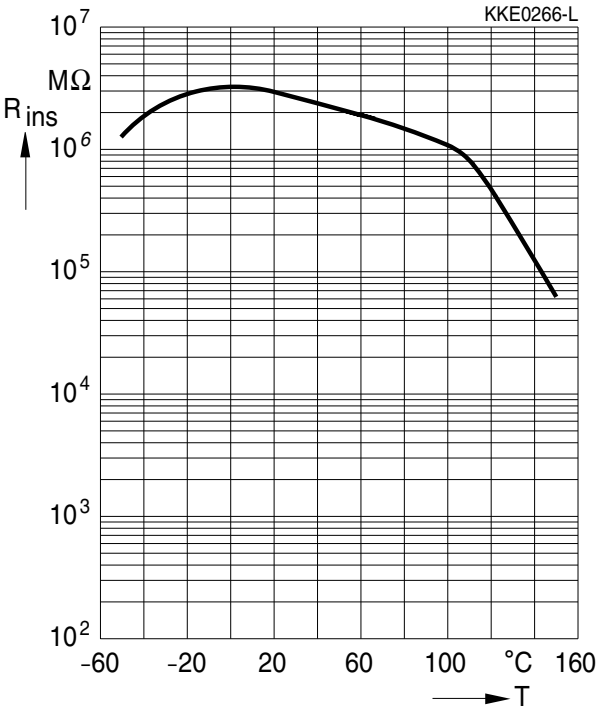
Dissipation factor tan δ versus temperature T



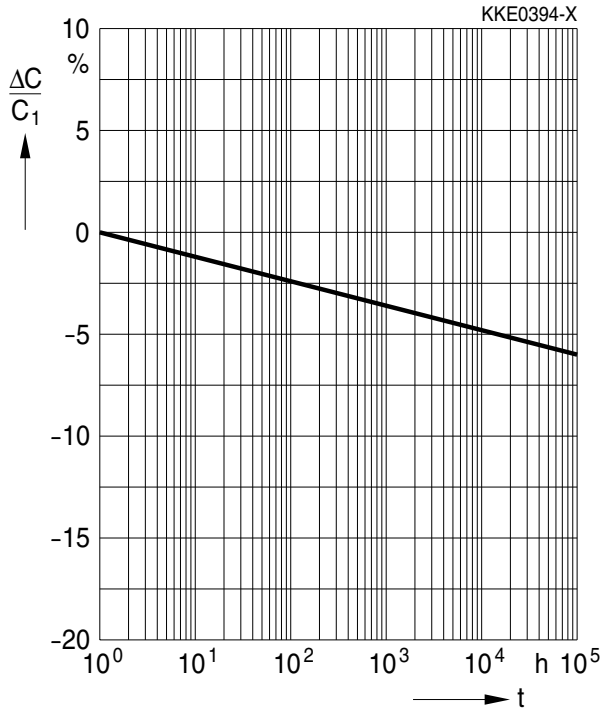
1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Typical characteristics[1)]

Insulation resistance R_{ins} versus temperature T



Capacitance change $\Delta C/C_1$ versus time t



1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Notes on the selection of ceramic capacitors

In the selection of ceramic capacitors, the following criteria must be considered:

1. Depending on the application, ceramic capacitors used to meet high quality requirements should at least satisfy the specifications to AEC-Q200. They must meet quality requirements going beyond this level in terms of ruggedness (e.g. mechanical, thermal or electrical) in the case of critical circuit configurations and applications (e.g. in safety-relevant applications such as ABS and airbag equipment or durable industrial goods).
2. At the connection to the battery or power supply (e.g. clamp 15 or 30 in the automobile) and at positions with stranding potential, to reduce the probability of short circuits following a fracture, two ceramic capacitors must be connected in series and/or a ceramic capacitor with integrated series circuit should be used. The MLSC from EPCOS contains such a series circuit in a single component.
3. Ceramic capacitors with the temperature characteristics Z5U and Y5V do not satisfy the requirements to AEC-Q200 and are mechanically and electrically less rugged than C0G or X7R/X8R ceramic capacitors. In applications that must satisfy high quality requirements, therefore, these capacitors should not be used as discrete components (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
4. For ESD protection, preference should be given to the use of multilayer varistors (MLV) (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
5. An application-specific derating or continuous operating voltage must be considered in order to cushion (unexpected) additional stresses (see the chapter “Reliability”).

The following should be considered in circuit board design

1. If technically feasible in the application, preference should be given to components having an optimal geometrical design.
2. At least FR4 circuit board material should be used.
3. Geometrically optimal circuit boards should be used, ideally those that cannot be deformed.
4. Ceramic capacitors must always be placed a sufficient minimum distance from the edge of the circuit board. High bending forces may be exerted there when the panels are separated and during further processing of the board (such as when incorporating it into a housing).
5. Ceramic capacitors should always be placed parallel to the possible bending axis of the circuit board.
6. No screw connections should be used to fix the board or to connect several boards. Components should not be placed near screw holes. If screw connections are unavoidable, they must be cushioned (for instance by rubber pads).

The following should be considered in the placement process

1. Ensure correct positioning of the ceramic capacitor on the solder pad.
2. Caution when using casting, injection-molded and molding compounds and cleaning agents, as these may damage the capacitor.
3. Support the circuit board and reduce the placement forces.
4. A board should not be straightened (manually) if it has been distorted by soldering.
5. Separate panels with a peripheral saw, or better with a milling head (no dicing or breaking).
6. Caution in the subsequent placement of heavy or leaded components (e.g. transformers or snap-in components): danger of bending and fracture.
7. When testing, transporting, packing or incorporating the board, avoid any deformation of the board not to damage the components.
8. Avoid the use of excessive force when plugging a connector into a device soldered onto the board.
9. Ceramic capacitors must be soldered only by the mode (reflow or wave soldering) permissible for them (see the chapter “Soldering directions”).
10. When soldering the most gentle solder profile feasible should be selected (heating time, peak temperature, cooling time) in order to avoid thermal stresses and damage.
11. Ensure the correct solder meniscus height and solder quantity.
12. Ensure correct dosing of the cement quantity.
13. Ceramic capacitors with an AgPd external termination are not suited for the lead-free solder process: they were developed only for conductive adhesion technology.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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