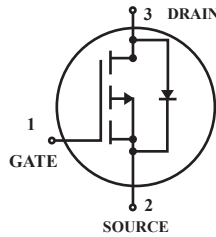


P-Channel Enhancement Mode Power MOSFET

(P/b) Lead(Pb)-Free

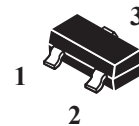


DRAIN CURRENT
-4.3 AMPERS

DRAIN SOURCE VOLTAGE
-12 VOLTAGE

Features:

- *Super High Dense Cell Design For Low $R_{DS(ON)}$
 $R_{DS(ON)} < 50m\Omega @ V_{GS}=10V$
- *Rugged and Reliable
- *Simple Drive Requirement
- *Fast Switching
- *1.8V Gate Rated
- *SOT-23 Package



SOT-23

Applications

- *Power Management in Notebook Computer
- *Portable Equipment
- *Battery Powered System

Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ³ , $V_{GS}@10V(T_A=25^\circ C)$ $V_{GS}@10V(T_A=70^\circ C)$	I_D	-4.3	A
		-3.4	
Pulsed Drain Current ¹	I_{DM}	-12	
Total Power Dissipation($T_A=25^\circ C$)	P_D	1.38	W
Maximum Junction-ambient ³	$R\theta_{JA}$	90	$^\circ C/W$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	$^\circ C$

Device Marking

WT6401=6401

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static

Drain-Source Breakdown Voltage $V_{GS}=0, I_D=-250\mu\text{A}$	BV_{DSS}	-12	-	-	V
Gate-Source Threshold Voltage $V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	$V_{GS(Th)}$	-	-	-1.0	
Gate-Source Leakage Current $V_{GS} = \pm 8\text{V}$	I_{GSS}	-	-	± 100	nA
Drain-Source Leakage Current ($T_j=25^\circ\text{C}$) $V_{DS}=-16\text{V}, V_{GS}=0$	I_{DSS}	-	-	-1	μA
Drain-Source Leakage Current ($T_j=70^\circ\text{C}$) $V_{DS}=-12\text{V}, V_{GS}=0$		-	-	-25	
Drain-Source On-Resistance ² $V_{GS}=-4.5\text{V}, I_D=-4.3\text{A}$ $V_{GS}=-2.5\text{V}, I_D=-2.5\text{A}$ $V_{GS}=-1.8\text{V}, I_D=-2.0\text{A}$	$R_{DS(on)}$	-	-	50 85 125	$\text{m}\Omega$
Forward Transconductance $V_{DS}=-5.0, I_D=-4.0\text{A}$	g_{fs}	-	12	-	S

Dynamic

Input Capacitance $V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1.0\text{MHz}$	C_{iss}	-	985	1580	pF
Output Capacitance $V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1.0\text{MHz}$	C_{oss}	-	180	-	
Reverse Transfer Capacitance $V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1.0\text{MHz}$	C_{rss}	-	160	-	

Switching

Turn-on Delay Time ² $V_{DS}=-10V, V_{GS}=-10V, I_D=-1A, R_D=10\Omega, R_G=3.3\Omega$	$t_d(\text{on})$	-	6	-	ns
Rise Time $V_{DS}=-10V, V_{GS}=-10V, I_D=-1A, R_D=10\Omega, R_G=3.3\Omega$	t_r	-	5	-	
Turn-off Delay Time $V_{DS}=-10V, V_{GS}=-10V, I_D=-1A, R_D=10\Omega, R_G=3.3\Omega$	$t_d(\text{off})$	-	16	-	
Fall Time $V_{DS}=-10V, V_{GS}=-10V, I_D=-1A, R_D=10\Omega, R_G=3.3\Omega$	t_f	-	3	-	
Total Gate Charge ² $V_{DS}=-12V, V_{GS}=-4.5V, I_D=-4.0A$	Q_g	-	15	24	nC
Gate-Source Charge $V_{DS}=-12V, V_{GS}=-4.5V, I_D=-4.0A$	Q_{gs}	-	1.3	-	
Gate-Source Change $V_{DS}=-12V, V_{GS}=-4.5V, I_D=-4.0A$	Q_{gd}	-	4	-	

Source-Drain Diode Characteristics

Forward On Voltage ² $V_{GS}=0V, I_S=-1.2A$	V_{SD}	-	-	1.2	V
Reverse Recovery Time ² $V_{GS}=0V, I_S=-4.0A, di/dt=100A/\mu s$	T_{rr}	-	25	-	ns
Reverse Recovery Charge $V_{GS}=0V, I_S=-4.0A, di/dt=100A/\mu s$	Q_{rr}	-	26	-	nC

- Note: 1. Pulse width limited by max, junction temperature.
 2. pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 3. Surface mounted on 1 in² copper pad of FR4 board; 270°C/W when mounted on min, copper pad.

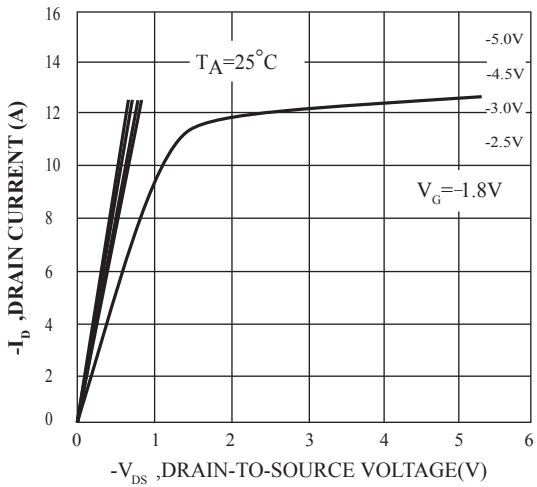


FIG.1 Typical Output Characteristics

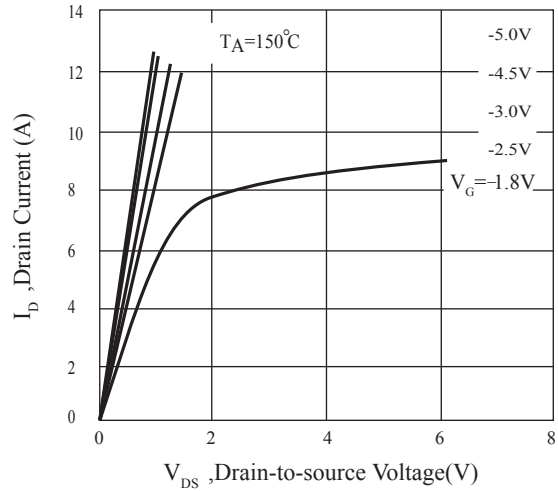


Fig.2 Typical Output Characteristics

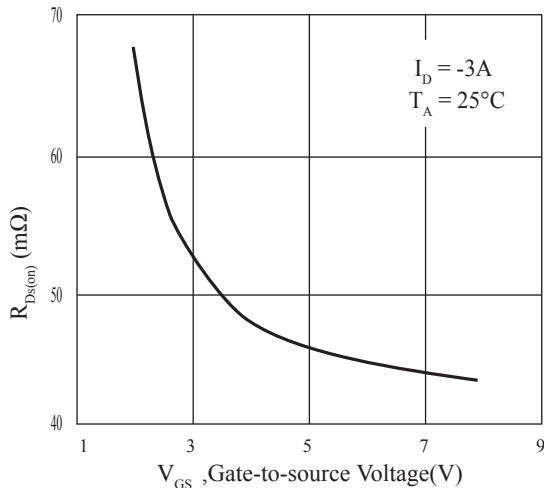


Fig.3 On-Resistance v.s. Gate Voltage

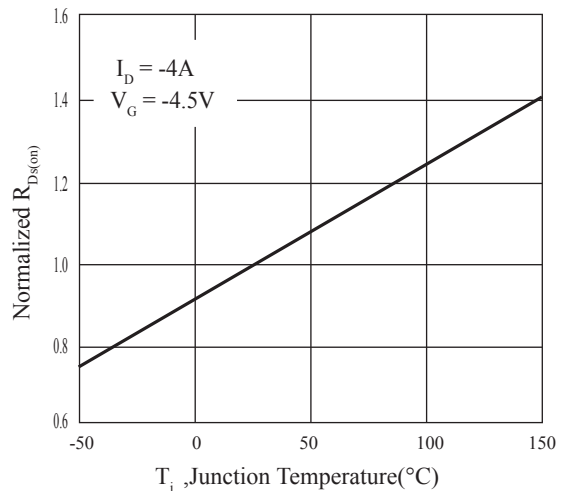


Fig.4 Normalized OnResistance

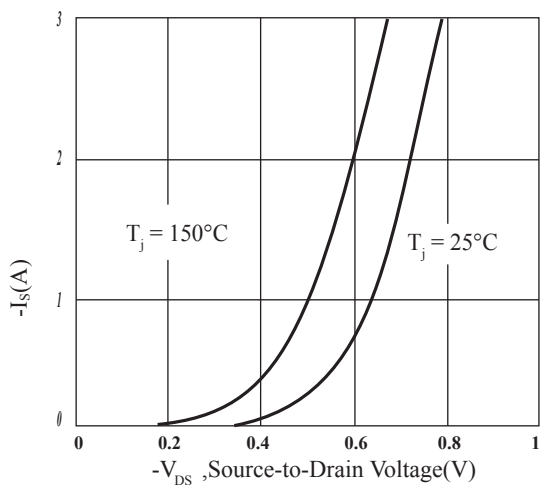


Fig.5 Forward Characteristics of Reverse Diode

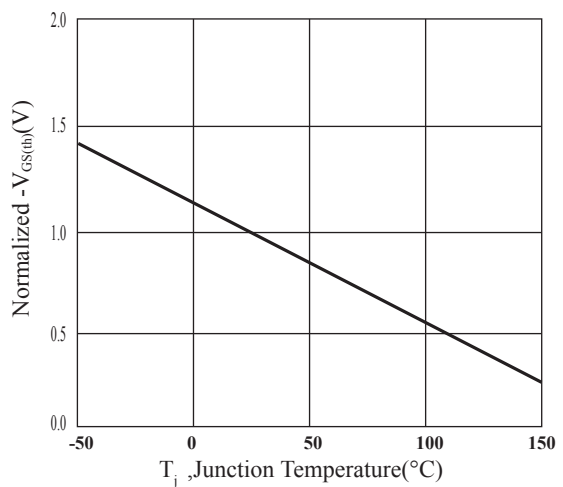


Fig.6 Gate Threshold Voltage v.s. Junction Temperature

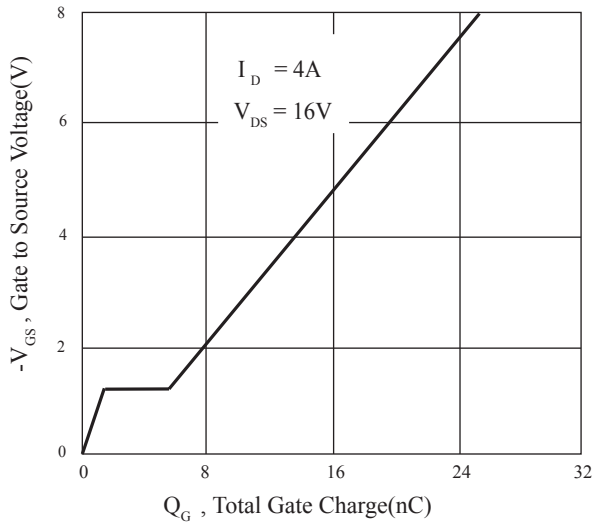


Fig 7. Gate Charge Characteristics

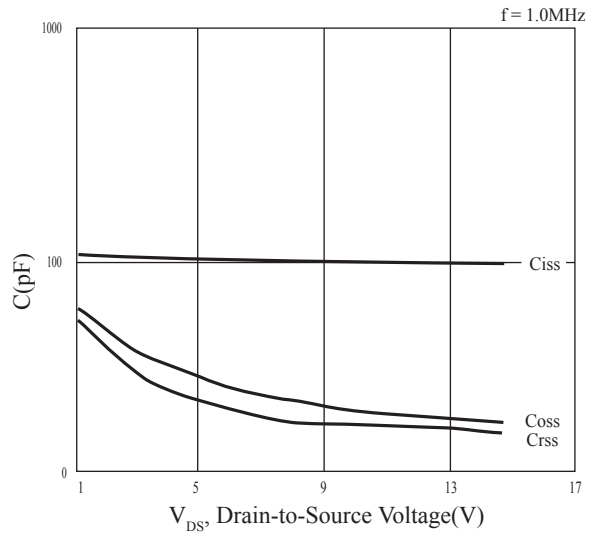


Fig 8. Typical Capacitance Characteristics

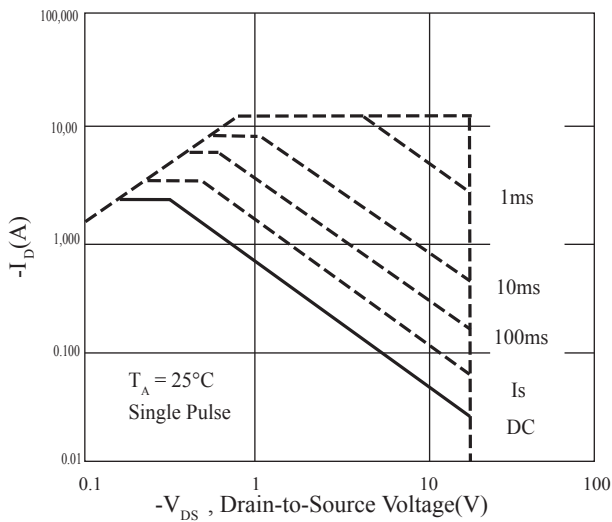


Fig 9. Maximum Safe Operation Area

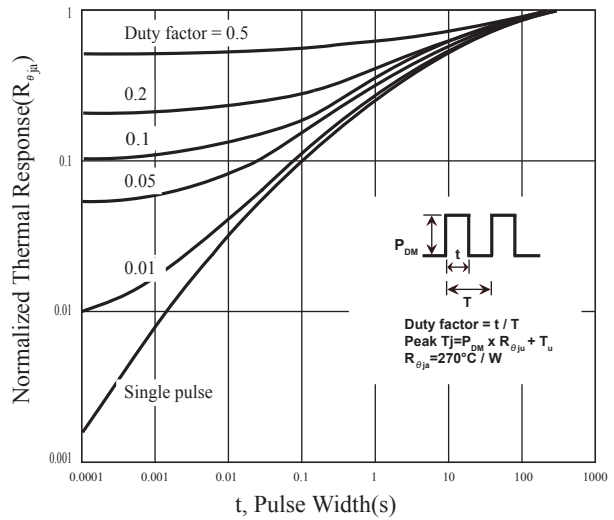


Fig 10. Effective Transient Thermal Impedance

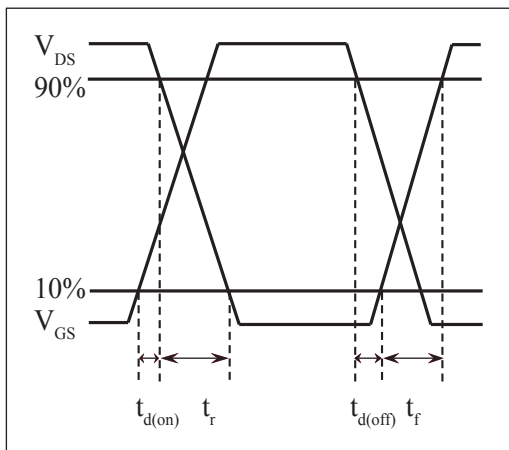


Fig 11. Switching Time Circuit

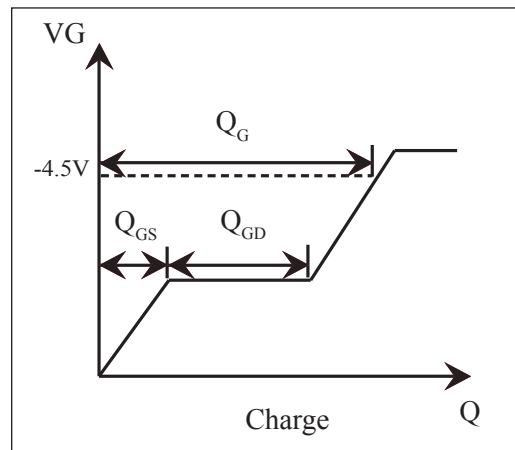


Fig 12. Gate Charge Waveform

SOT-23 Outline Dimension

