



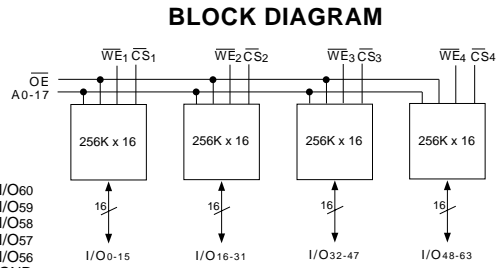
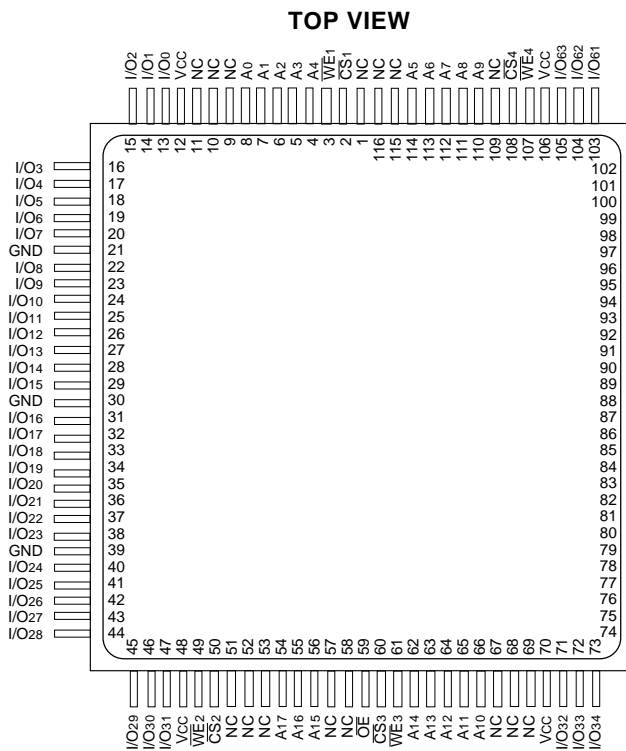
256Kx64 SRAM MODULE *ADVANCED**

FEATURES

- Access Times 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging:
 - 116 lead, 40mm, Hermetic CQFP (Package 504)
- Organized as 256Kx64, User Configurable as 512Kx32 or 1Mx16.
- Data I/O Compatible with 3.3V devices
- 2V Data Retention devices available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Weight
WS256K64-XG4WX - 20 grams typical

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION FOR WS256K64-XG4WX



PIN DESCRIPTION

I/O0-63	Data Inputs/Outputs
A0-17	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} + 0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Output Enable Capacitance	C _{OE}	V _{IN} = 0V, f = 1.0MHz	50	pF
Write Enable Capacitance	C _{WE}	V _{IN} = 0V, f = 1.0MHz	20	pF
Chip Select Capacitance	C _{CS}	V _{IN} = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	C _{I/O}	V _{IN} = 0V, f = 1.0MHz	20	pF
Address Input Capacitance	C _{AD}	V _{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

DC CHARACTERISTICS(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Units	
			Min	Max
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10 μA
Output Leakage Current	I _{LO}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$		10 μA
Operating Supply Current	I _{CC}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		920 mA
Standby Current	I _{SB}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		68 mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4 V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4	V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V



AC CHARACTERISTICS (VCC = 5.0V, GND = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	20		25		35		ns
Address Access Time	t _{AA}		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		20		25		35	ns
Output Enable to Output Valid	t _{OE}		12		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12		15		15	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		15		15	ns

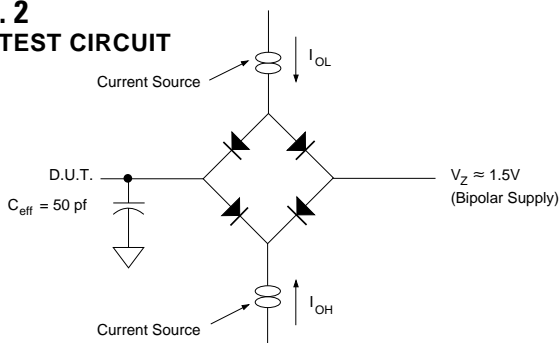
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS (VCC = 5.0V, GND = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	20		25		35		ns
Chip Select to End of Write	t _{CW}	17		20		25		ns
Address Valid to End of Write	t _{AW}	17		20		25		ns
Data Valid to End of Write	t _{DW}	12		15		20		ns
Write Pulse Width	t _{WP}	17		20		25		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	2		2		2		ns
Output Active from End of Write	t _{OW} ¹	0		0		0		ns
Write Enable to Output in High Z	t _{WHZ} ¹		10		10		15	ns
Data Hold Time	t _{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



FIG. 3
TIMING WAVEFORM - READ CYCLE

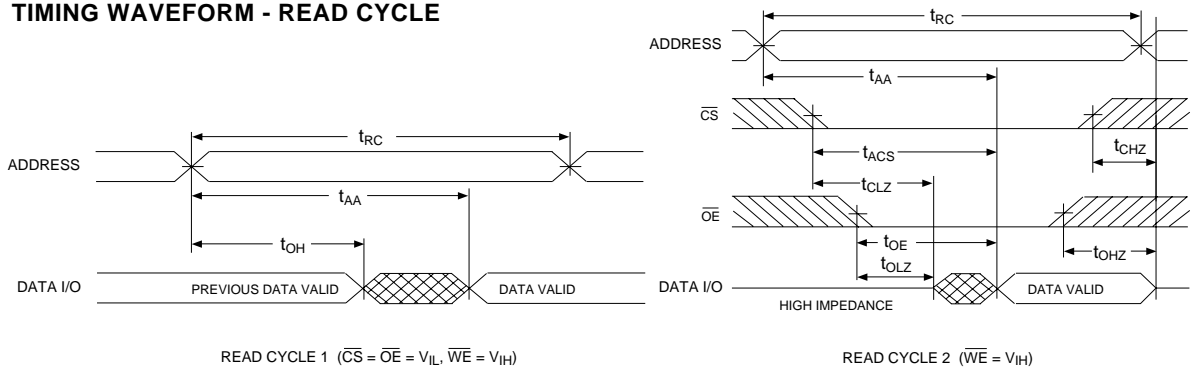


FIG. 4
WRITE CYCLE - \overline{WE} CONTROLLED

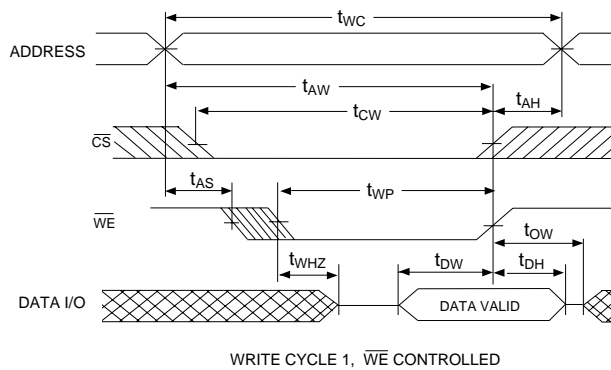
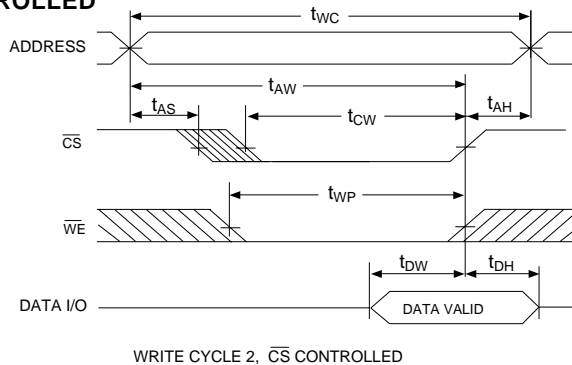
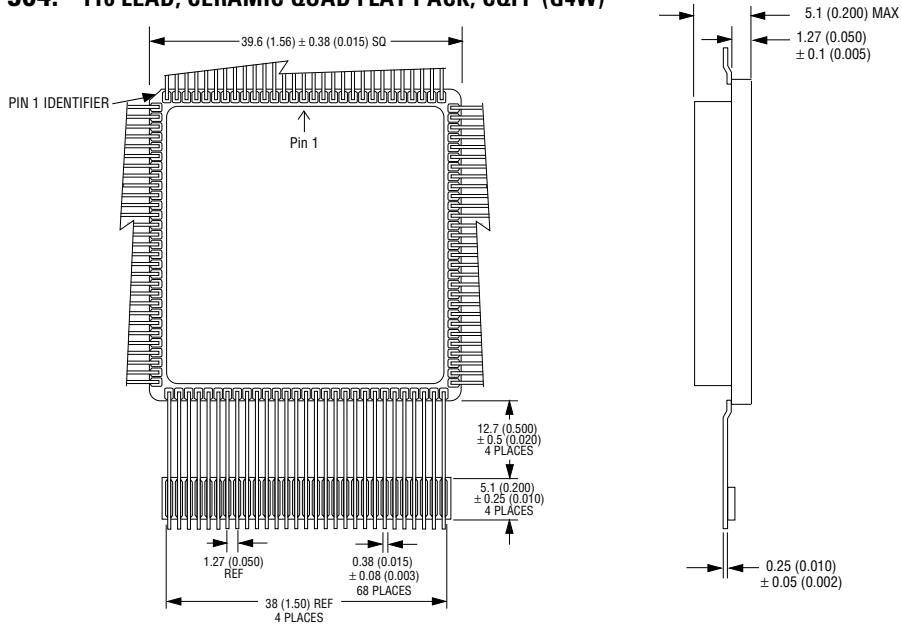


FIG. 5
WRITE CYCLE - \overline{CS} CONTROLLED





PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 256K64 - XXX G4W X

DEVICE GRADE:

- M = Military Screened -55°C to $+125^{\circ}\text{C}$
- I = Industrial -40°C to $+85^{\circ}\text{C}$
- C = Commercial 0°C to $+70^{\circ}\text{C}$

PACKAGE:

G4W = 116 Lead 40mm Ceramic Quad Flat Pack, CQFP (Package 504)

ACCESS TIME (ns)

ORGANIZATION, 256K x 64

User configurable as 1M x 16 or 512K x 32

SRAM

WHITE MICROELECTRONICS