1Mx32 SRAM MODULE

FEATURES

- Access Times of 17, 20, 25ns
- Packaging
  - 84 lead, 28mm CQFP, (Package 511)
  - 66 pin PGA Type, 1.385" sq., Hermetic Ceramic HIP (Package 402)*
- Organized as two banks of 512Kx32, User Configurable as 2Mx16 or 4Mx8

** Package to be developed.*

- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS1M32-XH2X* - 13 grams (typical)
  WS1M32-XG3X - 20 grams (typical)

PIN CONFIGURATION FOR WS1M32-XH2X*

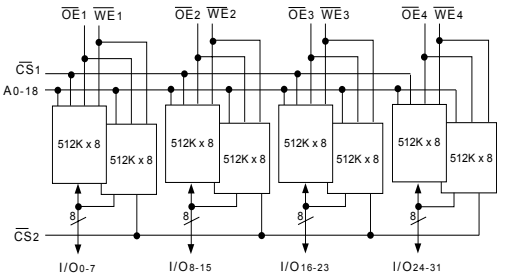
TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{WE}_2$	I/O15		I/O24	VCC	I/O31
I/O9	$\overline{OE}_2$	I/O14		I/O25	$\overline{OE}_4$	I/O30
I/O10	GND	I/O13		I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12		A6	I/O27	I/O28
A14	A10	$\overline{OE}_1$		A7	A3	A0
A15	A11	A18		$\overline{CS}_2$	A4	A1
A16	A12	$\overline{WE}_1$		A8	A5	A2
A17	VCC	I/O7		A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6		I/O16	$\overline{OE}_3$	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-18}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-2}$	Chip Selects
$\overline{OE}_{1-4}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

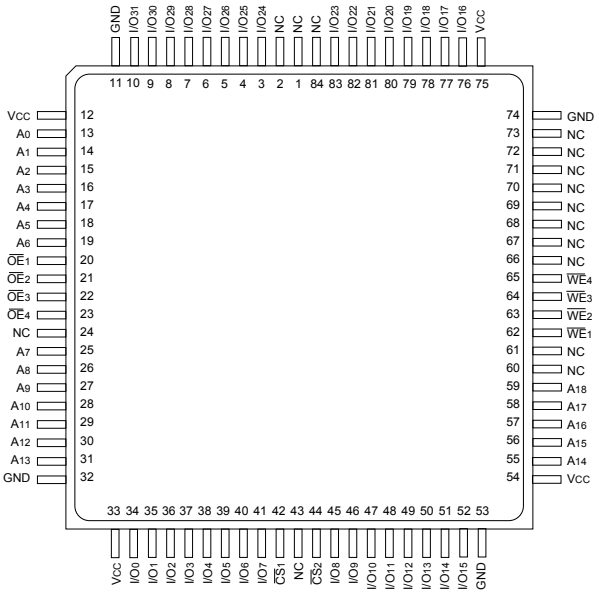
BLOCK DIAGRAM

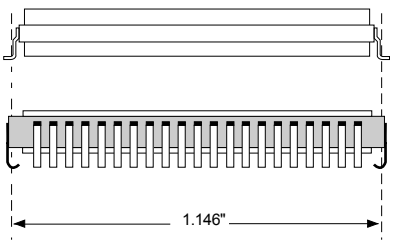


NOTE: $\overline{CS}_1$ & $\overline{CS}_2$ are used as bank select

PIN CONFIGURATION FOR WS1M32-XG3X

TOP VIEW





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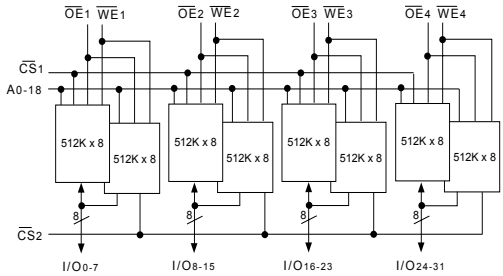


NOTE: $\overline{CS}_1$ & $\overline{CS}_2$ are used as bank select

The WEDC 84 lead G3 CQFP fills the same fit and function as the JEDEC 84 lead CQFJ or 84 PLCC. But the G3 has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc + 0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C
Operating Temp (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A=+25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}_{1\text{-}4}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
$\overline{WE}_{1\text{-}4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
$\overline{CS}_{1\text{-}2}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	30	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	75	pF

This parameter is guaranteed by design but not tested.

TRUTH TABLE

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	H	X	X	Standby	High Z	Standby
L	H	L	H	Read	Data Out	Active
L	H	H	H	Out Disable	High Z	Active
L	H	X	L	Write	Data In	Active
H	L	L	H	Read	Data Out	Active
H	L	H	H	Out Disable	High Z	Active
H	L	X	L	Write	Data In	Active
L	L	X	X	Invalid State	Invalid State	Invalid State

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		720	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		120	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, Vcc = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS
(V_{CC}=5.0V, GND=0V, T_A=-55°C to +125°C)

Parameter Read Cycle	Symbol	-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		ns
Address Access Time	t_{AA}		17		20		25	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		17		20		25	ns
Output Enable to Output Valid	t_{OE}		10		10		12	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		12		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		12		12	ns

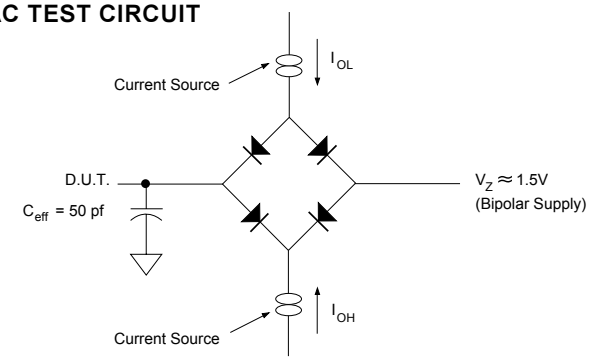
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC}=5.0V, GND=0V, T_A=-55°C to +125°C)

Parameter Write Cycle	Symbol	-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		ns
Chip Select to End of Write	t_{CW}	15		15		17		ns
Address Valid to End of Write	t_{AW}	15		15		17		ns
Data Valid to End of Write	t_{DW}	11		12		13		ns
Write Pulse Width	t_{WP}	15		15		17		ns
Address Setup Time	t_{AS}	2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	2		3		4		ns
Write Enable to Output in High Z	t_{WHZ}[1]		9		11		13	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

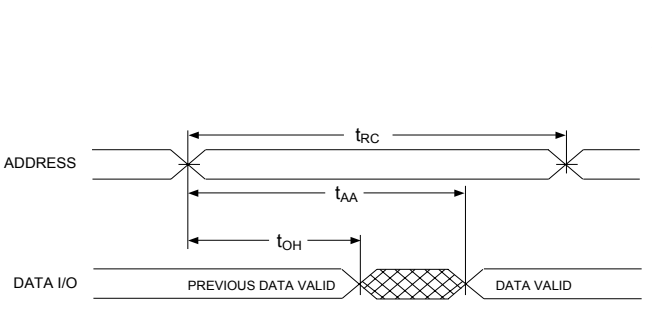


AC TEST CONDITIONS

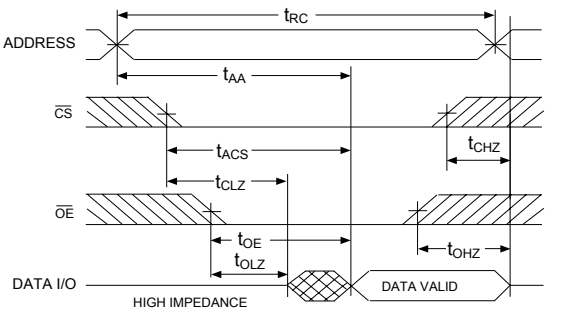
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z0 = 75\Omega$.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

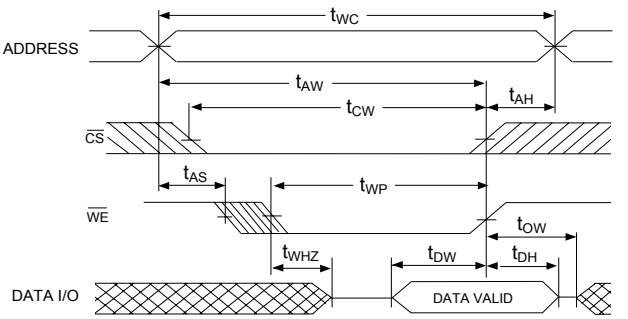


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



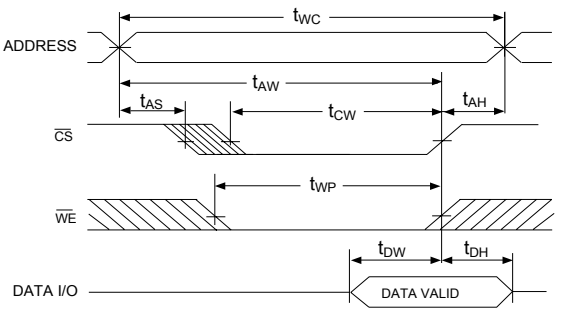
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



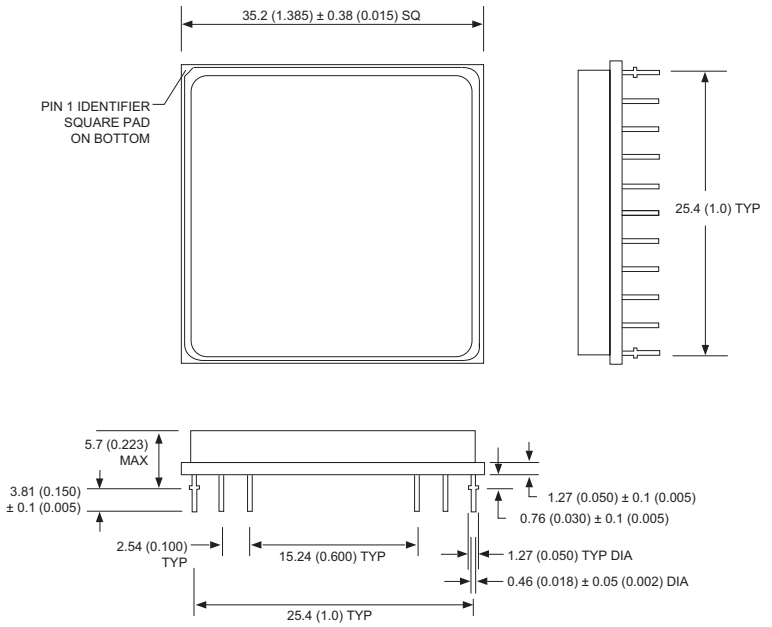
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



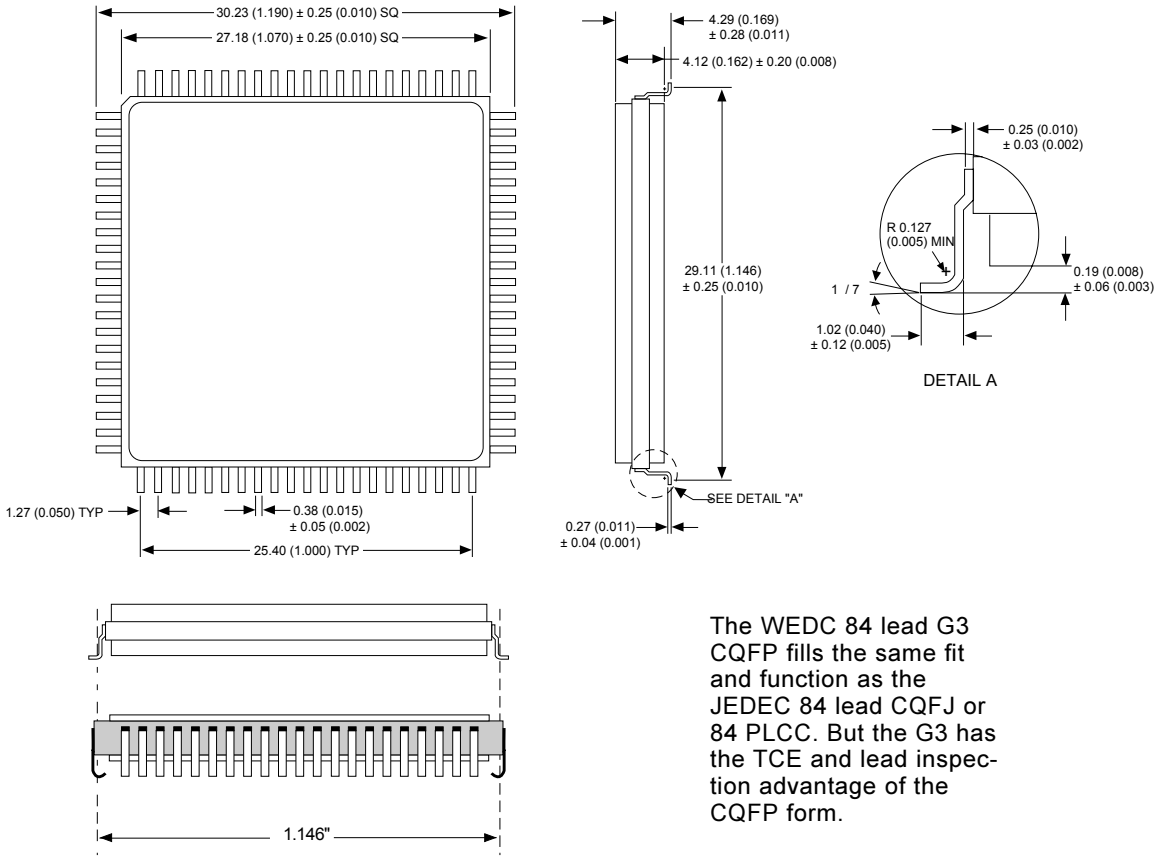
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 511: 84 LEAD, CERAMIC QUAD FLAT PACK (G3)



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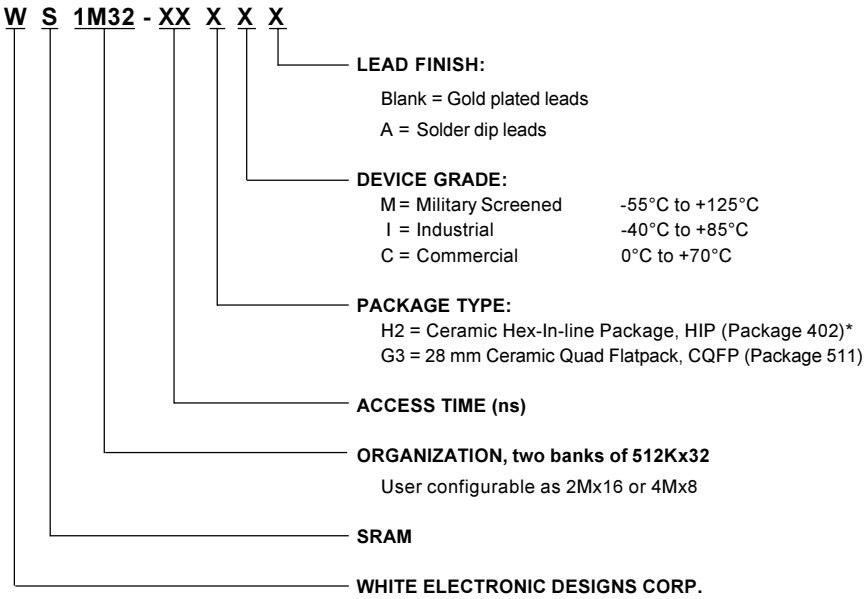
ORDERING INFORMATION



** Package to be developed.*