



32K x 8 Static RAM

Features

- **Low voltage range:**
— 2.7V – 3.6V
- **Low active power and standby power**
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

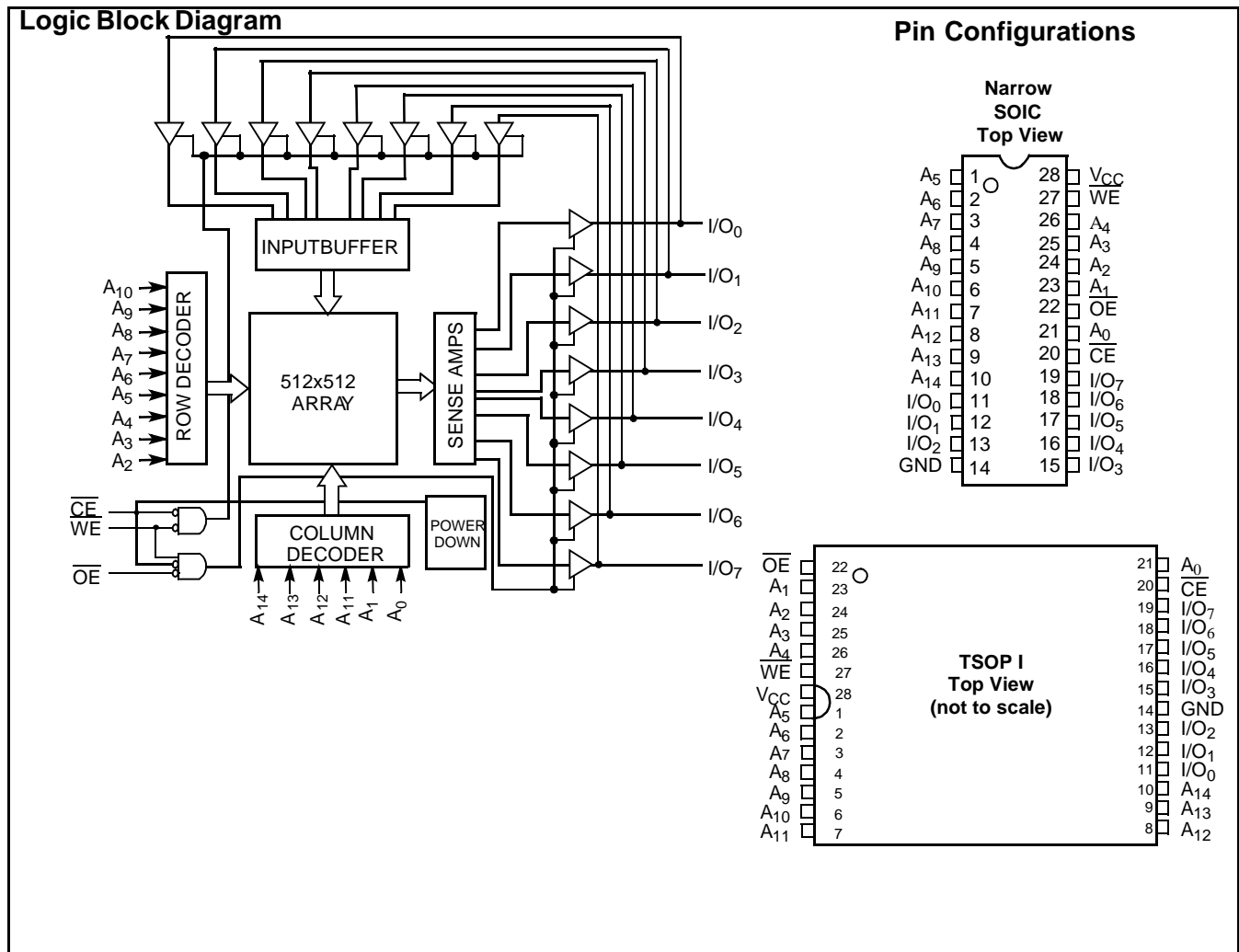
Functional Description

The WCMS0808U1X is composed of a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and three-state drivers. These devices have an automatic power-down feature,

reducing the power consumption by over 99% when deselected. The WCMS0808U1X is available in the 450-mil-wide (300-mil body width) narrow SOIC and TSOP.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... 0°C to +70°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State^[1]..... -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1]..... -0.5V to V_{CC} + 0.5V
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (LL Devices)			
	Min.	Typ.	Max.		Operating (I _{CC})		Standby (I _{SB2})	
					Typ.	Max.	Typ.	Max.
WCMS0808U1X	2.7V	3.0	3.6V	70 ns	11 mA	30 mA	0.1 μA	40 μA

Electrical Characteristics Over the Operating Range

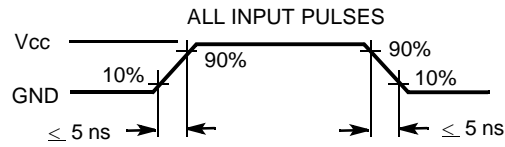
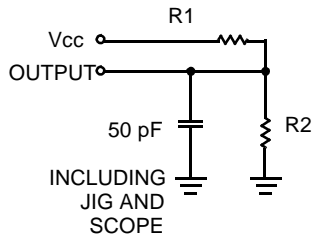
Parameter	Description	Test Conditions	WCMS0808U1X			Unit
			Min.	Typ. ^[1]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} +0.3V	V
V _{IL}	Input LOW Voltage		-0.5		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = 3.6V, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Ind'l	11	30	mA
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Ind'l	100	300	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Ind'l	0.1	40	μA

Capacitance^[3]

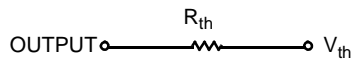
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C, and t_{AA} = 70ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


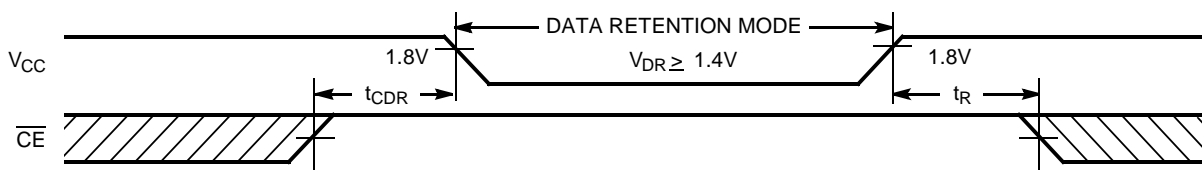
Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.3 V	Unit
R1	1103	KOhms
R2	1554	KOhms
RTH	645	KOhms
VTH	1.75V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[4]	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.4			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.6$ $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		0.1	6	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[3]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform


Switching Characteristics Over the Operating Range^[5]

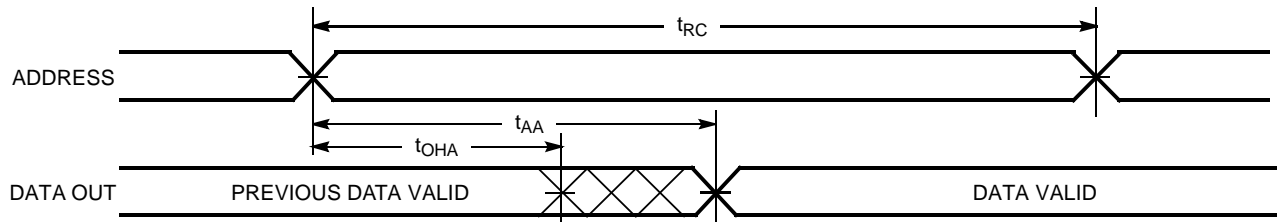
Parameter	Description	WCMS0808U1X		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[6]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		70	ns
WRITE CYCLE^[8,9]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE} LOW to Write End	60		ns
t _{AW}	Address Set-Up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	50		ns
t _{SD}	Data Set-Up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	10		ns

Notes:

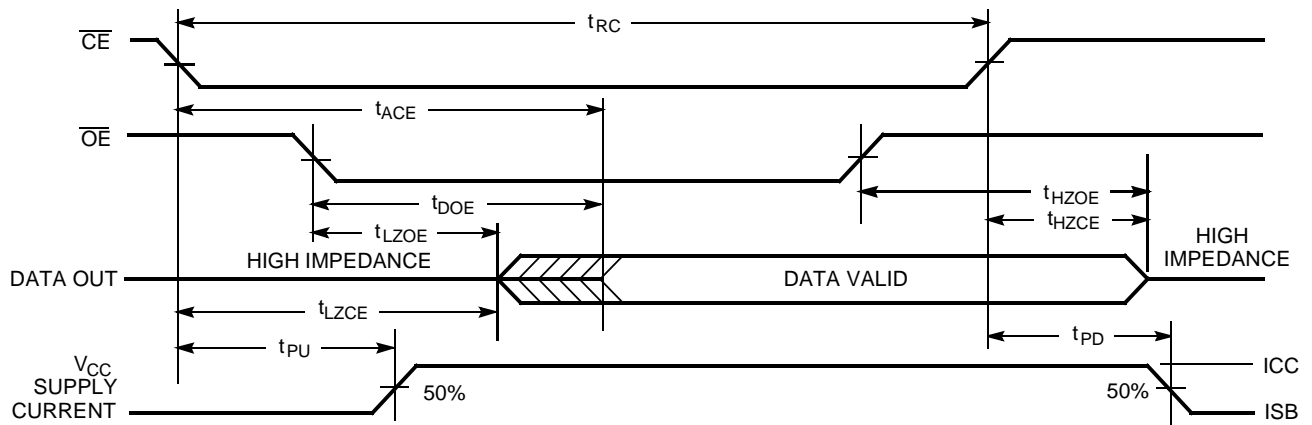
4. No input may exceed $V_{CC}+0.3V$.
5. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC} , and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Read Cycle No. 1^[10, 11]



Read Cycle No. 2^[11, 12]

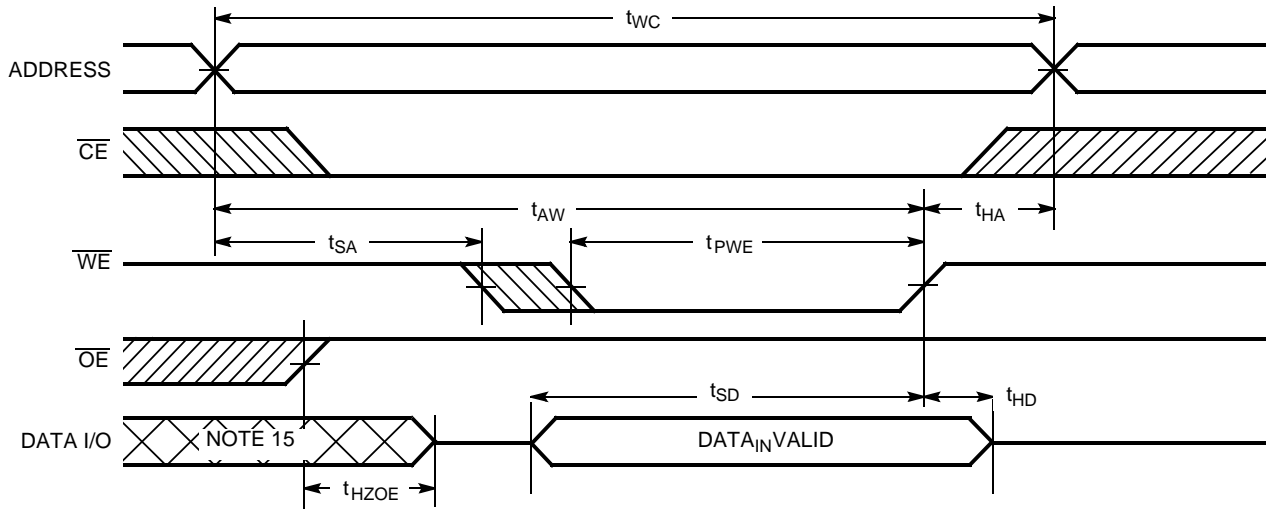


Notes:

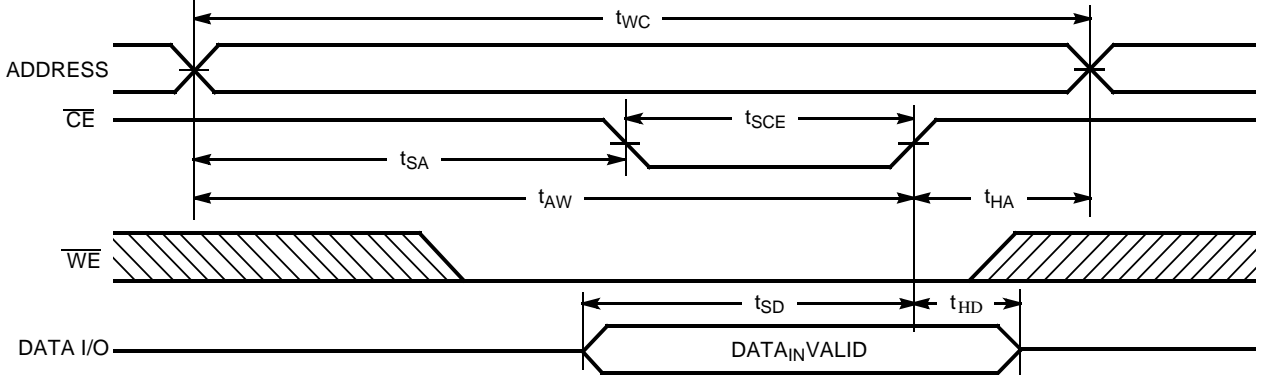
- 10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 11. \overline{WE} is HIGH for read cycle.
- 12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{WE} Controlled) [8, 13, 14]

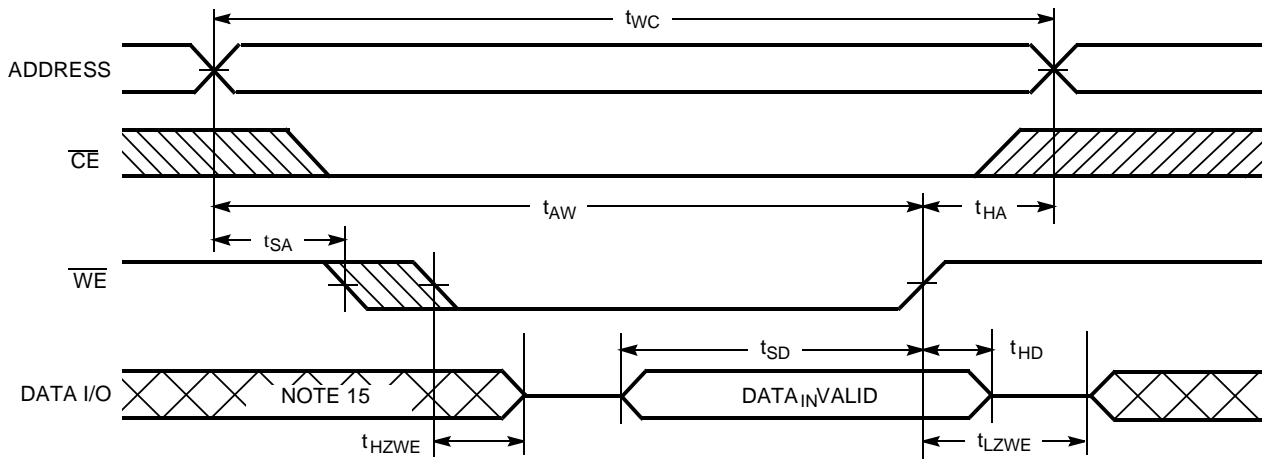


Write Cycle No. 2 (\overline{CE} Controlled) [8, 13, 14]



Notes:

- 13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 (WE Controlled, OE LOW)^[9, 14]

Truth Table

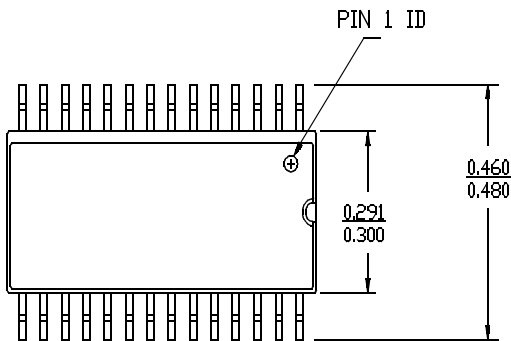
CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

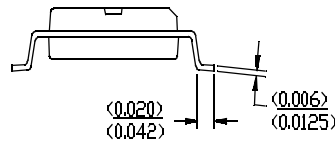
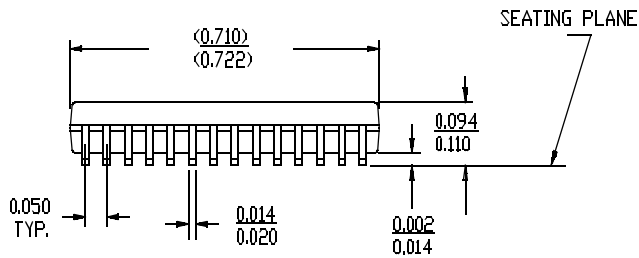
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMS0808U1X -NF70	N28	28-Lead 450-Mil (300-Mil Body Width) narrow SOIC	Industrial
	WCMS0808U1X-TF70	T28	28-Lead Thin Small Outline Package	

Package Diagrams

28-Lead 450-Mil (300-Mil Body Width) SOIC, N28



DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.

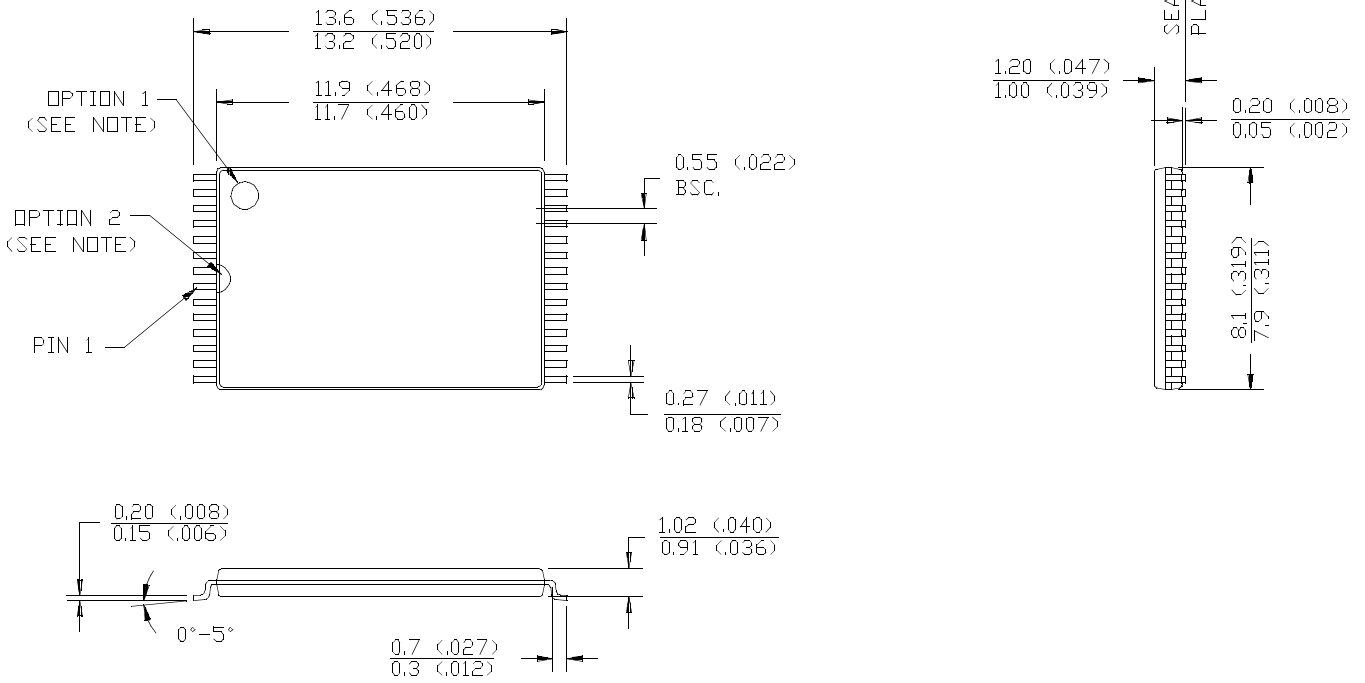


Package Diagrams (continued)

28-Lead Thin Small Outline Package, T28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)
MAX.
MIN.





Document Title: WCMS0808U1X, 32K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14009	115224	1/17/02	MGN	New Datasheet