



32Kx8 Static RAM

Features

- **Low Voltage Range**
— 4.5V–5.5V Operation
- **Low active power**
— 275 mW (max.)
- **Low standby power**
— 28 μ W (max.)
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

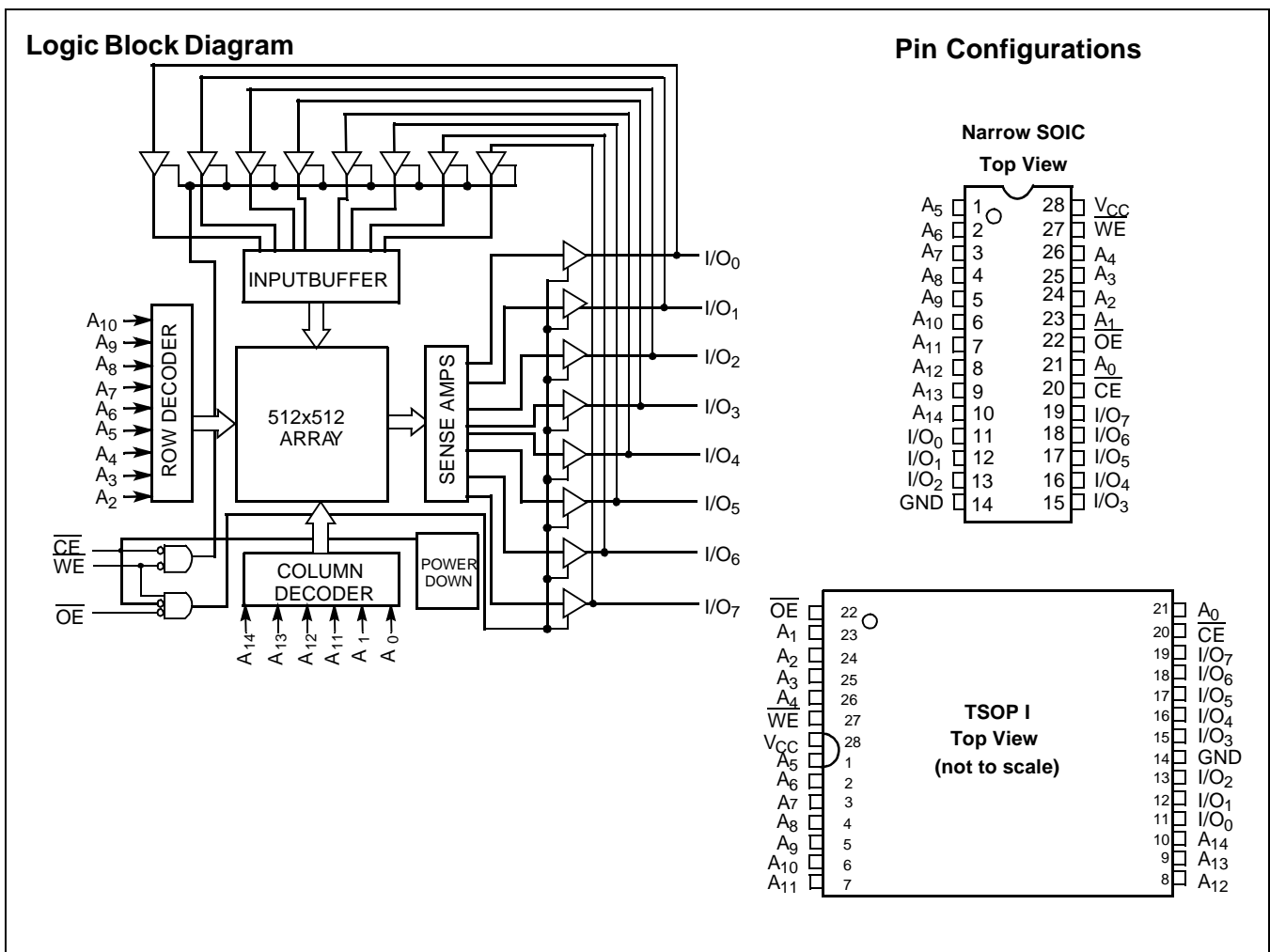
Functional Description

The WCMS0808C1X is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active

LOW output enable (\overline{OE}) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected. The WCMS0808C1X is in the standard 450-mil-wide (300-mil body width) SOIC and packages.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... 0°C to +70°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[1]..... -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1]..... -0.5V to V_{CC} + 0.5V
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

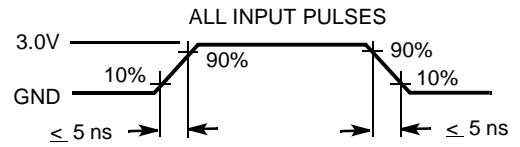
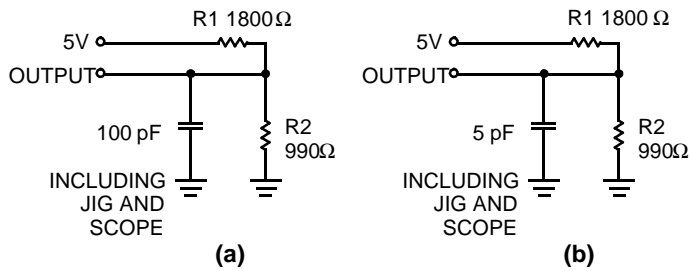
Parameter	Description	Test Conditions	WCMS0808C1X			Unit
			Min.	Typ ^[2]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage		-0.5		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-0.5		+0.5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-0.5		+0.5	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		25	50	mA
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		0.3	0.5	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0		0.1	10	μA

Capacitance^[3]

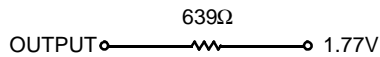
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

Note:

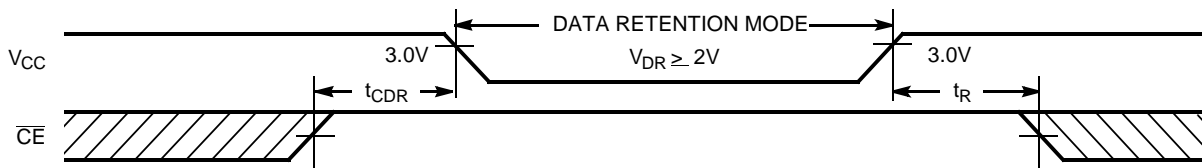
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT


Data Retention Characteristics

Parameter	Description	Conditions ^[4]	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = 3.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0			V
I_{CCDR}	Data Retention Current			0.1	10	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[3]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform

Note:

4. No input may exceed $V_{CC}+0.5V$.

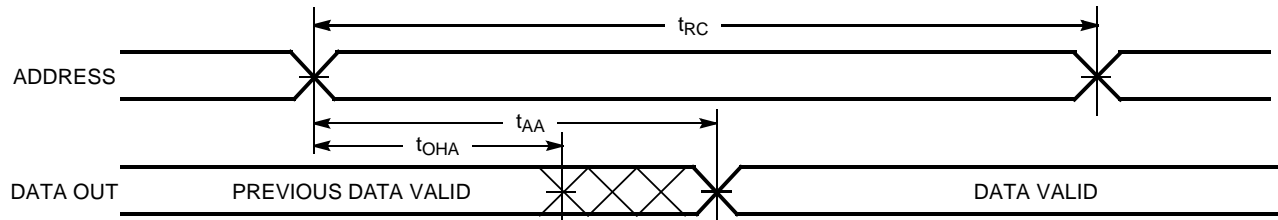
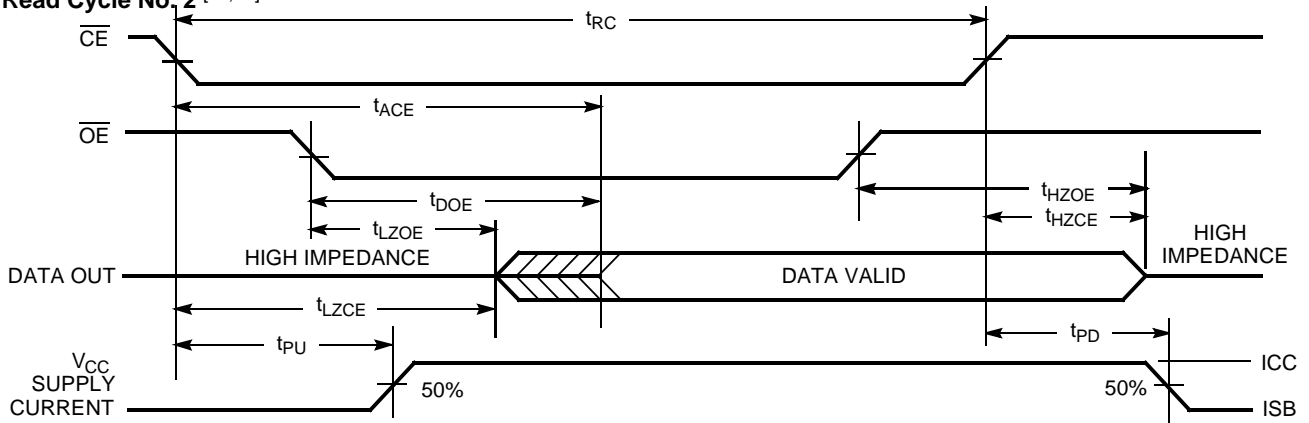


Switching Characteristics Over the Operating Range^[10]

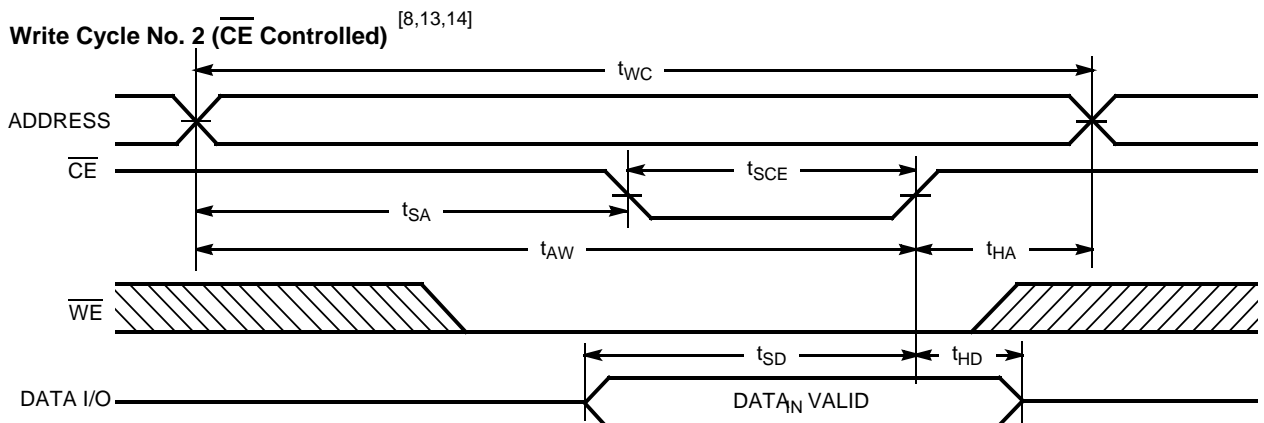
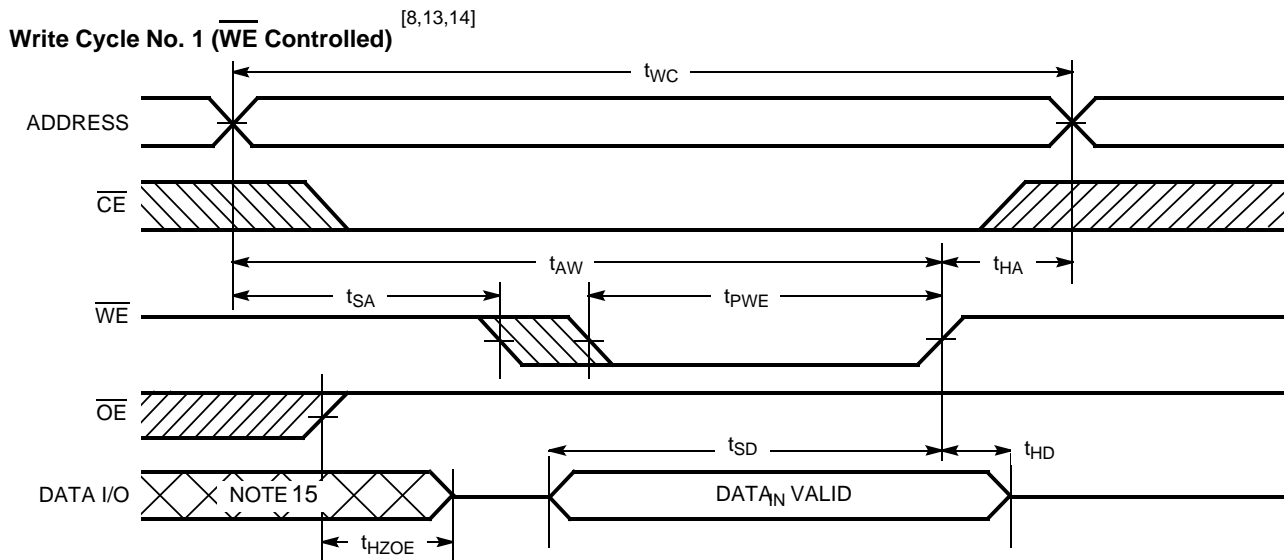
Parameter	Description	WCMS0808C1X		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	5		ns
t _{ACE}	\overline{CE} LOW to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[6]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		70	ns
WRITE CYCLE ^[8, 9]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE} LOW to Write End	60		ns
t _{AW}	Address Set-Up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	50		ns
t _{SD}	Data Set-Up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	5		ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

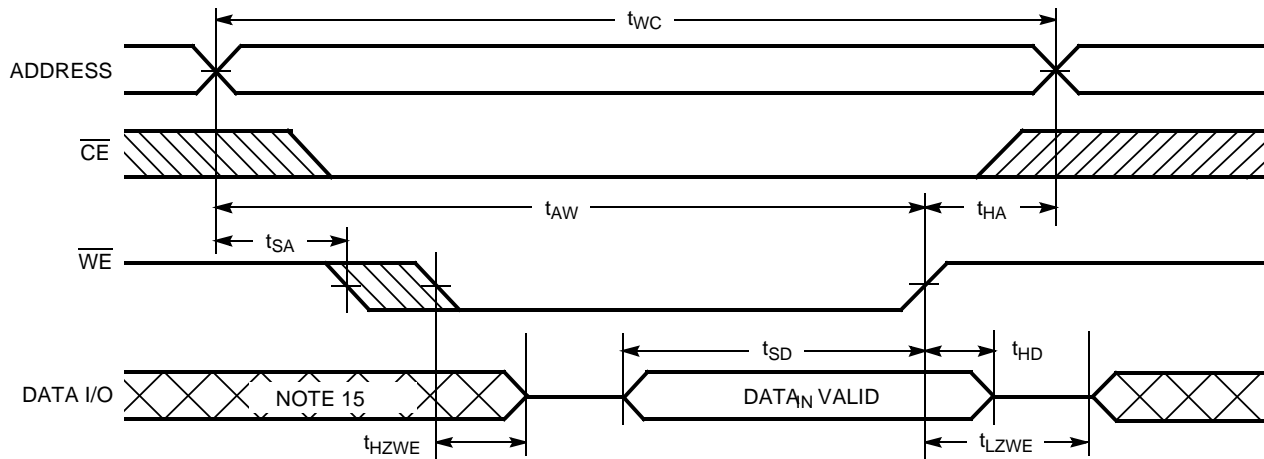
Switching Waveforms
Read Cycle No. 1 ^[10,11]

Read Cycle No. 2 ^[11,12]

Notes:

10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Notes:

13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) ^[9,14]

Note:

15. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

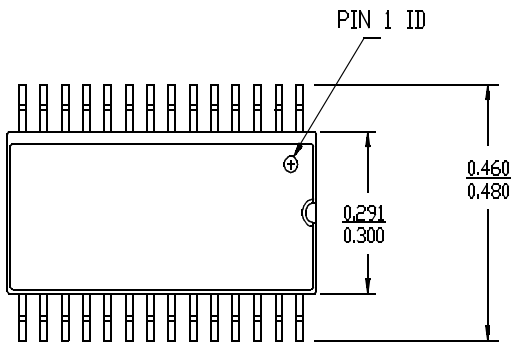
CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

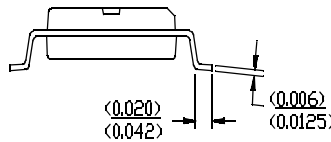
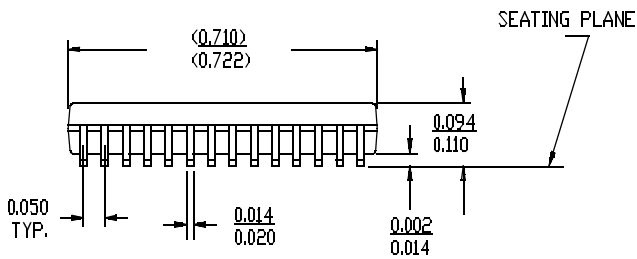
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMS0808C1X-NF70	N28	28-Lead 450-Mil (300-Mil Body Width) Narrow SOIC	Industrial
	WCMS0808C1X-TF70	T28	28-Lead Thin Small Outline Package (TSOP)	

Package Diagrams

28-Lead 450-Mil (300-Mil Body Width) SOIC, N28



DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.

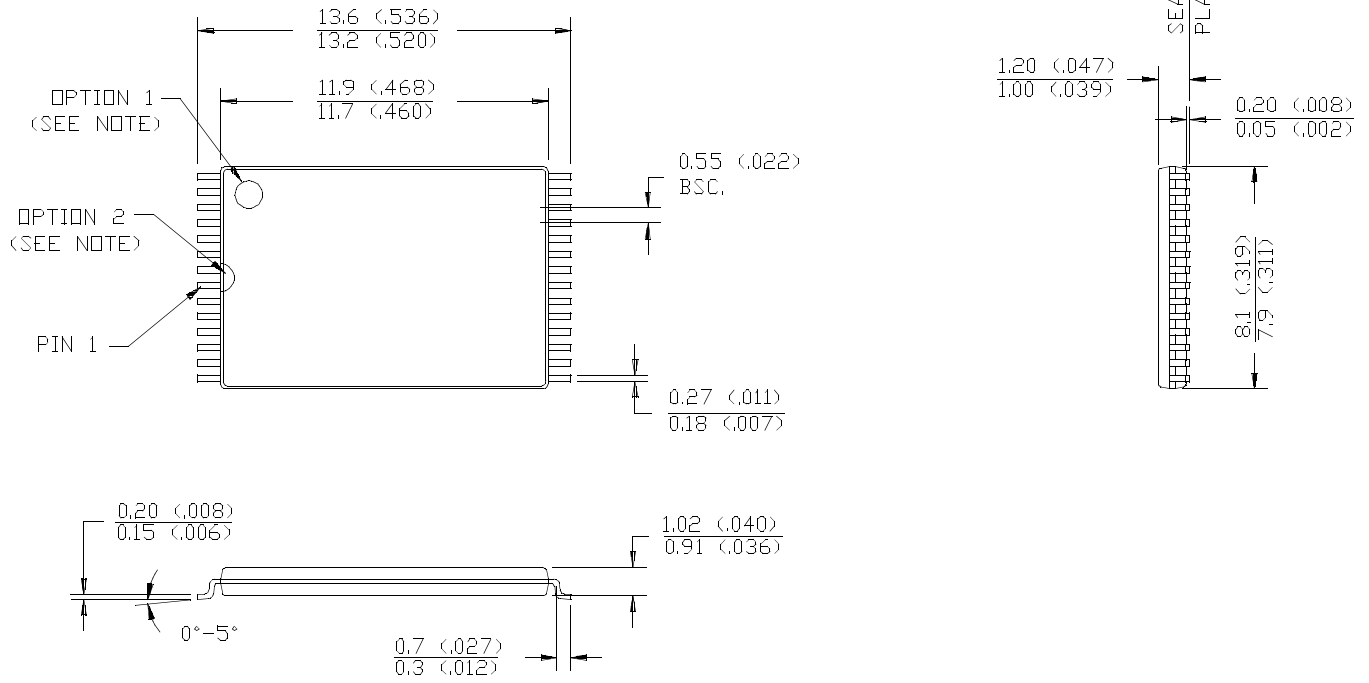


Package Diagrams (continued)

28-Lead Thin Small Outline Package, T28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)
MAX.
MIN.





WCMS0808C1X

32Kx8 Static RAM

Document Title: WCMS0808C1X, 32K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14010	115225	1/17/02	MGN	New Datasheet