



WEIDA

WCFS0808V1E

32K x 8 3.3V Static RAM

**Features**

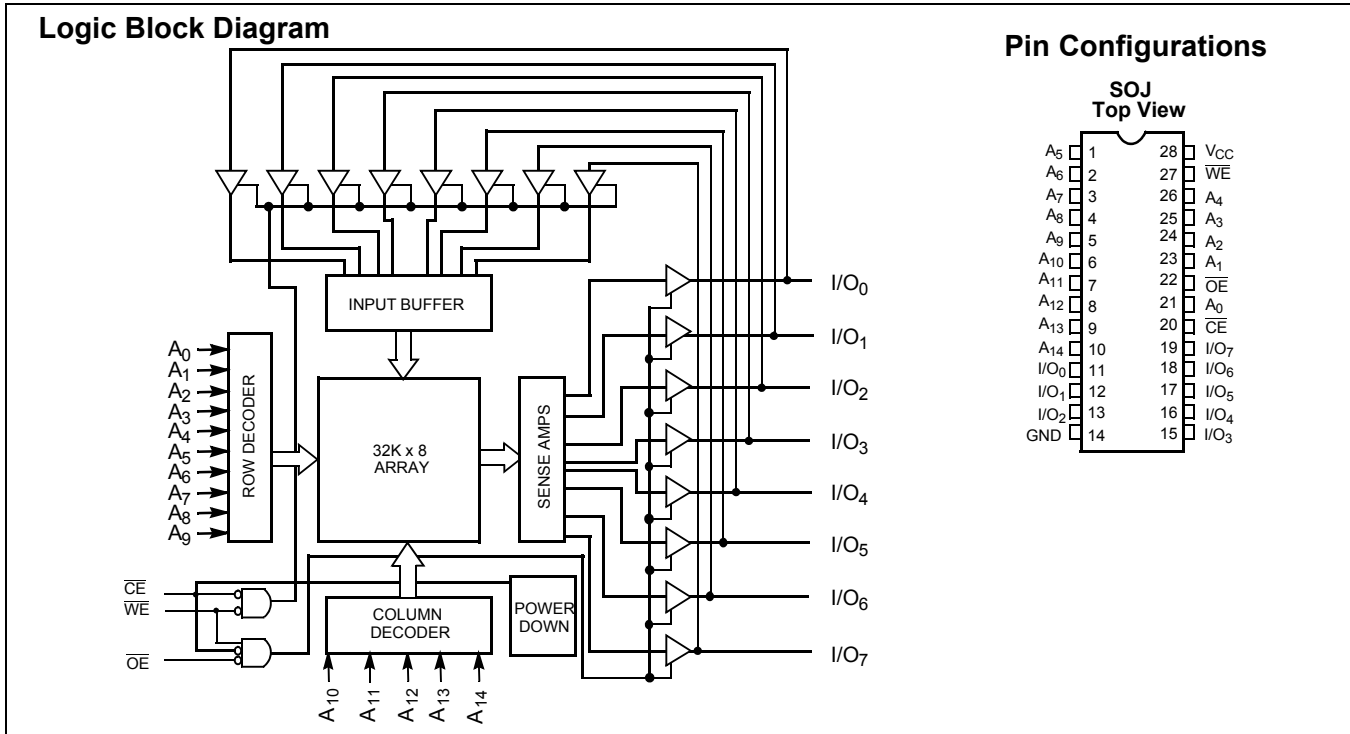
- Single 3.3V power supply
- Ideal for low-voltage cache memory applications
- High speed  
— 12/15 ns
- Plastic SOJ and TSOP packaging

**Functional Description**

The WCFS0808V1E is a high-performance 3.3V CMOS Static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE) and active LOW Output Enable (OE) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

An active LOW Write Enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When CE and WE inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>14</sub>). Reading the device is accomplished by selecting the device and enabling the outputs, CE and OE active LOW, while WE remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable (WE) is HIGH. The WCFS0808V1E is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I packages.



**Selection Guide**

	WCFS0808V1E 12ns	WCFS0808V1E 15ns
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	55	50
Maximum CMOS Standby Current (µA)	500	500

Pin Configuration

TSOP  
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Output Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ±300 mV

Electrical Characteristics Over the Operating Range<sup>[1]</sup>

Parameter	Description	Test Conditions	WCFS0808V1E 12ns		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current		-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[2]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		55	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> , or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		5	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs <sup>[3]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, WE ≥ V <sub>CC</sub> - 0.3V or WE ≤ 0.3V, f = f <sub>MAX</sub>		500	μA

Notes:

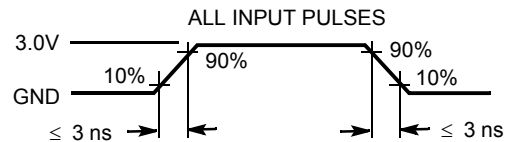
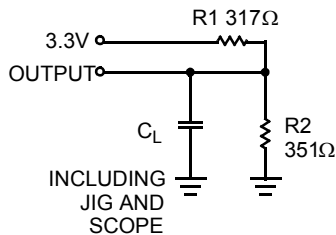
1. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Device draws low standby current regardless of switching on the addresses.

**Electrical Characteristics** Over the Operating Range (continued)

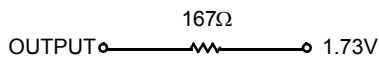
Parameter	Description	Test Conditions	WCFS0808V1E 15ns		Unit
			Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -2.0 \text{ mA}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4.0 \text{ mA}$		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage		-0.3	0.8	V
$I_{IX}$	Input Load Current		-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC},$ Output Disabled	-5	+5	$\mu\text{A}$
$I_{OS}$	Output Short Circuit Current <sup>[2]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		50	mA
$I_{SB1}$	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH},$ $V_{IN} \geq V_{IH},$ or $V_{IN} \leq V_{IL},$ $f = f_{MAX}$		5	mA
$I_{SB2}$	Automatic CE Power-Down Current — CMOS Inputs <sup>[3]</sup>	Max. $V_{CC}, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V,$ $\overline{WE} \geq V_{CC} - 0.3V$ or $\overline{WE} \leq 0.3V,$ $f = f_{MAX}$		500	$\mu\text{A}$

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$ : Addresses	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	5	pF
$C_{IN}$ : Controls			6	pF
$C_{OUT}$	Output Capacitance		6	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT


**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

Parameter	Description	WCFS0808V1E 12ns		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	12		ns
$t_{AA}$	Address to Data Valid		12	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>				
$t_{WC}$	Write Cycle Time	12		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	8		ns
$t_{AW}$	Address Set-Up to Write End	8		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	8		ns
$t_{SD}$	Data Set-Up to Write End	7		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		7	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and capacitance  $C_L = 30$  pF.
- At any given temperature and voltage condition,  $t_{HZOE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in AC Test Loads. Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics** Over the Operating Range<sup>[5]</sup> (Continued)

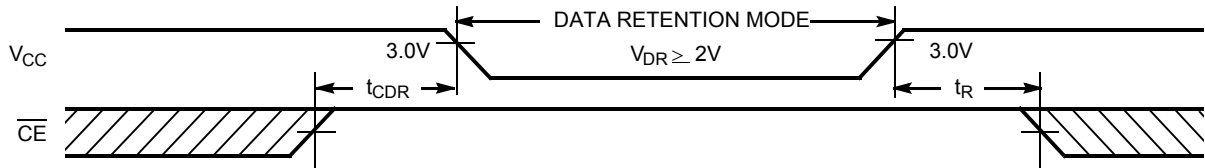
Parameter	Description	WCFS0808V1E 15ns		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	15		ns
$t_{AA}$	Address to Data Valid		15	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		15	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>				
$t_{WC}$	Write Cycle Time	15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10		ns
$t_{AW}$	Address Set-Up to Write End	10		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		ns
$t_{SD}$	Data Set-Up to Write End	8		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		7	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		ns

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$t_{CDR}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R$	Operation Recovery Time		$t_{RC}$		ns

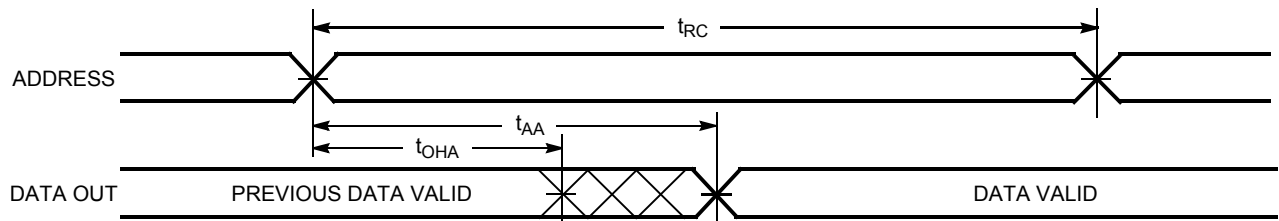


### Data Retention Waveform

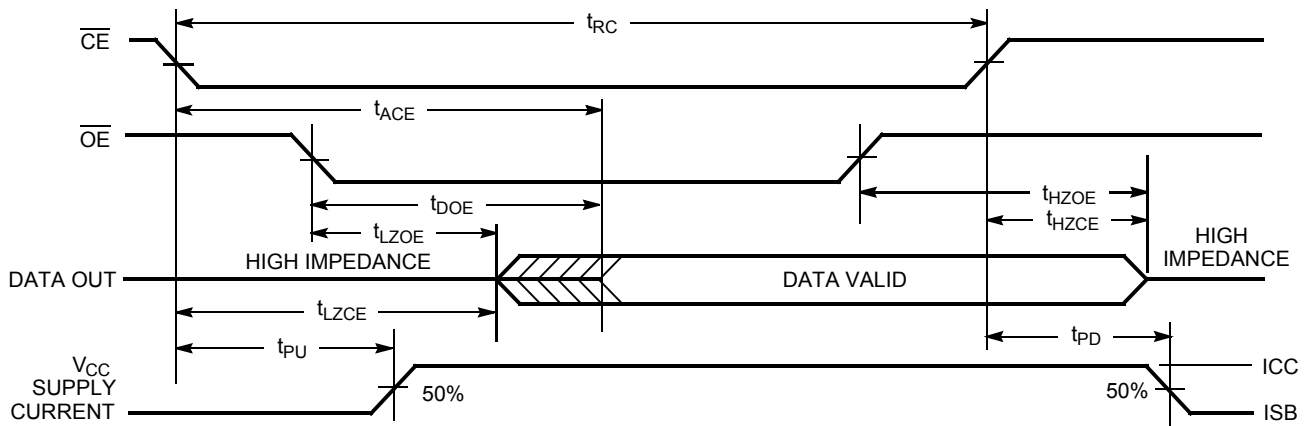


### Switching Waveforms

#### Read Cycle No. 1<sup>[10, 11]</sup>



#### Read Cycle No. 2<sup>[11, 12]</sup>



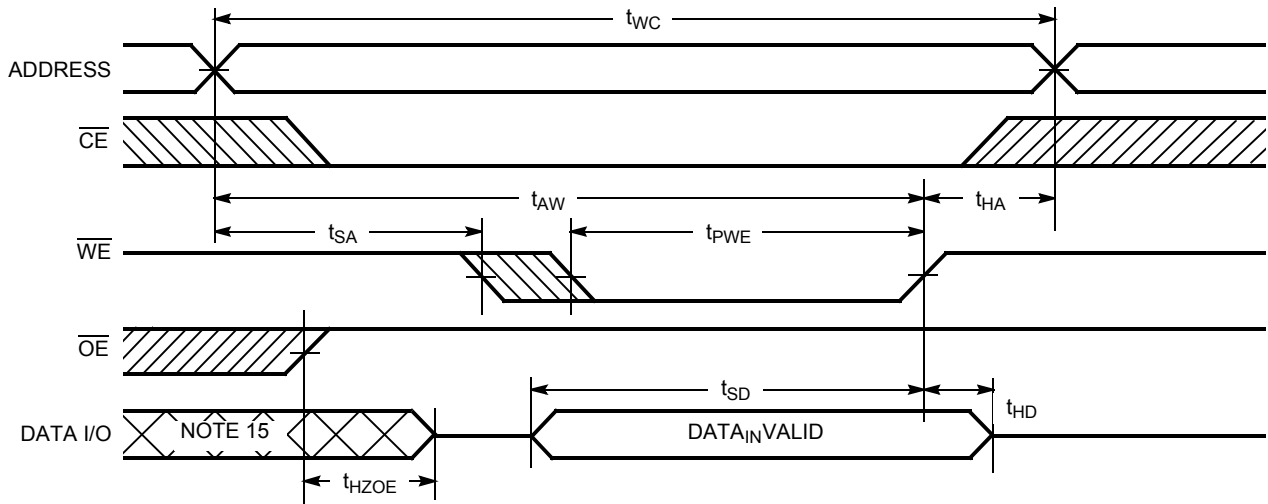
**Notes:**

- 10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 11. WE is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

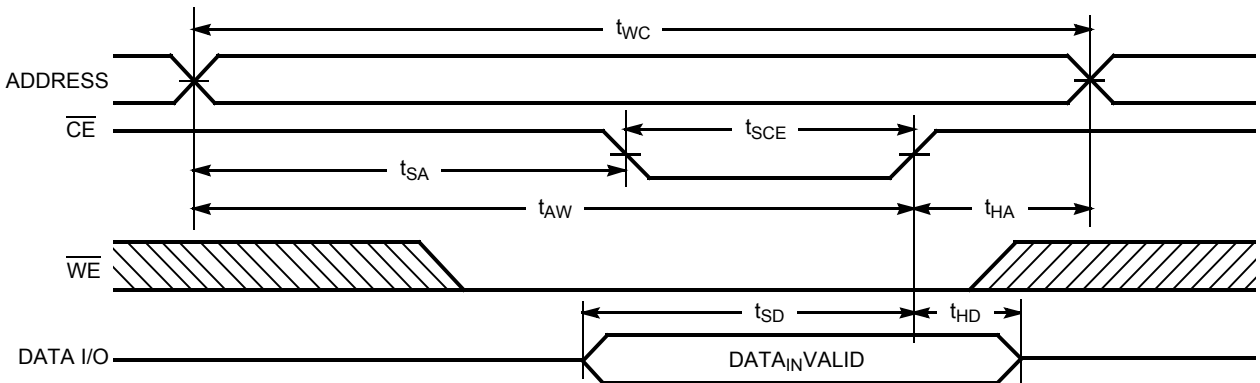


Switching Waveforms (continued)

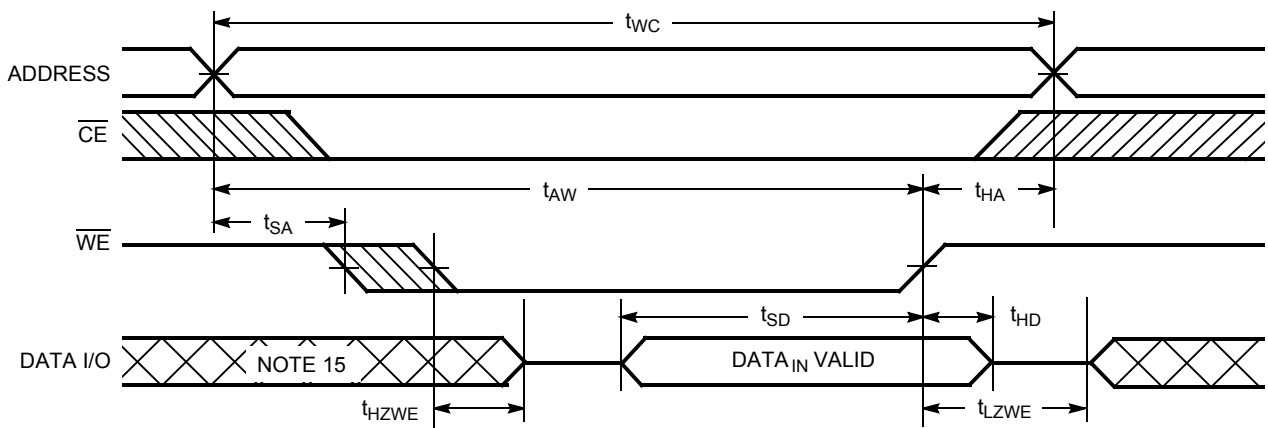
Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[8, 13, 14]</sup>



Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[8, 13, 14]</sup>



Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[9, 14]</sup>



Notes:

- 13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 15. During this period, the I/Os are in the output state and input signals should not be applied.



**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

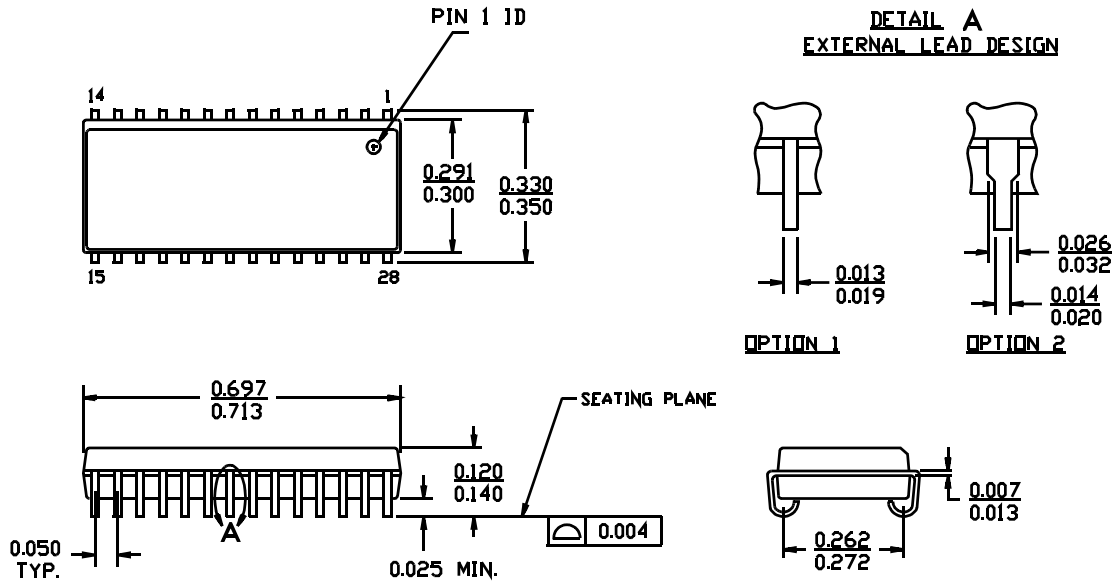
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	WCFS0808V1E-JC12	J	28-Lead Molded SOJ	Commercial
15	WCFS0808V1E-JC15	J	28-Lead Molded SOJ	
	WCFS0808V1E-TC15	T	28-Lead Thin Small Outline Package	



Package Diagrams

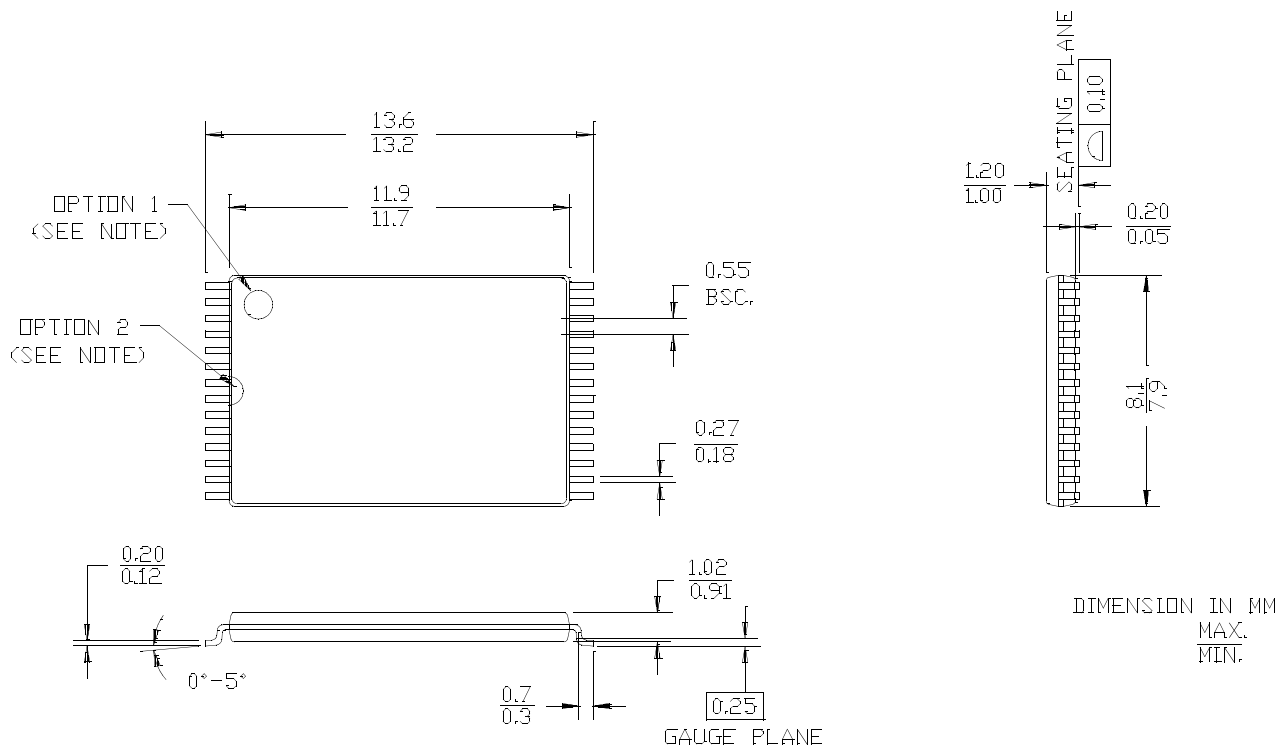
28-Lead (300-Mil) Molded SOJ J

DIMENSIONS IN INCHES MIN.  
MAX.



28-Lead Thin Small Outline Package Type 1 (8x13.4 mm) T

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2





**Revision History**

<b>Document Title: WCFS0808V1E 32K x 8 3.3V Static RAM</b> <b>Document Number: Document #: 38-05225 Rev. **</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>ISSUE DATE</b>	<b>ORIG. OF CHANGE</b>	<b>DESCRIPTION OF CHANGE</b>
**	113103	1/25/2002	XFL	New Datasheet