



200MHZ CLOCK FOR SOLANO CHIPSET

1.0 GENERAL DESCRIPTION

The W83194BR-138 is a Clock Synthesizer for Intel 815 Solano chipset. W83194BR-138 provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

The W83194BR-138 provides I²C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.25% and 0.5% center type spread spectrum to reduce EMI.

The W83194BR-138 provides stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio. Also the skew of CPU, SDRAM and 3V66 clock outputs are programmable. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83194BR-138 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V/ns slew rate into 20 pF loads as maintaining 50±5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V/ns slew rate.

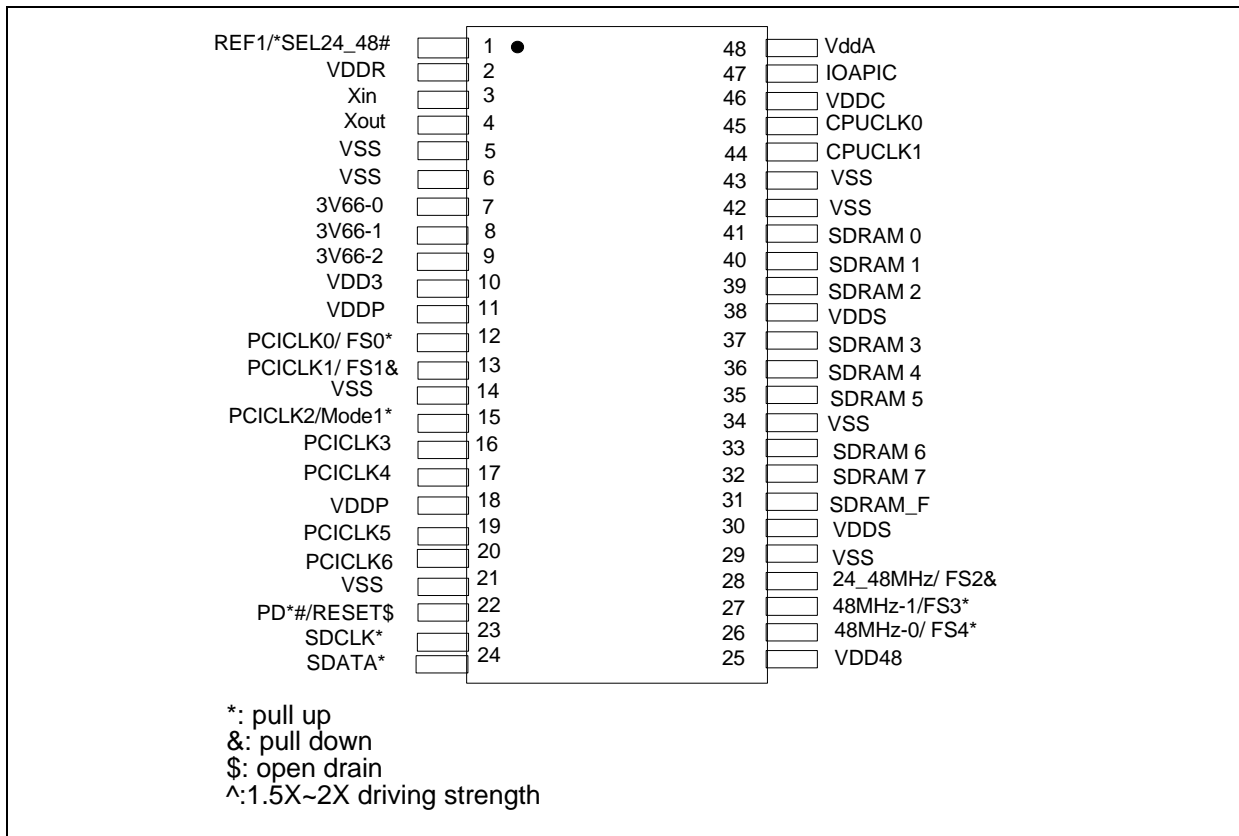
2.0 PRODUCT FEATURES

- 2 CPU clocks
- 3 3V66 clocks
- 9 SDRAM clocks for 2 DIMMs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
(VDDR = VDDP=VDDS = VDD48 = VDD3 = 3.3V, VDDA=VDDC=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- I²C 2-Wire serial interface and I²C read back
- 0.25% or 0.5% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
(mode as Tri-state or Normal)
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP



PRELIMINARY

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	3	IN	Crystal input with internal loading capacitors(36pF) and feedback resistors.
Xout	4	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors(36pF).

4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:1]	45,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset.
PD#/ RESET\$	22	I/OD	If Mode1*=1, Power Down mode when driven low. If Mode1*=0, 4ms pulse RESET# (open drain) when Watch dog timer time out
IOAPIC	47	OUT	Clock outputs synchronous with PCI clock and powered by VddA.
SDRAM_F, SDRAM[0:7]	31,32,33,35,36,37,39,40,41	OUT	SDRAM clock outputs.
PCICLK0/ *FS0	12	I/O	3.3V 33MHz PCI clock during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=1).
PCICLK1/ FS1&	13	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=0).
PCICLK2/ Mode1*	15	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for Mode1* pin at initial power up for the output PD#/RESET# output selection.
PCICLK [3:6]	16,17,19,20	OUT	Low skew (< 250ps) PCI clock outputs.
3V66 [0:2]	7,8,9	OUT	3.3V output clocks for the chipset.



PRELIMINARY

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	24	I/O	Serial data of I ² C 2-wire control interface with internal pull-up resistor.
*SDCLK	23	IN	Serial clock of I ² C 2-wire control interface with internal pull-up resistor.

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / *SEL24_48#	1	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Latched input for SEL24_48 at initial power up for H/W selecting the output frequency of 24_48MHz (Default=1, 24MHz).
24_48MHz/FS2&	28	I/O	24MHz or 48MHz output clock. Default is 24MHz. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=0).
48MHz_0/ FS3*	27	I/O	48MHz / Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=1).
48MHz_1/ FS4*	26	I/O	48MHz / Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=1).

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddC,VddA	46,48	Power supply for CPU & IOAPIC, 2.5V or 3.3V.
Vdd48	25	Power supply for 48MHz output,3.3V.
Vdd3	10	Power supply for 3V_66 output, 3.3V.
VddP	11,18	Power supply for PCICLK, 3.3V.
VddR	2	Power supply for REF0, 3.3V.
VddS	30,38	Power supply for SDRAM_F,SDRAM[0:11], nominal 3.3V.
Vss	5,6,14,21,29,34,42,43	Circuit Ground.



PRELIMINARY

5.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU(MHz)	SDRAM (MHz)	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	66.67	100.00	66.67	33.33	16.67
0	0	0	0	1	66.87	100.31	66.87	33.44	16.72
0	0	0	1	0	68.67	103.00	68.67	34.33	17.17
0	0	0	1	1	71.34	107.00	71.34	35.67	17.83
0	0	1	0	0	100.00	100.00	66.67	33.33	16.67
0	0	1	0	1	100.30	100.30	66.87	33.43	16.72
0	0	1	1	0	103.00	103.00	68.67	34.33	17.17
0	0	1	1	1	107.00	107.00	71.33	35.67	17.83
0	1	0	0	0	133.33	133.33	66.67	33.33	16.67
0	1	0	0	1	133.73	133.73	66.87	33.43	16.72
0	1	0	1	0	137.33	137.33	68.67	34.33	17.17
0	1	0	1	1	120.00	120.00	60.00	30.00	15.00
0	1	1	0	0	133.33	100.00	66.67	33.33	16.67
0	1	1	0	1	133.73	100.30	66.87	33.43	16.72
0	1	1	1	0	137.33	103.00	68.67	34.33	17.17
0	1	1	1	1	120.00	90.00	60.00	30.00	15.00
1	0	0	0	0	136.00	136.00	68.00	34.00	17.00
1	0	0	0	1	140.00	140.00	70.00	35.00	17.50
1	0	0	1	0	142.67	142.67	71.33	35.67	17.83
1	0	0	1	1	145.33	145.33	72.67	36.33	18.17
1	0	1	0	0	136.00	102.00	68.00	34.00	17.00
1	0	1	0	1	140.00	105.00	70.00	35.00	17.50
1	0	1	1	0	142.67	107.00	71.34	35.67	17.83
1	0	1	1	1	145.33	109.00	72.67	36.33	18.17
1	1	0	0	0	146.67	146.67	73.34	36.67	18.33
1	1	0	0	1	153.33	153.33	76.67	38.33	19.17
1	1	0	1	0	160.00	160.00	80.00	40.00	20.00
1	1	0	1	1	166.67	166.67	83.34	41.67	20.83
1	1	1	0	0	146.67	110.00	73.34	36.67	18.33
1	1	1	0	1	160.00	120.00	80.00	40.00	20.00
1	1	1	1	0	166.67	125.00	83.34	41.67	20.83
1	1	1	1	1	200.00	200.00	100.00	50.00	25.00



PRELIMINARY

5.0 SERIAL CONTROL 0REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2,) will be valid and acknowledged.

Frequency Table Setting by I2C (SEL5 ~ SEL0)

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU(MHz)	SDRAM (MHz)	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	0	66.67	100.00	66.67	33.33	16.67
0	0	0	0	0	1	66.87	100.31	66.87	33.44	16.72
0	0	0	0	1	0	68.67	103.00	68.67	34.33	17.17
0	0	0	0	1	1	71.34	107.00	71.34	35.67	17.83
0	0	0	1	0	0	100.00	100.00	66.67	33.33	16.67
0	0	0	1	0	1	100.30	100.30	66.87	33.43	16.72
0	0	0	1	1	0	103.00	103.00	68.67	34.33	17.17
0	0	0	1	1	1	107.00	107.00	71.33	35.67	17.83
0	0	1	0	0	0	133.33	133.33	66.67	33.33	16.67
0	0	1	0	0	1	133.73	133.73	66.87	33.43	16.72
0	0	1	0	1	0	137.33	137.33	68.67	34.33	17.17
0	0	1	0	1	1	120.00	120.00	60.00	30.00	15.00
0	0	1	1	0	0	133.33	100.00	66.67	33.33	16.67
0	0	1	1	0	1	133.73	100.30	66.87	33.43	16.72
0	0	1	1	1	0	137.33	103.00	68.67	34.33	17.17
0	0	1	1	1	1	120.00	90.00	60.00	30.00	15.00
0	1	0	0	0	0	136.00	136.00	68.00	34.00	17.00
0	1	0	0	0	1	140.00	140.00	70.00	35.00	17.50
0	1	0	0	1	0	142.67	142.67	71.33	35.67	17.83
0	1	0	0	1	1	145.33	145.33	72.67	36.33	18.17
0	1	0	1	0	0	136.00	102.00	68.00	34.00	17.00
0	1	0	1	0	1	140.00	105.00	70.00	35.00	17.50
0	1	0	1	1	0	142.67	107.00	71.34	35.67	17.83
0	1	0	1	1	1	145.33	109.00	72.67	36.33	18.17
0	1	1	0	0	0	146.67	146.67	73.34	36.67	18.33
0	1	1	0	0	1	153.33	153.33	76.67	38.33	19.17
0	1	1	0	1	0	160.00	160.00	80.00	40.00	20.00
0	1	1	0	1	1	166.67	166.67	83.34	41.67	20.83
0	1	1	1	0	0	146.67	110.00	73.34	36.67	18.33
0	1	1	1	0	1	160.00	120.00	80.00	40.00	20.00
0	1	1	1	1	0	166.67	125.00	83.34	41.67	20.83
0	1	1	1	1	1	200.00	200.00	100.00	50.00	25.00

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PRELIMINARY

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU(MHz)	SDRAM (MHz)	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
1	0	0	0	0	0	136.00	102.00	68.00	34.00	17.00
1	0	0	0	0	1	138.00	138.00	69.00	34.50	17.25
1	0	0	0	1	0	139.00	104.25	69.50	34.75	17.38
1	0	0	0	1	1	141.00	141.00	70.50	35.25	17.63
1	0	0	1	0	0	142.00	142.00	71.00	35.50	17.75
1	0	0	1	0	1	142.00	106.50	71.00	35.50	17.75
1	0	0	1	1	0	143.00	143.00	71.50	35.75	17.88
1	0	0	1	1	1	143.00	107.25	71.50	35.75	17.88
1	0	1	0	0	0	144.00	144.00	72.00	36.00	18.00
1	0	1	0	0	1	144.00	108.00	72.00	36.00	18.00
1	0	1	0	1	0	146.00	146.00	73.00	36.50	18.25
1	0	1	0	1	1	146.00	109.50	73.00	36.50	18.25
1	0	1	1	0	0	147.00	147.00	73.50	36.75	18.38
1	0	1	1	0	1	147.00	110.25	73.50	36.75	18.38
1	0	1	1	1	0	148.00	148.00	74.00	37.00	18.50
1	0	1	1	1	1	148.00	111.00	74.00	37.00	18.50
1	1	0	0	0	0	149.00	111.75	74.50	37.25	18.63
1	1	0	0	0	1	152.00	152.00	76.00	38.00	19.00
1	1	0	0	1	0	153.00	114.75	76.50	38.25	19.13
1	1	0	0	1	1	156.00	156.00	78.00	39.00	19.50
1	1	0	1	0	0	157.00	117.75	78.50	39.25	19.63
1	1	0	1	0	1	158.00	158.00	79.00	39.50	19.75
1	1	0	1	1	0	159.00	119.25	79.50	39.75	19.88
1	1	0	1	1	1	160.00	160.00	80.00	40.00	20.00
1	1	1	0	0	0	162.00	121.50	81.00	40.50	20.25
1	1	1	0	0	1	164.00	123.00	82.00	41.00	20.50
1	1	1	0	1	0	170.00	170.00	85.00	42.50	21.25
1	1	1	0	1	1	175.00	116.67	58.33	29.17	14.58
1	1	1	1	0	0	180.00	120.00	60.00	30.00	15.00
1	1	1	1	0	1	185.00	123.33	61.67	30.83	15.42
1	1	1	1	1	0	190.00	126.67	63.33	31.67	15.83
1	1	1	1	1	1	200.40	133.60	66.80	33.40	16.70

5.1 Register 0: CPU Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I ² C)
6	0	-	SSEL2 (Frequency table selection by software via I ² C)
5	0	-	SSEL1 (Frequency table selection by software via I ² C)
4	0	-	SSEL0 (Frequency table selection by software via I ² C)
3	0	-	0 = Selection by hardware 1 = Selection by software I ² C - Bit (2, 7:4)
2	0	-	SSEL4 (Frequency table selection by software via I ² C)
1	0	-	SSEL5 (Frequency table selection by software via I²C)
0	0	-	0 = Running 1 = Tristate all outputs

5.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	X	-	FS0#
6	X	-	FS1#
5	X	-	FS2#
4	X	-	FS3#
3	X	-	FS4#
2	0	-	1 = ±0.25% Center type Spread Spectrum Modulation 0 = ±0.5% Center type Spread Spectrum Modulation
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	1	-	1 = Center type Spread Spectrum Modulation 0 = Down type Spread Spectrum Modulation

5.3 Register 2: SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1		SDRAM7 (Active / Inactive)
6	1		SDRAM6 (Active / Inactive)
5	1		SDRAM5 (Active / Inactive)
4	1		SDRAM4 (Active / Inactive)
3	1		SDRAM3 (Active / Inactive)
2	1		SDRAM2 (Active / Inactive)
1	1		SDRAM1 (Active / Inactive)
0	1		SDRAM0 (Active / Inactive)

5.4 Register 3: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	31	SDRAM_F (Active / Inactive)
6	1	20	PCICLK6 (Active / Inactive)
5	1	19	PCICLK5 (Active / Inactive)
4	1	17	PCICLK4 (Active / Inactive)
3	1	16	PCICLK3 (Active / Inactive)
2	1	15	PCICLK2 (Active / Inactive)
1	1	13	PCICLK1 (Active / Inactive)
0	1	12	PCICLK0 (Active / Inactive)

5.5 Register 4: Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	9	3V66_2(Active / Inactive)
6	1	8	3V66_1(Active / Inactive)
5	1	7	3V66_0(Active / Inactive)
4	1	28	24_48MHz(Active / Inactive)
3	1	47	IOAPIC(Active / Inactive)
2	1	27	48MHz_0(Active / Inactive)
1	1	26	48MHz_1(Active / Inactive)
0	1	1	REF0 (Active / Inactive)

5.6 Register 5: SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	CSkew2 (CPU to SDRAM skew program bit)
6	0	-	CSkew1 (CPU to SDRAM skew program bit)
5	0	-	CSkew0 (CPU to SDRAM skew program bit)
4	1	-	CASkew2 (CPU to 3V66 skew program bit)
3	0	-	CASkew1 (CPU to 3V66 skew program bit)
2	0	-	CASkew0 (CPU to 3V66 skew program bit)
1	1	44	CPUCLK1(Active / Inactive)
0	1	45	CPUCLK0(Active / Inactive)



PRELIMINARY

5.7 Register 6~10: Step-less M/N mode Control Registers

5.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	1	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

5.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Version ID
2	0	-	Winbond Version ID
1	1	-	Winbond Version ID
0	0	-	Winbond Version ID

Register10 Bit3-6				Ratio		
Bit6	Bit 5	Bit 4	Bit 3			
DS3	DS2	DS1	DS0	CPU	SDRAM	3V66
0	0	0	0	4	4	6
0	0	0	1	3	3	6
0	0	1	0	2	3	6
0	0	1	1	2	2	6
0	1	0	0	6	4	6
0	1	0	1	3	4	6
0	1	1	0	6	3	6
0	1	1	1	4	3	6
1	0	x	x	2	2	4
1	1	x	x	2	4	6

6.0 SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V _{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T _{STG}	Storage Temperature	- 65°C to + 150°C
T _B	Ambient Temperature	- 55°C to + 125°C
T _A	Operating Temperature	0°C to + 70°C

6.2 AC CHARACTERISTICS

VddR=Vdd3=VddP=VddS=3.3V - 5 %, VddC = VddA= 2.375V~2.9V , T_A = 0° C to +70° C						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t _{OFF}	1		4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t _{SKEW}			250	ps	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t _{CCJ}			±250	ps	
CPU/SDRAM Absolute Jitter	t _{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW _J			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t _{TLH} t _{THL}	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V _{over}	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V _{RBE}	0.7		2.1	V	Ring Back must not enter this range.

6.3 DC CHARACTERISTICS

$V_{ddR}=V_{dd3}=V_{ddP}=V_{ddS}=3.3V - 5\%, V_{ddC} = V_{ddA}= 2.375V\sim 2.9V, T_A = 0^\circ C \text{ to } +70^\circ C$						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		$V_{dd}+0.3$	V_{dc}	
Input Low Current (no pull-up Resistors)	I_{IL}	-5	2.0		μA	
Input Low Current (pull-up Resistors)	I_{IL}	-200	-100		μA	
Input High Current	I_{IH}	-5		5	μA	
Operating Current	I_{DD}		60	100	mA	@66M
Power Down Current	I_{DDPD}		400	600	μA	$C_L= 0pF$
Input Frequency	F_i		14.318		MHz	$V_{dd}=3.3V$
Pin Inductance	L_{pin}		7		nH	
Input Capacitance	C_{IN}			5	pF	Logic Inputs
	C_{OUT}		6		pF	Output pins capacitance
	C_{INX}	13.5		22.5	pF	X1 & X2 pins
Transition Time	T_{Tra}			3	mS	
Disable/Enable Delay	T	1		10	nS	
Clock stabilization	T_{STA}			3	mS	

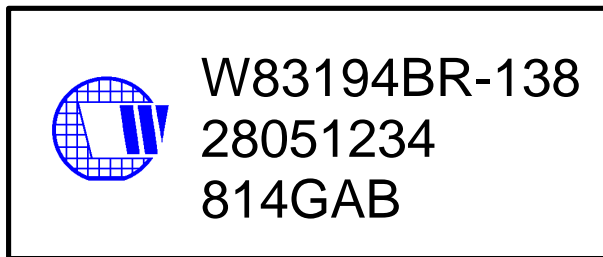


PRELIMINARY

7.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-138	48 PIN SSOP	Commercial, 0°C to +70°C

8.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-138

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

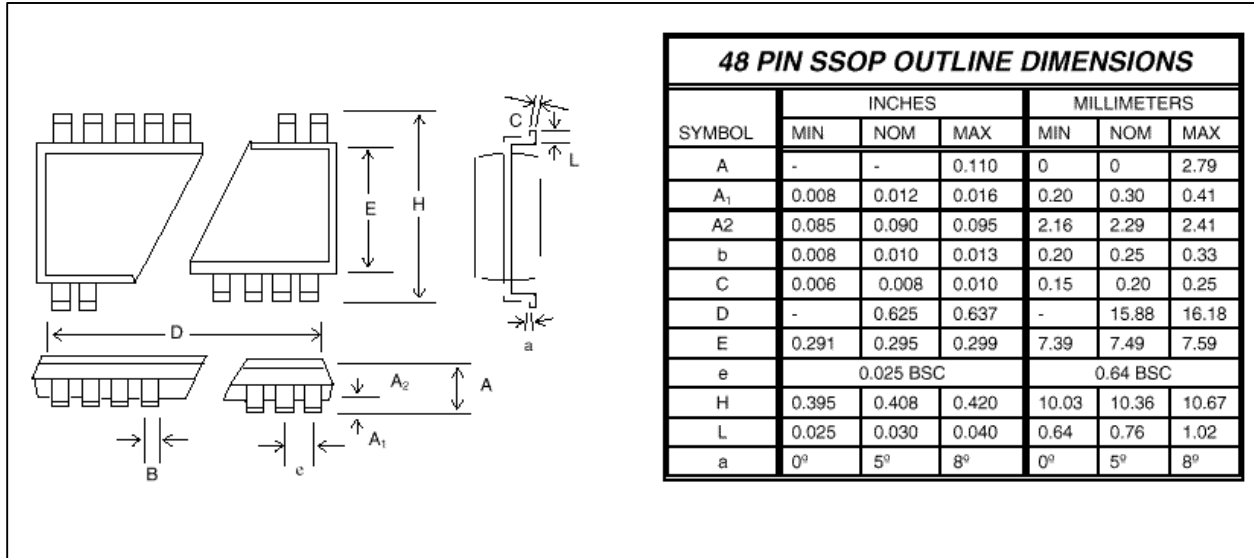
G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.

9.0 PACKAGE DRAWING AND DIMENSIONS



Headquarters
 No. 4, Creation Rd. III
 Science-Based Industrial Park
 Hsinchu, Taiwan
 TEL: 886-35-770066
 FAX: 886-35-789467
 www: <http://www.winbond.com.tw/>

Taipei Office
 11F, No. 115, Sec. 3, Min-Sheng East Rd.
 Taipei, Taiwan
 TEL: 886-2-7190505
 FAX: 886-2-7197502
 TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
 Rm. 803, World Trade Square, Tower II
 123 Hoi Bun Rd., Kwun Tong
 Kowloon, Hong Kong
 TEL: 852-27516023-7
 FAX: 852-27552064

Winbond Electronics (North America) Corp.
 2730 Orchard Parkway
 San Jose, CA 95134 U.S.A.
 TEL: 1-408-9436666
 FAX: 1-408-9436668

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