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VP1058

8-BIT, 25MHz, VIDEO FLASH ADC (SINGLE + 5V SUPPLY)

The VP1058 is a low power analog-to-digital flash converter which requires no preceding sample and hold stage. Operating from a single +5V supply, it is capable of digitising analog signals with frequencies up to the Nyquist limit.

Output data is available in four possible 8-bit formats, selectable via two digital control inputs, giving either true or inverted code in binary or offset twos' complement.

FEATURES

- 8-Bit Resolution
- 25MHz Conversion Rate
- 60MHz 3dB Analog Input Bandwidth
- Single +5V Supply Operation
- Low Power Consumption (Typically 670mW)
- +3V to +5V Analog Input Range
- Selectable Data Format
- TTL Compatible
- Direct Replacement for TDC 1058 or CXA 1096P
- Low Cost
- No Missing Codes - Guaranteed

APPLICATIONS

- Digital Television
- Computing
- Radar
- Medical Imaging
- Nucleonics
- Low-Cost, High-Speed Data Conversion

OPERATING TEMPERATURE RANGE

Commercial 0°C to 70°C (Still - Air ambient)

ORDERING INFORMATION

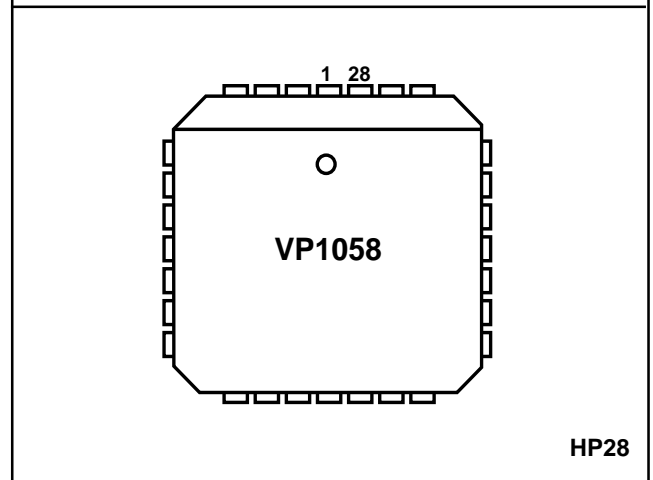
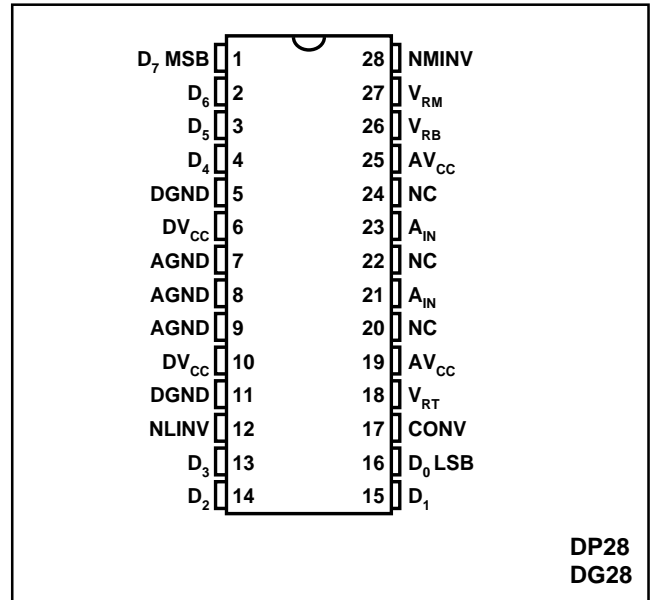
VP1058 F CG DPAS (Commercial - Plastic DIL Package, DP28)

VP1058 F CG HPAS (Commercial - Quad Plastic J Lead Package, HP28)

VP1058 F CG DGAS (Commercial - Ceramic DIL Package, DG28)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Analog input, A _{IN}	V _{CC} +0.5
Reference voltage V _{RT} , V _{RB}	V _{CC} +0.5
Reference voltage V _{RT} , V _{RB}	2.5V
Digital inputs	V _{CC}
Mid-ref input current	-50mA to +50mA
Digital output current	-20mA to +20mA
Voltage between AGND and DGND	-0.5V to +0.5V
Voltage between AV _{CC} and DV _{CC}	-0.5V to +0.5V



Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	D ₇ MSB	8	AGND	15	D ₁	22	NC
2	D ₆	9	AGND	16	D ₀ LSB	23	A _{IN}
3	D ₅	10	DV _{CC}	17	CONV	24	NC
4	D ₄	11	DGND	18	V _{RT}	25	AV _{CC}
5	DGND	12	NLINV	19	AV _{CC}	26	V _{RB}
6	DV _{CC}	13	D ₃	20	NC	27	V _{RM}
7	AGND	14	D ₂	21	A _{IN}	28	NMINV

Fig.1 Pin Connections (Top View)

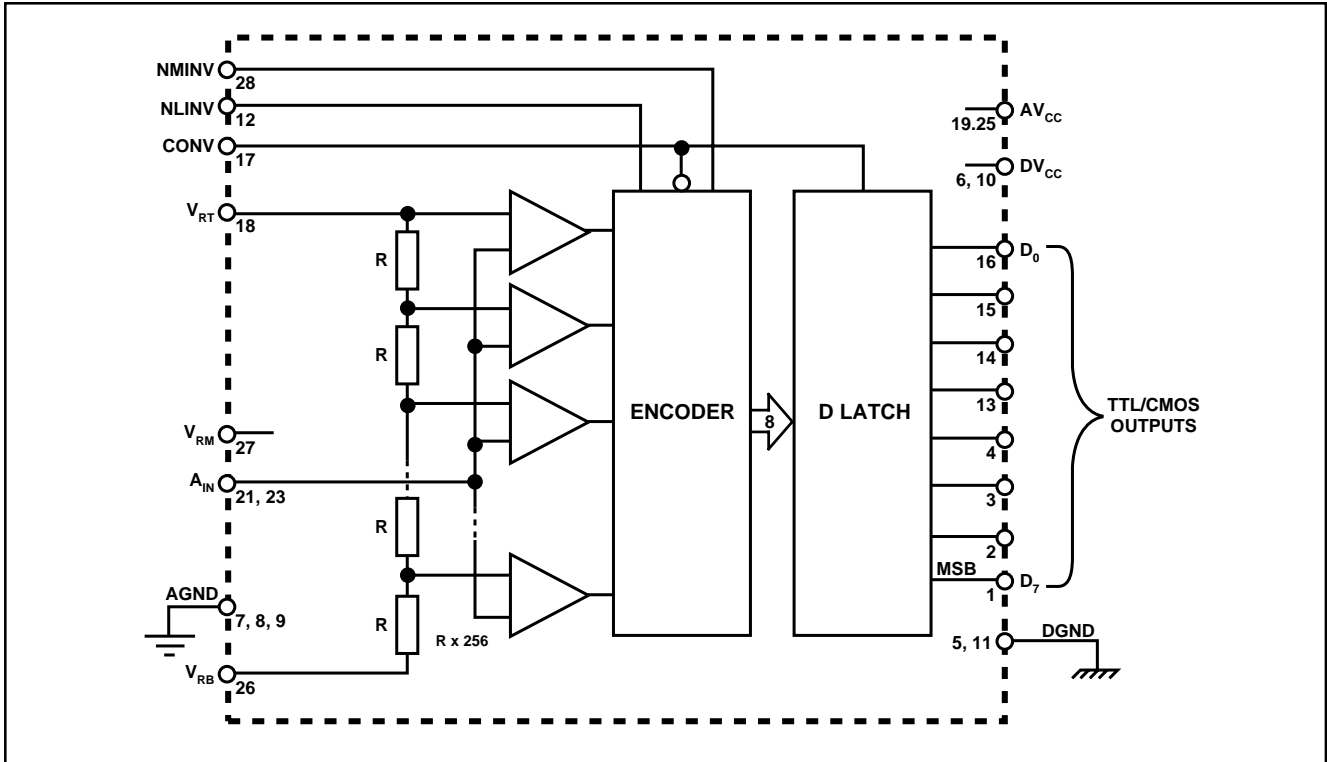


Fig.2 Internal block diagram

PIN DESCRIPTIONS

Pin No.	Function	Description
1	D ₇	Most significant bit (output data bit 7)
2 - 4	D ₆ - D ₄	Output data bits 6 to 4
5, 11	DGND	Digital ground
6, 10	DV _{CC}	Digital supply pin (+5V)
7 - 9	AGND	Analog ground
12	NLINV	Not Least significant bits INvert - inverts data D ₀ to D ₆ when taken low
13 - 15	D ₃ - D ₁	Output data bits 3 to 1
16	D ₀	Least significant bit (output data bit 0)
17	CONV	Clock input - the rate of input (CONVert) clock signal determines the ADC sampling rate
18	V _{RT}	Top of reference resistor chain
19, 25	AV _{CC}	Analog supply pin
20, 22, 24	NC	Not connected
21, 23	A _{IN}	Analog input pin
26	V _{RB}	Bottom of reference resistor chain
27	V _{RM}	Midpoint of reference resistor - can be used for linearity adjustment
28	NMINV	Not Most significant bit INvert - inverts data bit D ₇ when taken low

THERMAL CHARACTERISTICS

Storage Temperature Range	-65°C to +150°C		
Maximum Junction Operating Temperature	+175°C		
Lead Temperature (soldering 60 seconds)	300°C		
	DP	HP	DG
Junction to Ambient θ _{jA}	55	57	44
Junction to Case θ _{jc}	14	15	9

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5V ± 0.25V
Reference V _{RT}	5V ± 0.1V
Reference V _{RB}	3V ± 0.1V
AV _{CC} to DV _{CC}	0V ± 50mV
Analog Input	4V ± 1V

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions conditions (unless otherwise stated):

$$V_{CC} = +5V \pm 0.25V, T_{amb} = 25^{\circ}C$$

DC CHARACTERISTICS

Characteristic	Symbol	Temp	Test level	Value.			Units	Conditions	
				Min.	Typ.	Max.			
Power Supply									
Supply voltage	AV_{CC}/DV_{CC}	Full	4	4.75		5.25	V	AGND/DGND = 0V	
Supply current	I_{CC}	Full	4	95	125	165	mA		
Power dissipation	P	Full	4	500	670	900	mW		
		25	1	105	125	150	mA		
		25	1	540	670	830	mW		
Analog Input									
Input range	A_{IN}	Full	4	V_{RB}		V_{RT}	V	} $V_{RT} > V_{RB}$	
Input bias current	I_{IN}	Full	4	60	150	500	μA		
3dB bandwidth	f_{3dB}	25	4		60		MHz		
Input capacitance	C_{IN}	25	4		30		pF		
Reference Ladder									
Ladder resistance	R_D	Full	4	50	90	145	Ω		} $V_{RT} > V_{RB}$
		25	1	75	100	125	Ω		
Ladder voltage (top)	V_{RT}	Full	4		5.0	$AV_{CC} + 0.1$	V		
Ladder voltage (bottom)	V_{RB}	Full	4	2.5	3.0		V		
Ladder offset (top)	V_{RTO}	25	5		15		mV		
Ladder offset (bottom)	V_{RBO}	25	5		5		mV		
Ladder temp. coeff.	R_{TC}	Full	5		0.33		$\Omega/^{\circ}C$		
Digital Inputs									
Logic '1' voltage	V_{IH}	Full	4	2.0			V	} $V_I = V_{CC} = MAX$ } $V_I = 2.4V, V_{CC} = MAX$ } $V_I = 0.4V, V_{CC} = MAX$	
Logic '0' voltage	V_{IL}	Full	4			0.8	V		
Logic '1' current	I_{IH}	Full	4			350	μA		
Logic '1' current	I_{IH}	Full	4			75	μA		
Logic '0' current	I_{IL}	Full	4			-150	μA		
Logic '0' current	I_{IL}	Full	4				μA		
Digital Outputs									
Logic '1' voltage	V_{OH}	Full	4	2.4			V	} Into a standard LSTTL load	
		25	1	2.4			V		
Logic '0' voltage	V_{OL}	Full	4			0.4	V		
		25	1			0.4	V		
Static performance									
Differential non-linearity	DNL	Full	4		± 0.5		LSB		
		25	4		± 0.5		LSB		
Integral non-linearity	INL	Full	4		± 0.5		LSB		
		25	4		± 0.5		LSB		

AC CHARACTERISTICS

Characteristic	Symbol	Temp	Test level	Value.			Units	Conditions
				Min.	Typ.	Max.		
Clock min.high	t_{PW1}	Full	4	15			ns	} A_{IN} at FS & 12.5MHz
Clock min.low	t_{PW0}	Full	4	15			ns	
Max. conversion rate	f_{MAX}	Full	4	25			MHz	
Aperture delay	t_{AD}	25	5		3		ns	
Output data delay	t_D	25	4			25	ns	
		Full	4			30	ns	
Output hold time	t_{HO}	25	4	5			ns	
		Full	4	5			ns	
Aperture Jitter		25	5		50		ps	
Dynamic Performance								
Differential non-linearity	DNL	25	1	-0.85	± 0.5	+1	LSB	} $f_{CLK} = 25MHz$ } A_{IN} at FS & 1.019MHz
Integral non-linearity	INL	25	1		± 1	± 2	LSB	
S/N ratio	SNR	25	1		45		dB	
		Full	4		44.5		dB	
		25	4		44.0		dB	
		Full	4		43.5		dB	
		25	4		43.5		dB	
Effective No. of bits	ENOB	Full	4		43.0		dB	
		25	1		7.2		bits	
			4		7.1		bits	
			4		7.0		bits	

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ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency, at which the spectral power of the fundamental frequency as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

Aperture Delay

The delay between the falling edge of the CONV signal and the instant at which the analog input is sampled.

Aperture Jitter

The variation between successive samples of the aperture delay.

Conversion Rate

The maximum rate at which the converter will run.

Differential Non-Linearity (DNL)

The deviation of any code width from an ideal LSB step.

Effective Number of Bits (ENOB)

This is a measure of the dynamic performance which is calculated from the following expression.:

$$ENOB = \frac{SNR - 1.76}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

Integral Non-Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Data Delay

The delay between the 50% point of the rising edge of the CONV signal and the 50% point of any data output change.

Reference Ladder Offset

The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

Signal-to-Noise Ratio (SNR)

The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

Test Levels

- Level 1** - 100% production tested
- Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
- Level 3** - Sample tested only
- Level 4** - Parameter is guaranteed by design and characteristics testing
- Level 5** - Parameter is a typical value only

CONVERSION TIMING

Operation of the VP1058 requires that an external clock be applied to the CONV (convert) pin. This CONV signal synchronises the sampling, conversion, and output stages of the devices as shown in the timing diagram (Fig.3).

The analog input is sampled when the comparator array is latched after a rising edge on the CONV pin. This rising edge also causes the result of the previous sample to be transferred to the outputs. Data at the outputs is latched at the same time as the 255 to 8 encoding of the current sample. Both these operations are performed on the falling edge of the CONV signal. This results in a 'pipeline' delay which means that the

digital result of sample 'N' is available for acquisition by external circuitry whilst sample 'N+2' is being taken.

The time interval between a rising edge on the CONV pin and the comparators latching is the aperture delay time (t_{AD}). This time may be subject to small variations mainly due to temperature and component matching. The short term uncertainty in the aperture delay time is specified by the aperture jitter (or aperture error). Output data becomes valid after t_D (output data delay). Data remains valid for at least t_{HO} (output hold time) after the rising edge of the CONV pin.

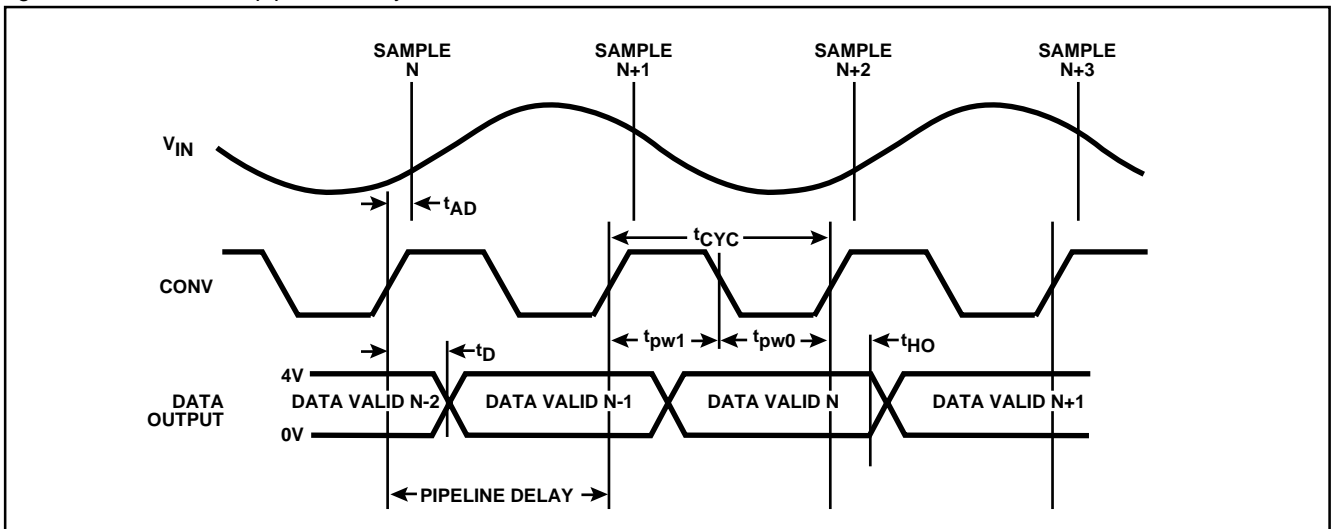


Fig.3 Timing diagram

GENERAL CIRCUIT DESCRIPTION

The VP1058 employs a 'flash' architecture consisting of a reference resistor chain, an array of 256 comparators, encoding logic, and a full 8-bit D-type output latch. The 255 reference levels generated by the resistor chain are compared with the analog input signal by the comparator array. This produces a thermometer code which the encoding logic converts into an 8-bit word. The D-type latch accepts this data and holds the outputs until the next conversion. The format of the output data is determined by the NLINV and NMINV control lines.

Analog Input

The maximum amplitude and offset of the input is defined by the setting of the two reference voltages V_{RB} and V_{RT} . A signal outside this range will cause the output to be either full-scale positive or full-scale negative, depending on whether the signal is off scale in the positive or negative direction.

For optimum performance, the input signal should be biased at +4.0V with a 2V peak-to-peak amplitude. The necessary gain, offset and low impedance drive required for the input signal can be provided by use of a high slew rate ADC driver.

Reference Voltage

The reference chain between pins V_{RB} and V_{RT} is formed of 256 series resistors and has a total resistance of approximately 90Ω. A mid-reference pin, V_{RM} , is provided for precise setting of the integral linearity, although adjustment is not necessary to meet the data sheet specification.

The VP1058 will convert analog signals in the range $V_{RB} \leq A_{IN} \leq V_{RT}$, where V_{RB} and V_{RT} are in the range +3V to +5V. (The design of the VP1058 has been optimised for $V_{RB} = 3V$ and $V_{RT} = 5V$). All reference pins should be adequately decoupled close to the device.

Output Format

The output data format is controlled by the logic levels at the NLINV and NMINV pins as shown on the output coding table. These inputs are active low and may be tied to DV_{CC} for logic '1' or DGND for logic '0'. Both inputs are considered DC controls and as such should only be altered while the converter is in the steady state.

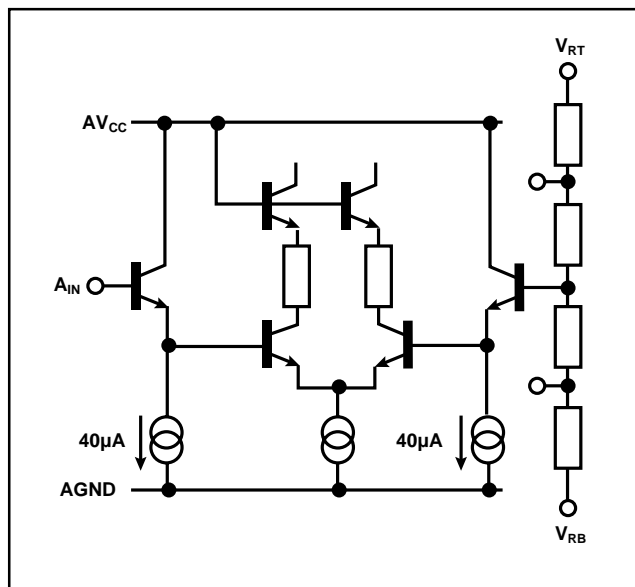


Fig.4 Analog input

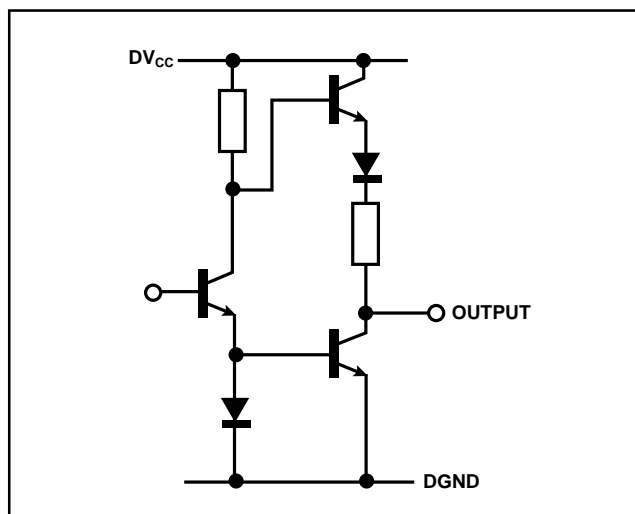


Fig.5 TTL output stage

Code	Input voltage		Binary		Offset 2s' complement	
	20.V Full Scale 7.8431mV Step	2.048V Full Scale 8.0mV Step	True	Inverted	True	Inverted
			NMINV = 1	0	0	1
			NLINV = 1	0	1	0
000	5.0V	5.0V	0000 0000	1111 1111	1000 0000	0111 1111
001	4.9922V	4.9922V	0000 0001	1111 1110	1000 0001	0111 1110
•	•	•	•	•	•	•
127	4.0039V	3.9840V	0111 1111	1000 0000	1111 1111	0000 0000
128	3.9961V	3.9760V	1000 0000	0111 1111	0000 0000	1111 1111
129	3.9882V	3.9680V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•	•	•
254	3.0079V	2.9680V	1111 1110	0000 0001	0111 1110	1000 0001
255	3.0V	2.960V	1111 1111	0000 0000	0111 1111	1000 0000

Table 1 Output coding

VP1058

APPLICATION NOTES

As with all high speed analog-to-digital converters, careful consideration must be given to circuit layout. The best performance from the VP1058 can be achieved by use of separate analog and digital ground planes. Ideally these should be connected at a point close to the device. This will reduce the amount of digital switching noise fed back into the analog section of the converter, so aiding device performance.

Supply line decoupling is important when dealing with mixed analog and digital signals, as they can provide a feedback path from the digital output currents. Therefore, the VP1058 should be decoupled close to the device supply pins with good quality high frequency, low inductance capacitors. Due to the high clock rates, long clock lines to the device should be avoided to reduce noise pick up.

A typical applications circuit is shown below. The analog input amplifier should be a wideband, high slew rate op-amp used to drive the input directly. A stable reference is needed for both input offset and gain control (e.g. REF12Z micropower voltage reference as shown in Fig.6). Both analog input pins should be connected close to the device with the input amplifiers feedback loop closed at the point. The reference inputs should be adequately decoupled to ground so as to limit the effects of system noise on conversion accuracy. A capacitor at the mid-reference point (as shown) may be useful in correcting any inherent reference ladder skew.

The circuit will accept a 1V p-p video signal and level shift and multiply it to provide the recommended 2V p-p signal to drive the VP1058.

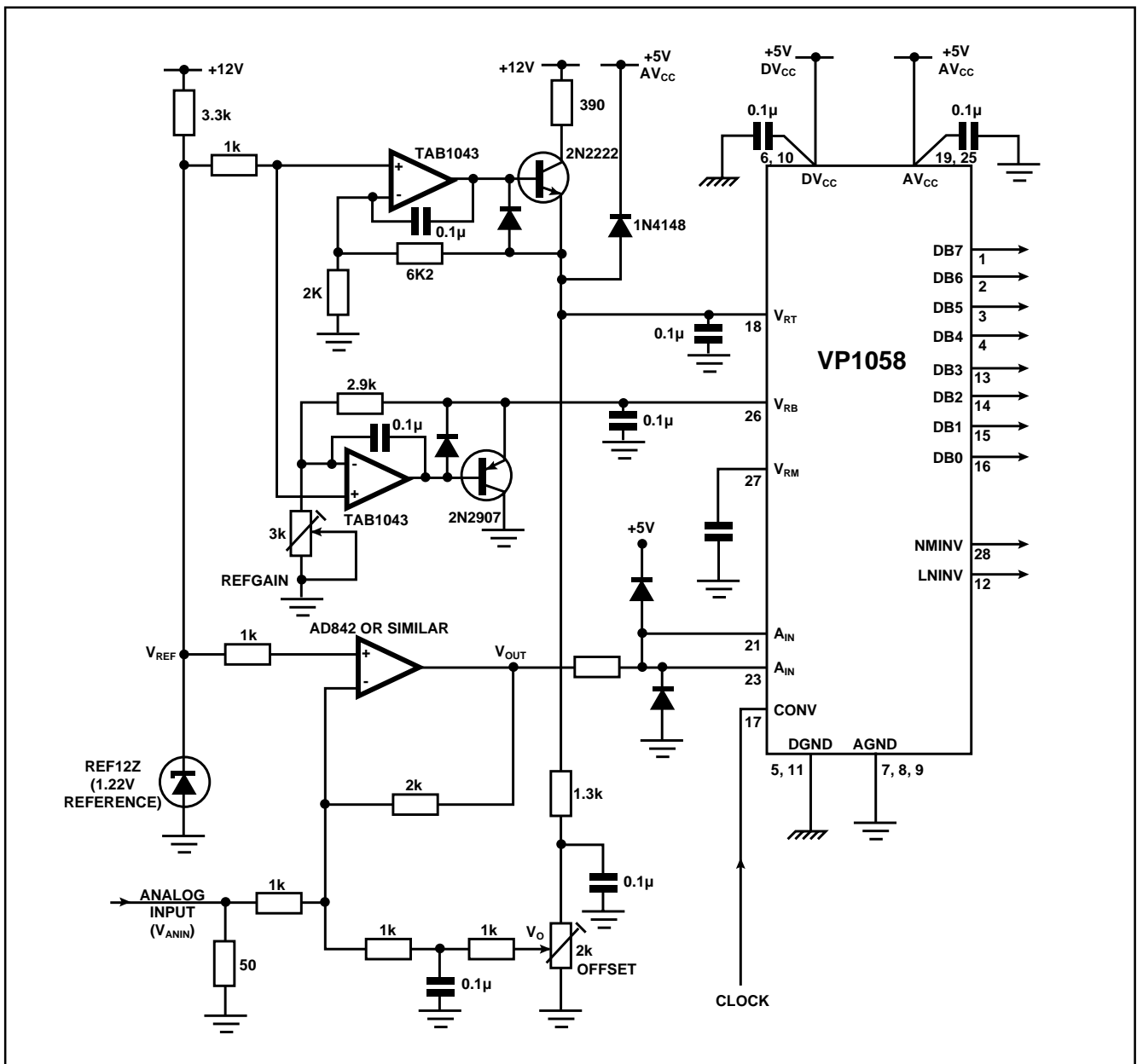


Fig.6 Typical applications circuit



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