

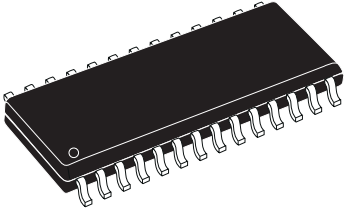


## QUAD CHANNEL HIGH SIDE DRIVER

TYPE	R <sub>DS(on)</sub>	I <sub>OUT</sub>	V <sub>CC</sub>
VNQ810	160 mΩ (*)	3.5 A (*)	36 V

(\*) Per each channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (\*\*)



**SO-28 (DOUBLE ISLAND)**

ORDER CODES		
PACKAGE	TUBE	T&R
SO-28	VNQ810	VNQ81013TR

### DESCRIPTION

The VNQ810 is a quad HSD formed by assembling two VND810 chips in the same SO-28 package. The VND810 is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V<sub>CC</sub> pin voltage clamp protects the device

against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off state. Output shorted to V<sub>CC</sub> is detected in the off state. Device automatically turns off in case of ground pin disconnection.

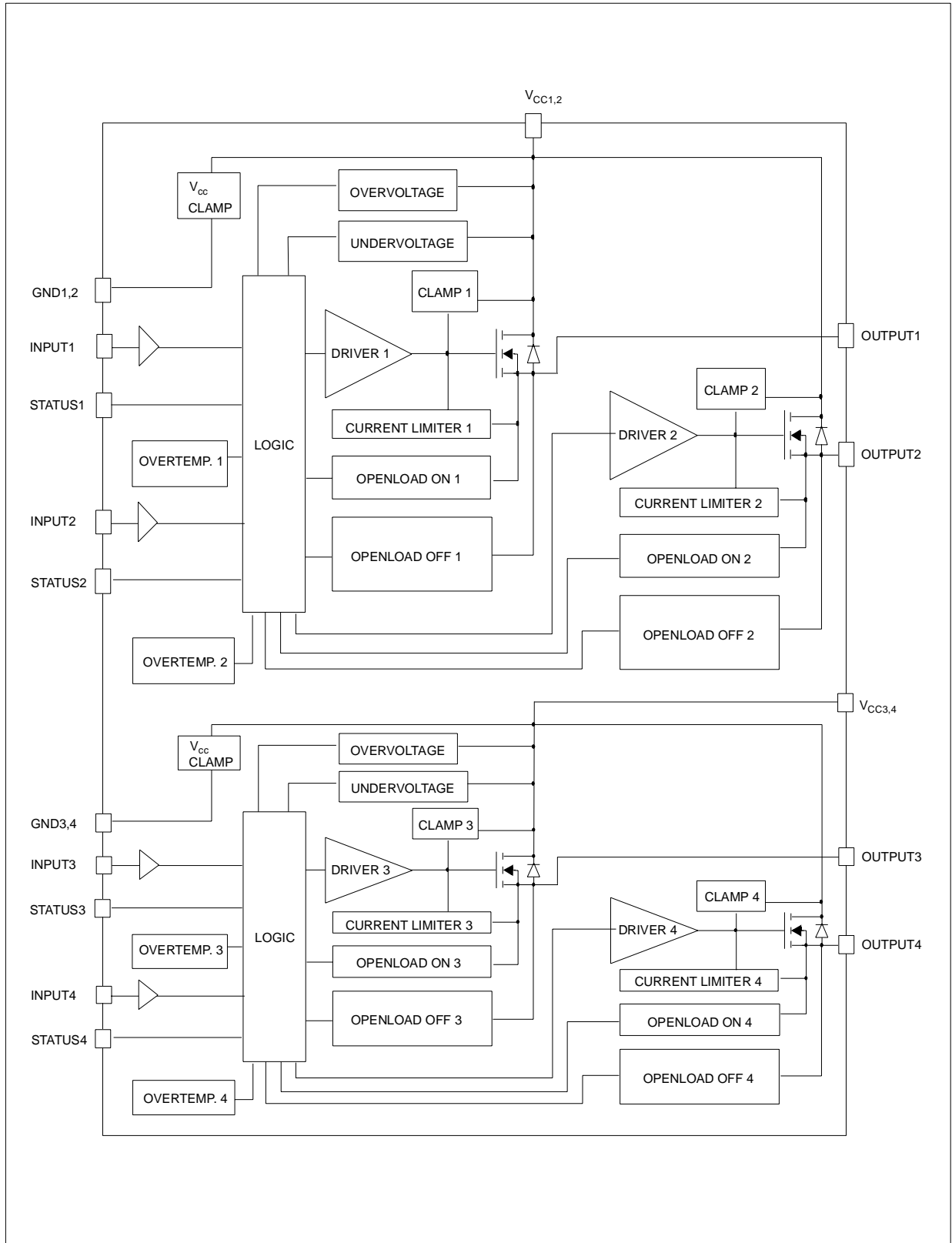
### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	41	V
-V <sub>CC</sub>	Reverse DC Supply Voltage	- 0.3	V
- I <sub>gnd</sub>	DC Reverse Ground Pin Current	- 200	mA
I <sub>OUT</sub>	DC Output Current	Internally Limited	A
- I <sub>OUT</sub>	Reverse DC Output Current	- 6	A
I <sub>IN</sub>	DC Input Current	+/- 10	mA
I <sub>STAT</sub>	DC Status Current	+/- 10	mA
V <sub>ESD</sub>	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V <sub>CC</sub>	5000	V
E <sub>MAX</sub>	Maximum Switching Energy (L=1.38mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =5A)	23	mJ
P <sub>tot</sub>	Power dissipation (per island) at T <sub>lead</sub> =25°C	6.25	W
T <sub>j</sub>	Junction Operating Temperature	Internally Limited	°C
T <sub>stg</sub>	Storage Temperature	- 55 to 150	°C

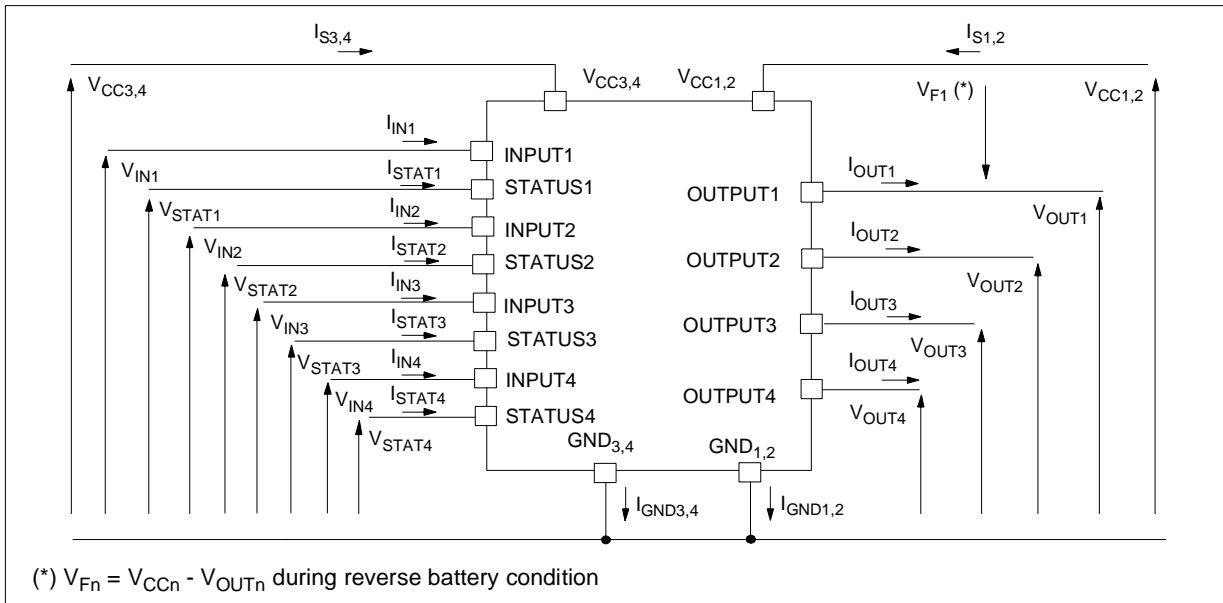
(\*\*) See application schematic at page 9

Rev. 1

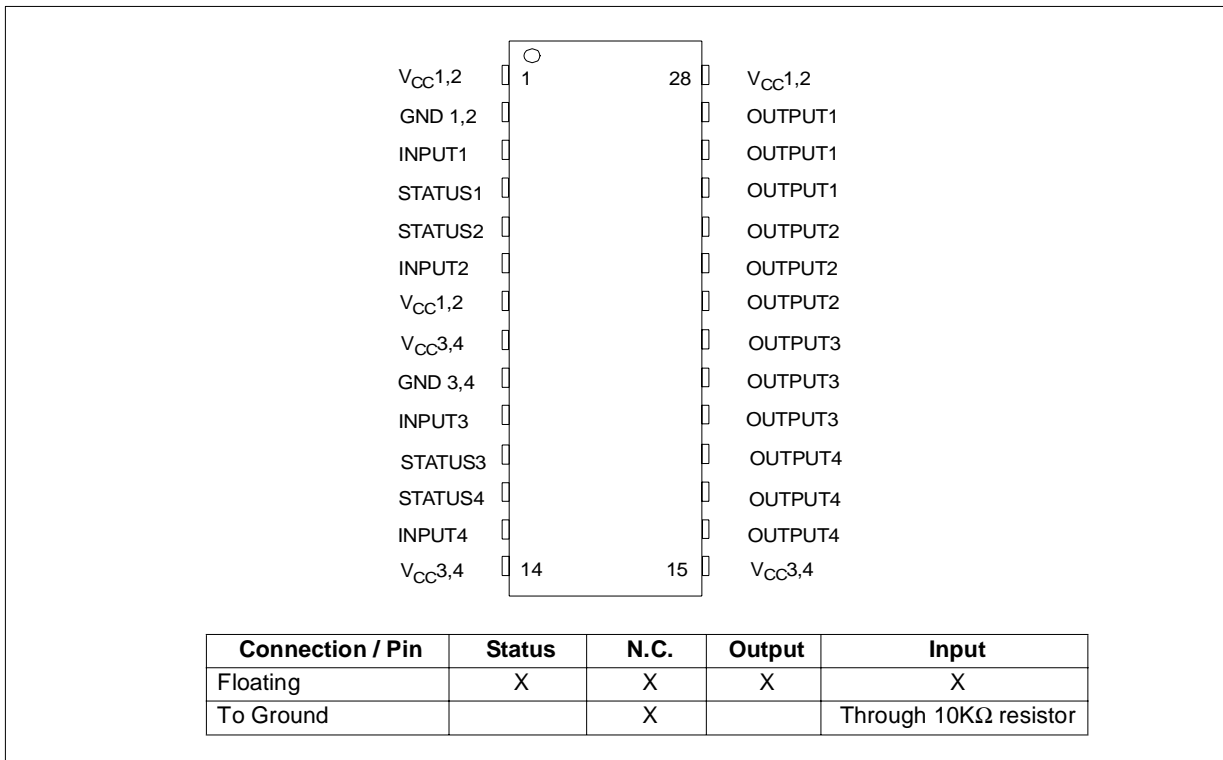
BLOCK DIAGRAM



**CURRENT AND VOLTAGE CONVENTIONS**



**CONFIGURATION DIAGRAM (TOP VIEW) & SUGGESTED CONNECTIONS FOR UNUSED AND N.C. PINS**



## VNQ810

### THERMAL DATA (Per island)

Symbol	Parameter	Value		Unit
R <sub>thj-lead</sub>	Thermal Resistance Junction-lead per chip	20		°C/W
R <sub>thj-amb</sub>	Thermal resistance Junction-ambient (one chip ON)	60 <sup>(1)</sup>	44 <sup>(2)</sup>	°C/W
R <sub>thj-amb</sub>	Thermal resistance Junction-ambient (two chips ON)	46 <sup>(1)</sup>	31 <sup>(2)</sup>	°C/W

(1) When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

(2) When mounted on a standard single-sided FR-4 board with 6cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

### ELECTRICAL CHARACTERISTICS (8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified) POWER OUTPUTS (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CC</sub> (**)	Operating Supply Voltage		5.5	13	36	V
V <sub>USD</sub> (**)	Undervoltage Shut-down		3	4	5.5	V
V <sub>OV</sub> (**)	Overvoltage Shut-down		36			V
R <sub>ON</sub>	On State Resistance	I <sub>OUT</sub> =1A; T <sub>j</sub> =25°C I <sub>OUT</sub> =1A; V <sub>CC</sub> >8V			160 320	mΩ mΩ
I <sub>S</sub> (**)	Supply Current	Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V; T <sub>j</sub> =25°C On State; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V; I <sub>OUT</sub> =0A		12 12 5	40 25 7	µA µA mA
I <sub>L(off1)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V	0		50	µA
I <sub>L(off2)</sub>	Off State Output Current	V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5V	-75		0	µA
I <sub>L(off3)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C			5	µA
I <sub>L(off4)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C			3	µA

(\*\*) Per island

### SWITCHING (Per each Channel) (V<sub>CC</sub>=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	R <sub>L</sub> =13Ω from V <sub>IN</sub> rising edge to V <sub>OUT</sub> =1.3V		30		µs
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>L</sub> =13Ω from V <sub>IN</sub> falling edge to V <sub>OUT</sub> =11.7V		30		µs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on Voltage Slope	R <sub>L</sub> =13Ω from V <sub>OUT</sub> =1.3V to V <sub>OUT</sub> =10.4V		See relative diagram		V/µs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off Voltage Slope	R <sub>L</sub> =13Ω from V <sub>OUT</sub> =11.7V to V <sub>OUT</sub> =1.3V		See relative diagram		V/µs

### V<sub>CC</sub> - OUTPUT DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>F</sub>	Forward on Voltage	-I <sub>OUT</sub> =0.5A; T <sub>j</sub> =150°C			0.6	V

**ELECTRICAL CHARACTERISTICS** (continued)

## LOGIC INPUT (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input Low Level				1.25	V
$I_{IL}$	Low Level Input Current	$V_{IN}=1.25V$	1			$\mu A$
$V_{IH}$	Input High Level		3.25			V
$I_{IH}$	High Level Input Current	$V_{IN}=3.25V$			10	$\mu A$
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
$V_{ICL}$	Input Clamp Voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6	6.8 -0.7	8	V V

## STATUS PIN (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status Low Output Voltage	$I_{STAT}=1.6mA$			0.5	V
$I_{LSTAT}$	Status Leakage Current	Normal Operation; $V_{STAT}=5V$			10	$\mu A$
$C_{STAT}$	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5V$			100	pF
$V_{SCL}$	Status Clamp Voltage	$I_{STAT}=1mA$ $I_{STAT}=-1mA$	6	6.8 -0.7	8	V V

## PROTECTIONS (Per each channel) (see note 1)

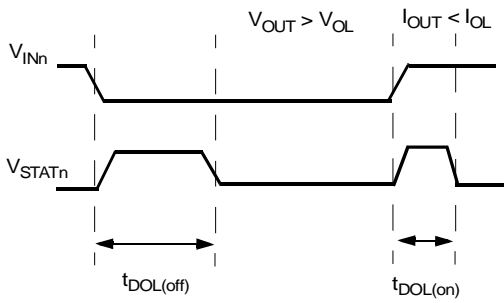
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shut-down Temperature		150	175	200	$^{\circ}C$
$T_R$	Reset Temperature		135			$^{\circ}C$
$T_{hyst}$	Thermal Hysteresis		7	15		$^{\circ}C$
$t_{sdl}$	Status Delay in Overload Conditions	$T_j > T_{TSD}$			20	$\mu s$
$I_{lim}$	Current limitation	$5.5V < V_{CC} < 36V$	3.5	5	7.5 7.5	A A
$V_{DEMAG}$	Turn-off Output Clamp Voltage	$I_{OUT}=1A$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

Note 1: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

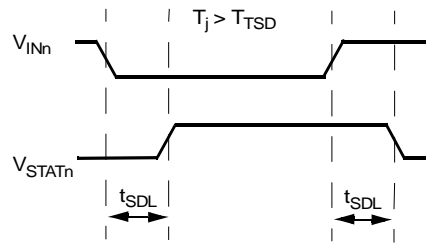
## OPENLOAD DETECTION (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{OL}$	Openload ON State Detection Threshold	$V_{IN}=5V$	20	40	80	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0A$			200	$\mu s$
$V_{OL}$	Openload OFF State Voltage Detection Threshold	$V_{IN}=0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	$\mu s$

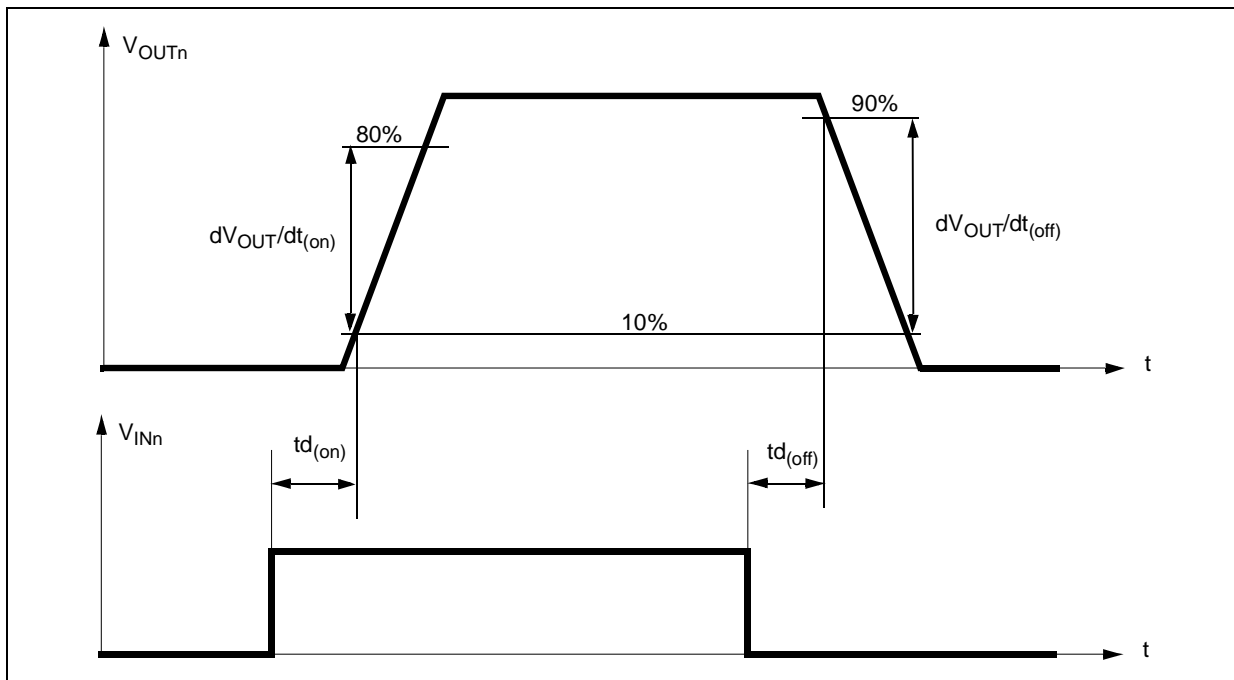
OPEN LOAD STATUS TIMING (with external pull-up)



OVER TEMP STATUS TIMING



SWITCHING TIME WAVEFORMS



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	( $T_j < T_{TSD}$ ) H ( $T_j > T_{TSD}$ ) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage > $V_{OL}$	L	H	L
	H	H	H
Output Current < $I_{OL}$	L	L	H
	H	H	L

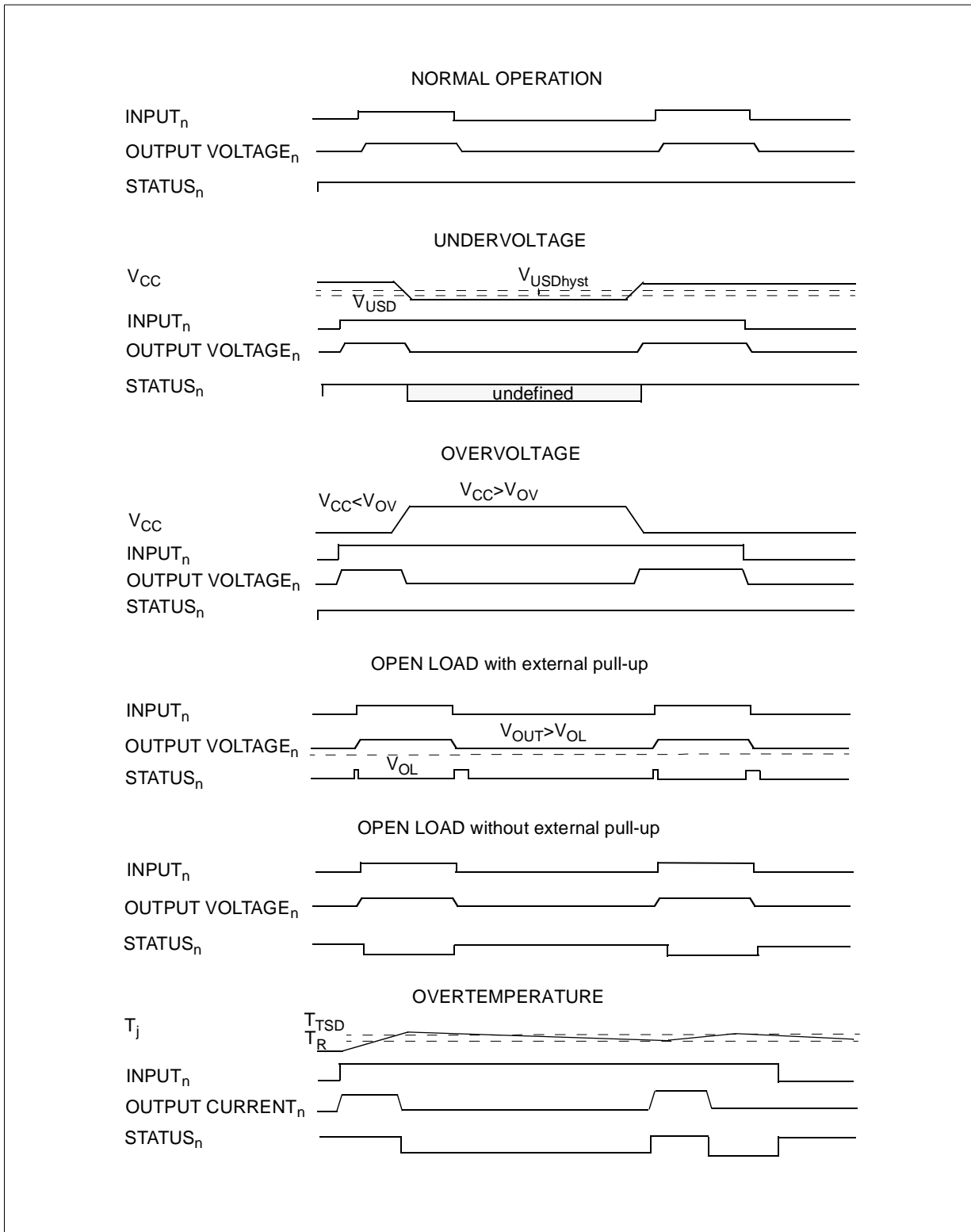
ELECTRICAL TRANSIENT REQUIREMENTS ON V<sub>CC</sub> PIN

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

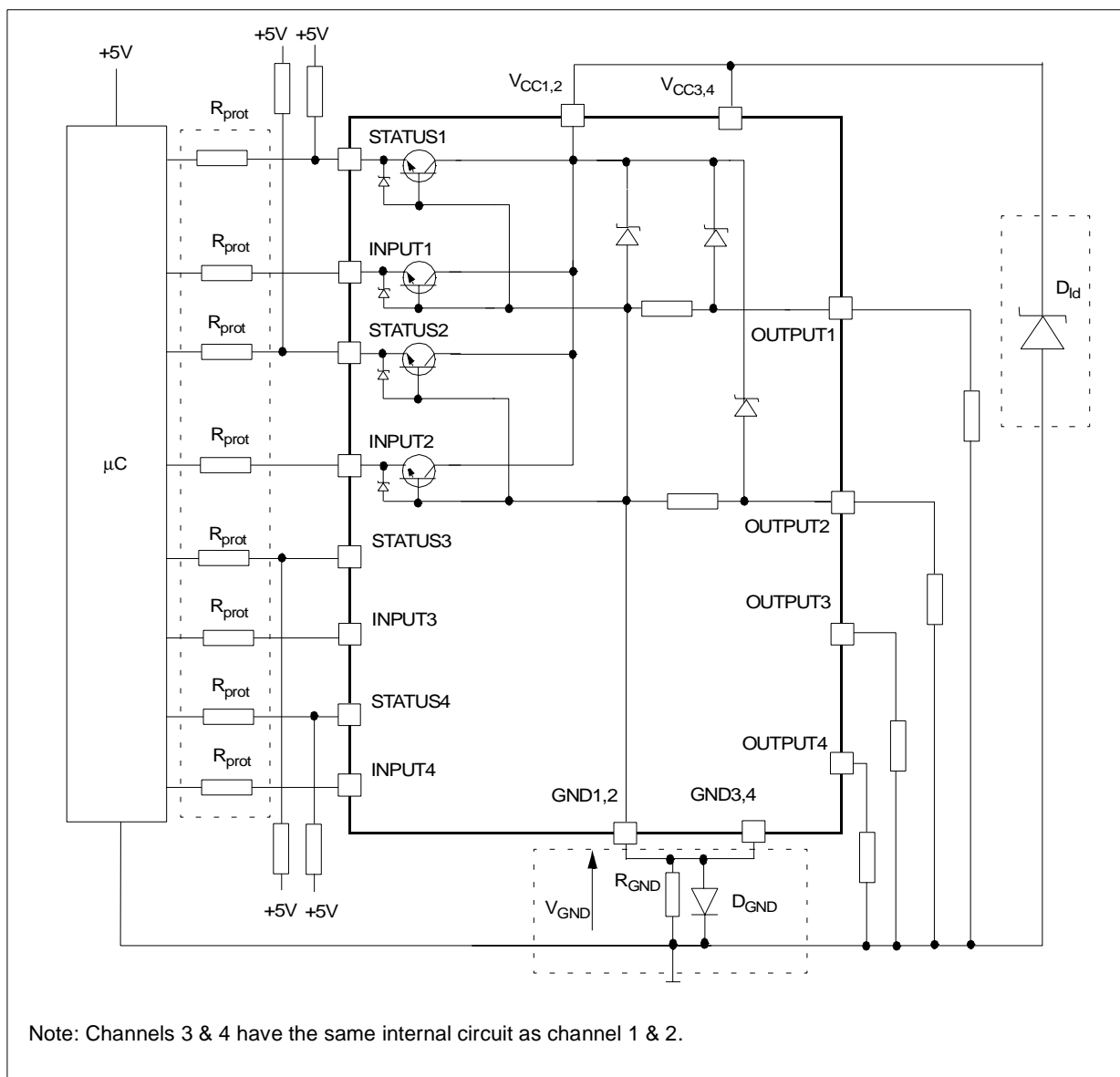
CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 1: Waveforms





## APPLICATION SCHEMATIC

**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

Solution 1: Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600\text{mV} / 2(I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggest to utilize Solution 2.

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND}=1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

### LOAD DUMP PROTECTION

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The

same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

### $\mu C$ I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$   
Calculation example:

For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$   
 $5k\Omega \leq R_{prot} \leq 65k\Omega$ .

Recommended  $R_{prot}$  value is  $10k\Omega$ .

## OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1) no false open load indication when load is connected:

in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition

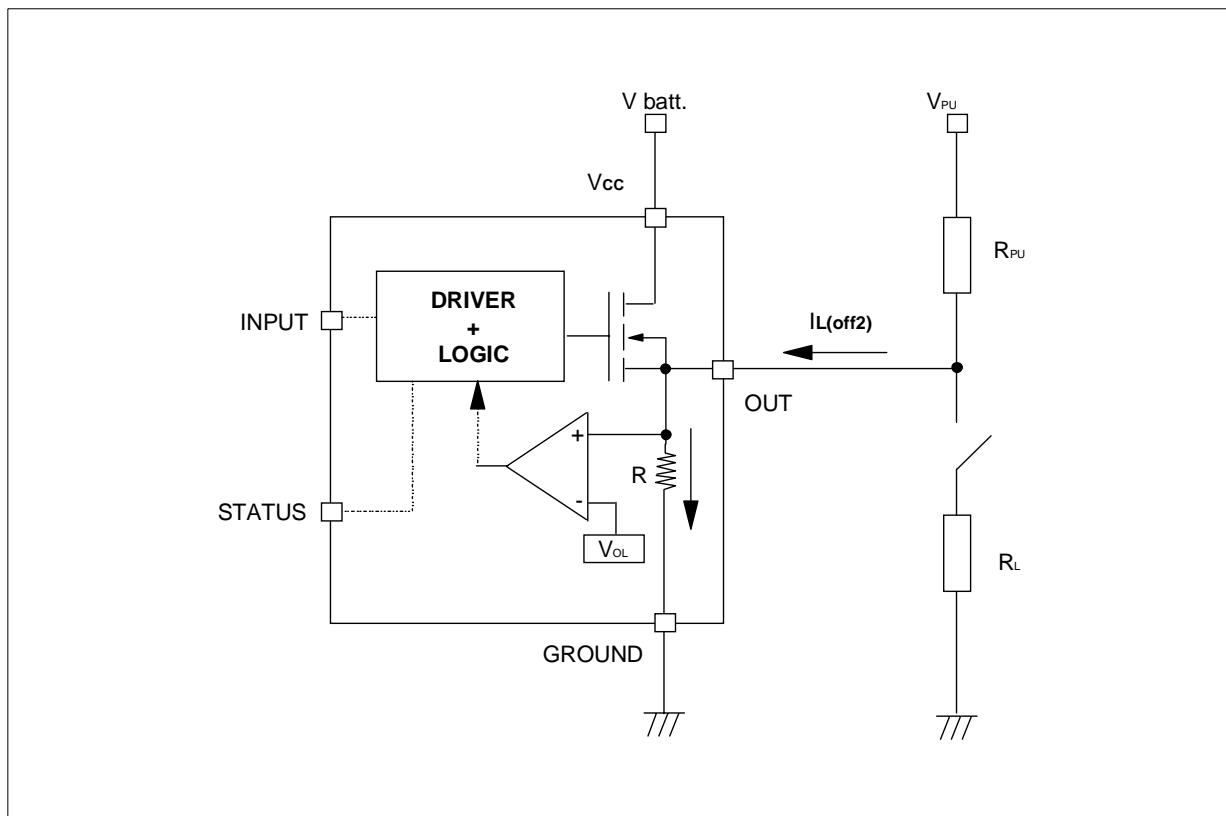
$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$ .

2) no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .

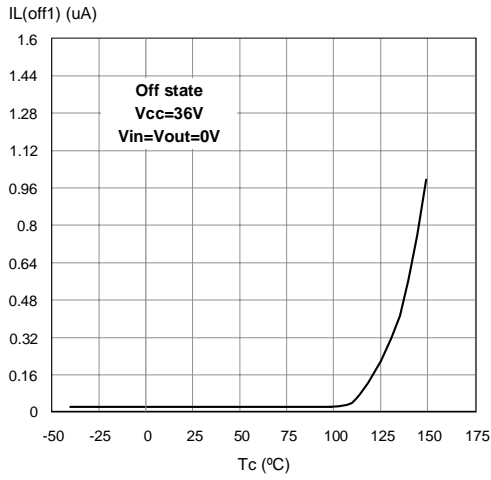
Because  $I_{S(OFF)}$  may significantly increase if  $V_{out}$  is pulled high (up to several mA), the pull-up resistor  $R_{PU}$  should be connected to a supply that is switched OFF when the module is in standby.

The values of  $V_{OLmin}$ ,  $V_{OLmax}$  and  $I_{L(off2)}$  are available in the Electrical Characteristics section.

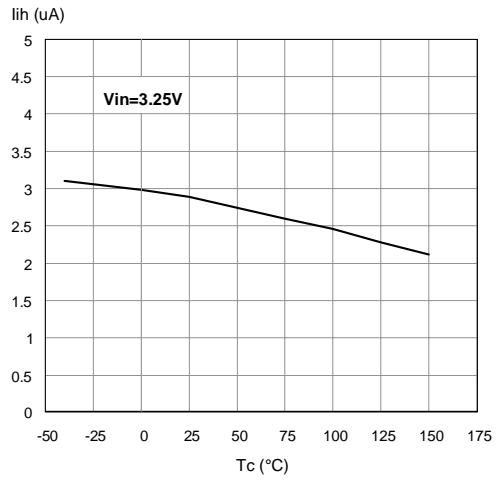
### Open Load detection in off state



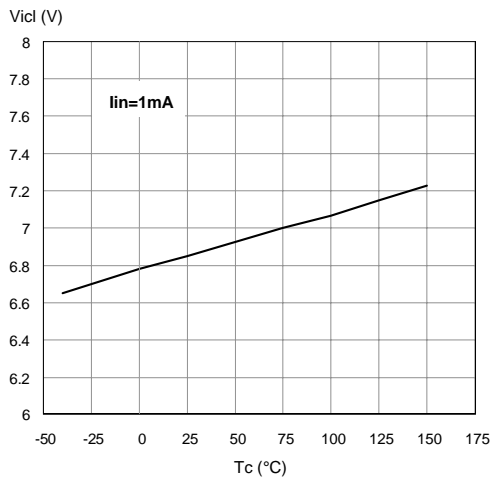
Off State Output Current



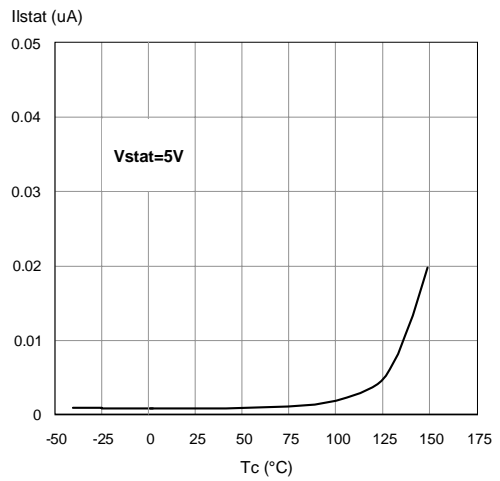
High Level Input Current



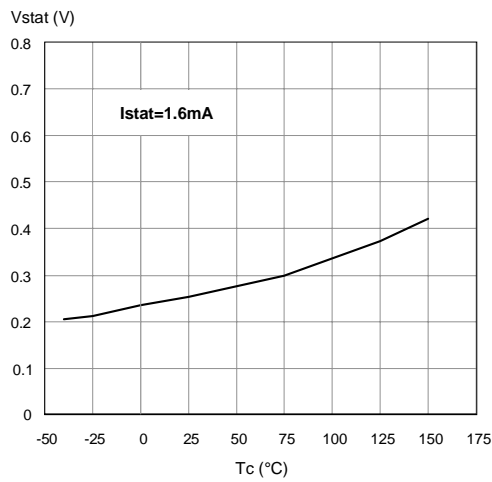
Input Clamp Voltage



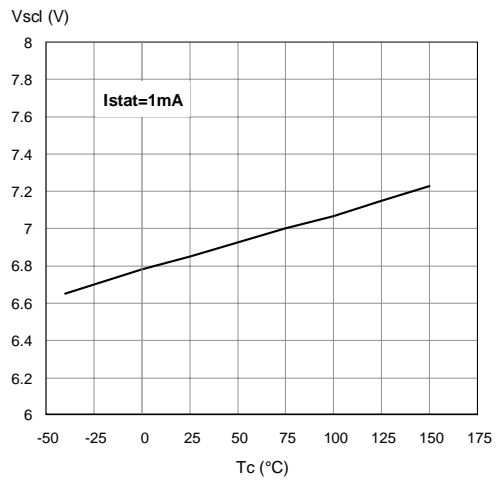
Status Leakage Current



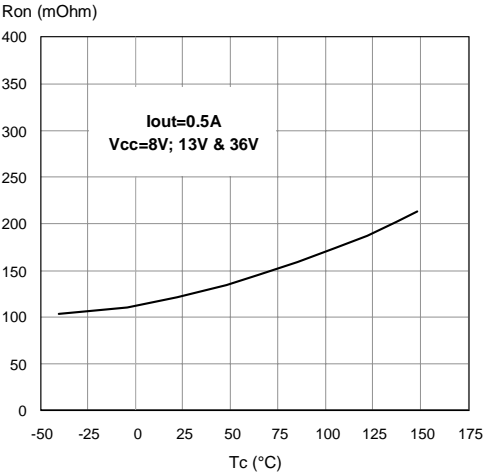
Status Low Output Voltage



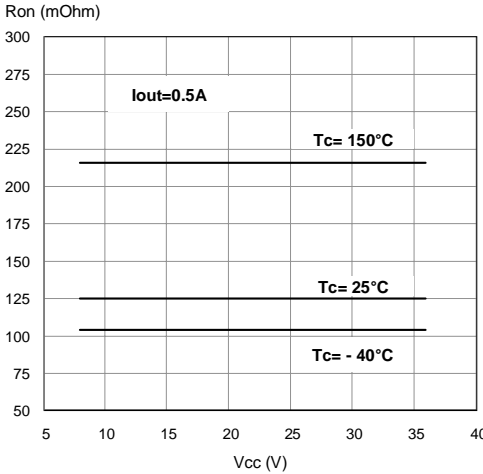
Status Clamp Voltage



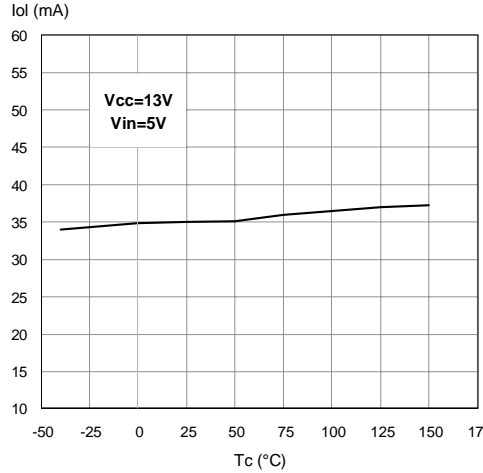
On State Resistance Vs  $T_{case}$



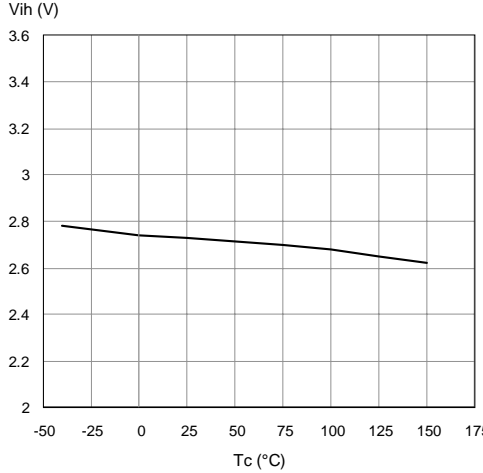
On State Resistance Vs  $V_{CC}$



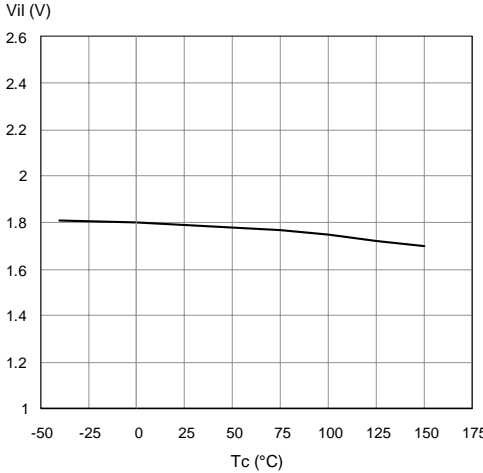
Openload On State Detection Threshold



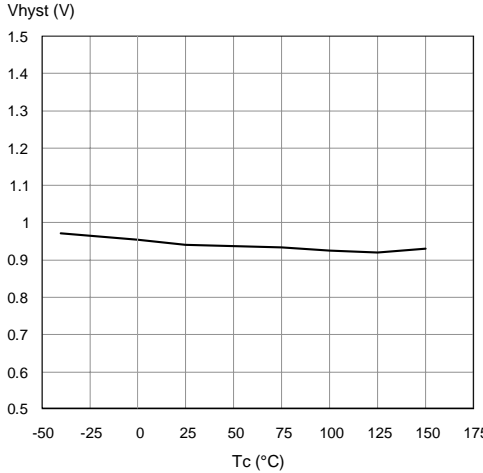
Input High Level



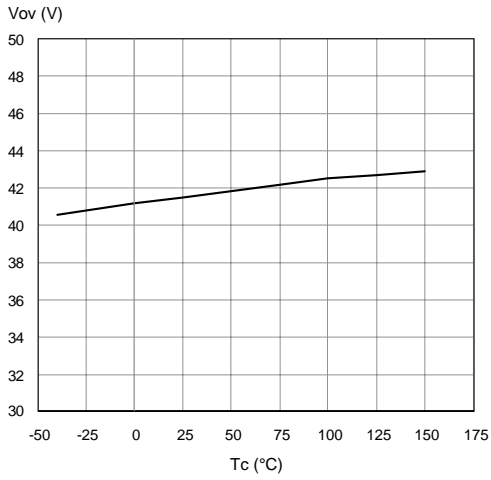
Input Low Level



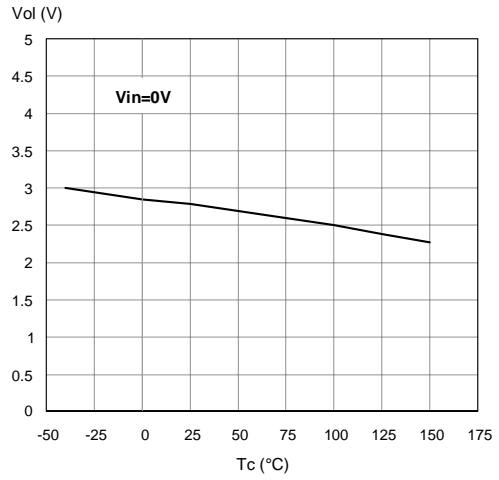
Input Hysteresis Voltage



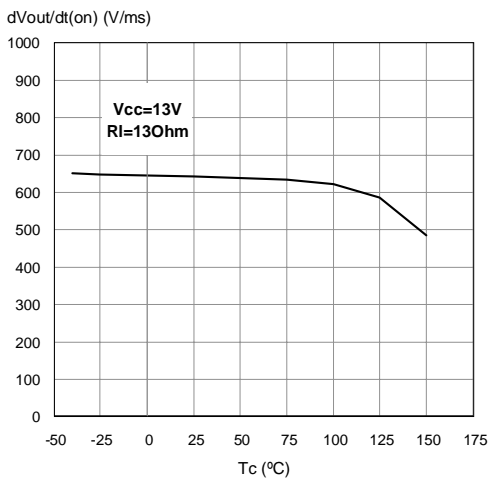
Overvoltage Shutdown



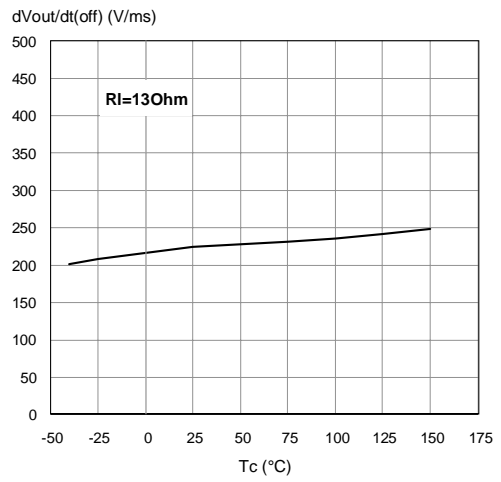
Openload Off State Voltage Detection Threshold



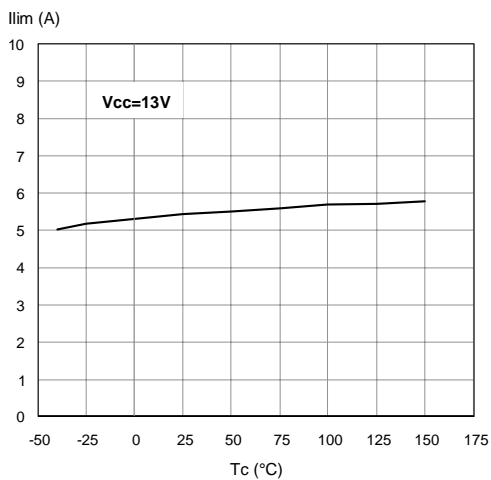
Turn-on Voltage Slope



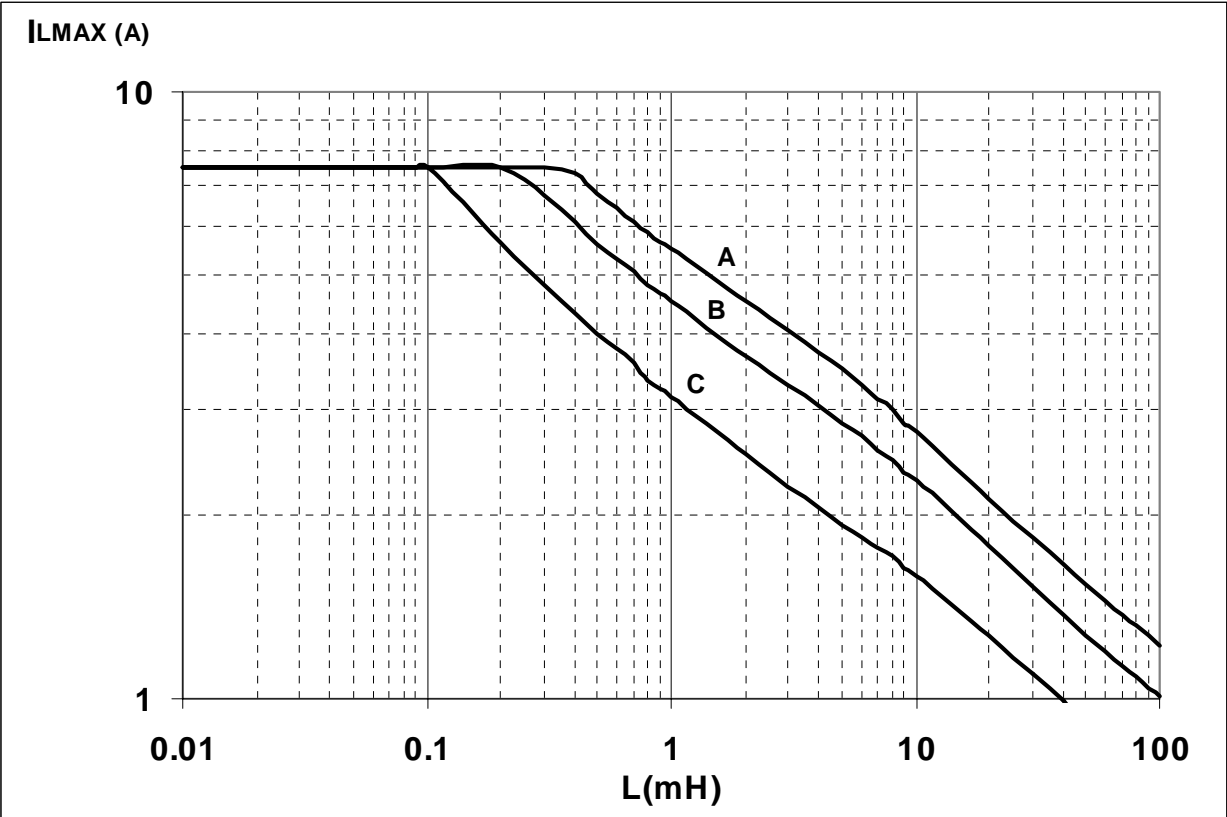
Turn-off Voltage Slope



I<sub>LIM</sub> Vs T<sub>case</sub>



Maximum turn off current versus load inductance



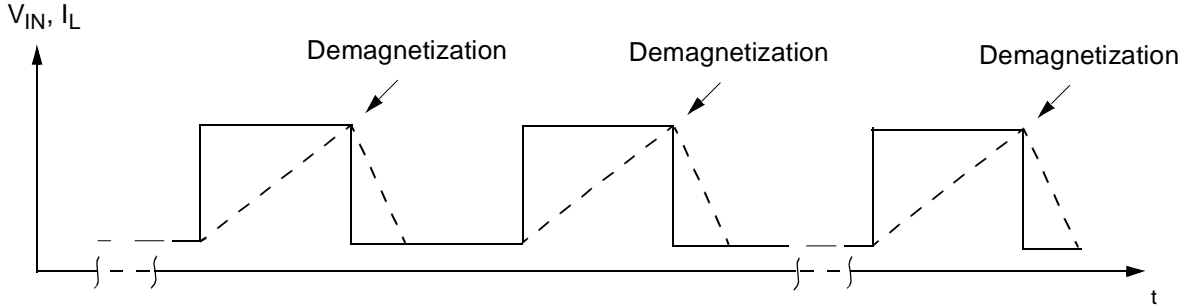
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

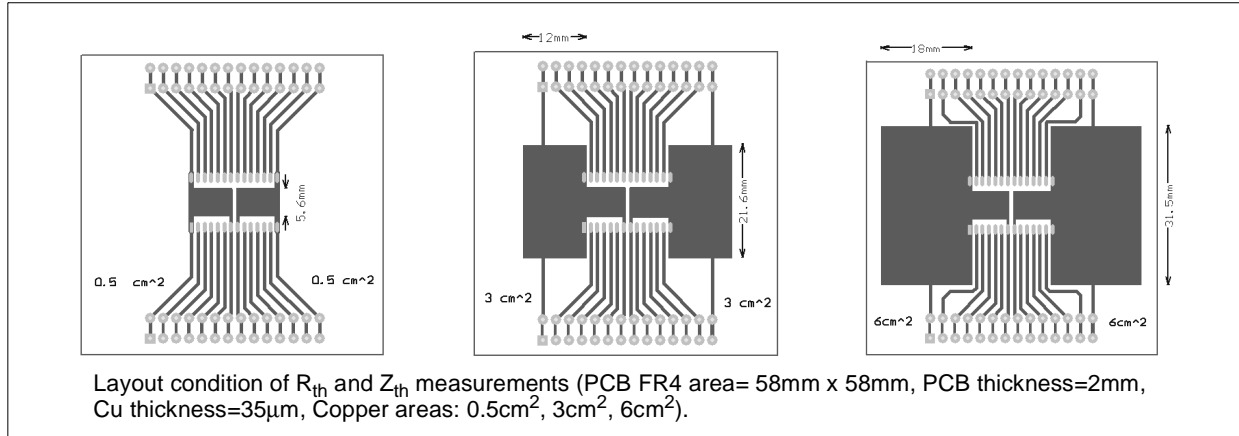
Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



**SO-28 DOUBLE ISLAND THERMAL DATA**

**SO-28 Double island PC Board**

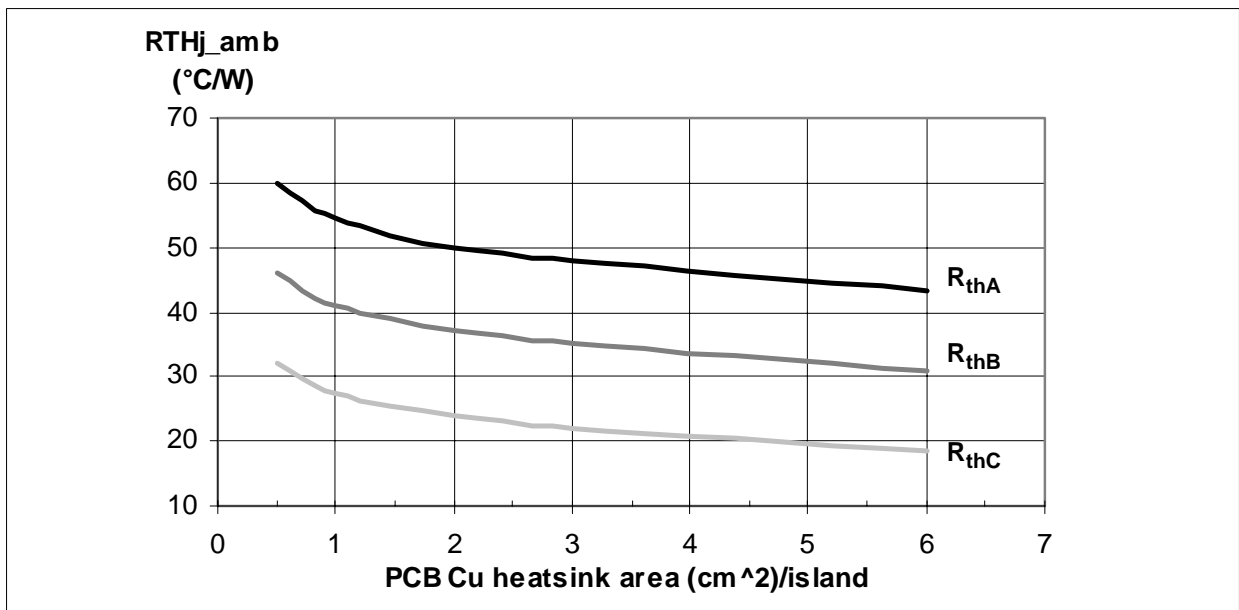


**Thermal calculation according to the PCB heatsink area**

Chip 1	Chip 2	$T_{jchip1}$	$T_{jchip2}$	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

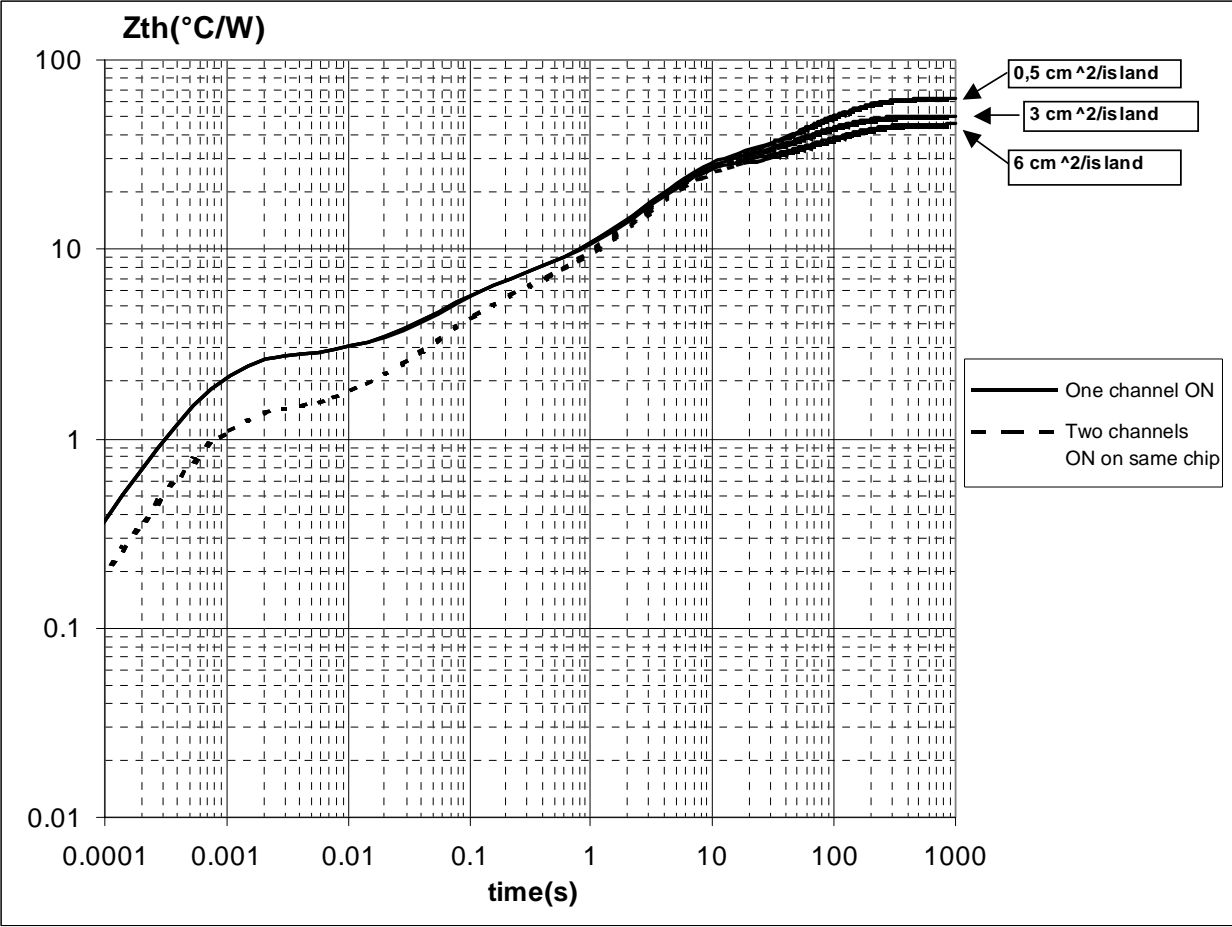
$R_{thA}$  = Thermal resistance Junction to Ambient with one chip ON  
 $R_{thB}$  = Thermal resistance Junction to Ambient with both chips ON and  $P_{dchip1} = P_{dchip2}$   
 $R_{thC}$  = Mutual thermal resistance

**$R_{thj-amb}$  Vs. PCB copper area in open box free air condition**

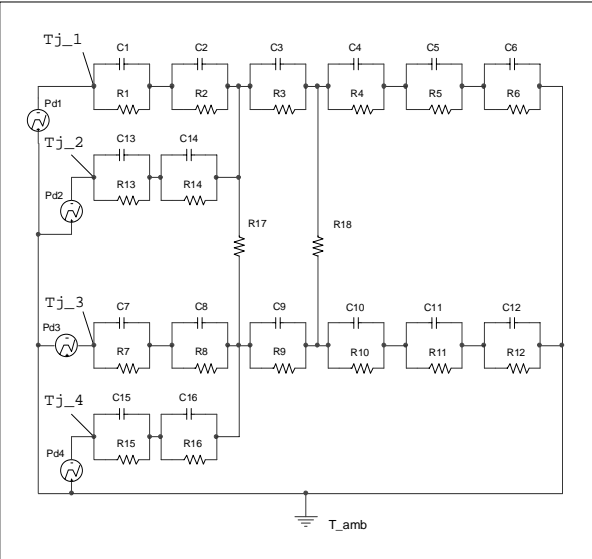




SO-28 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a four channels HSD in SO-28



Pulse calculation formula  
 $Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$

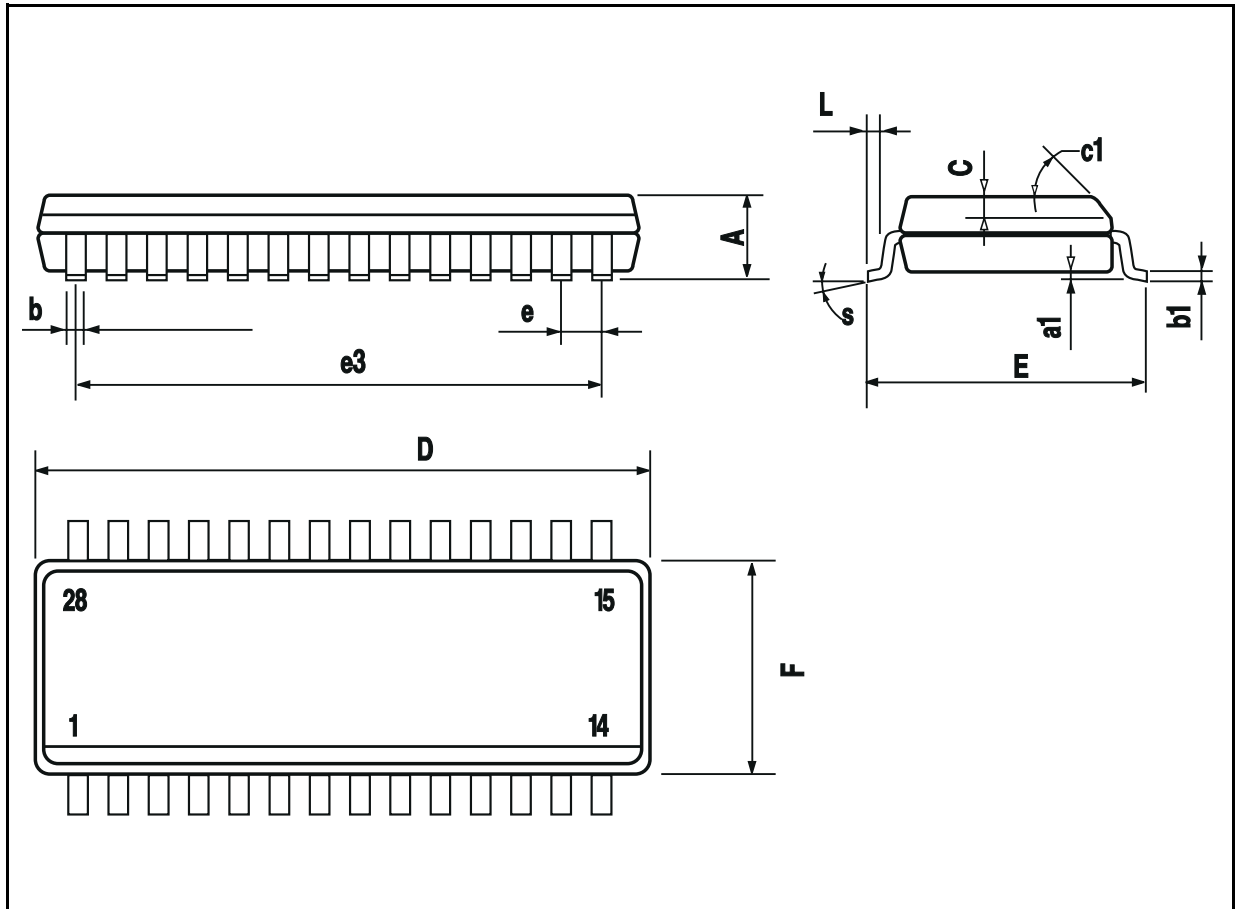
where  $\delta = t_p/T$   
**Thermal Parameter**

Area/island (cm <sup>2</sup> )	0.5	6
R1=R7=R13=R15 (°C/W)	0.35	
R2=R8=R14=R16 (°C/W)	1.8	
R3=R9 (°C/W)	4.5	
R4=R10 (°C/W)	11	
R5=R11 (°C/W)	15	
R6=R12 (°C/W)	30	13
C1=C7=C13=C15 (W.s/°C)	0.0001	
C2=C8=C14=C16 (W.s/°C)	7.00E-04	
C3=C9 (W.s/°C)	6.00E-03	
C4=C10 (W.s/°C)	0.2	
C5=C11 (W.s/°C)	1.5	
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	

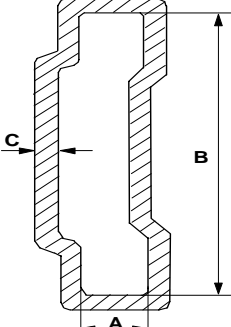


**SO-28 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	17.7		18.1	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
S	8 (max.)					



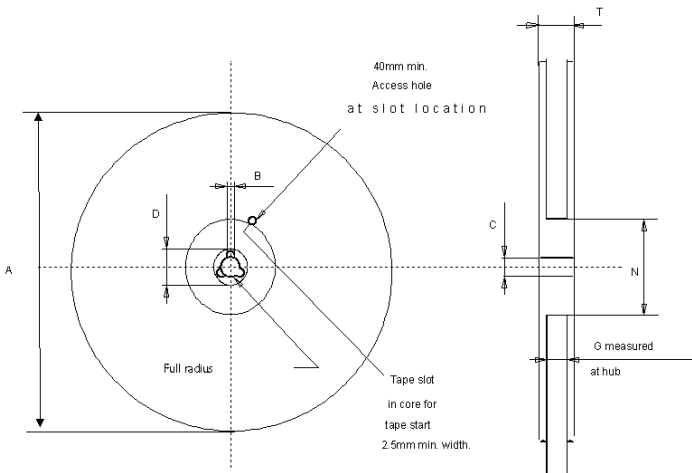
**SO-28 TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	28
<b>Bulk Q.ty</b>	700
<b>Tube length (<math>\pm 0.5</math>)</b>	532
<b>A</b>	3.5
<b>B</b>	13.8
<b>C (<math>\pm 0.1</math>)</b>	0.6

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**

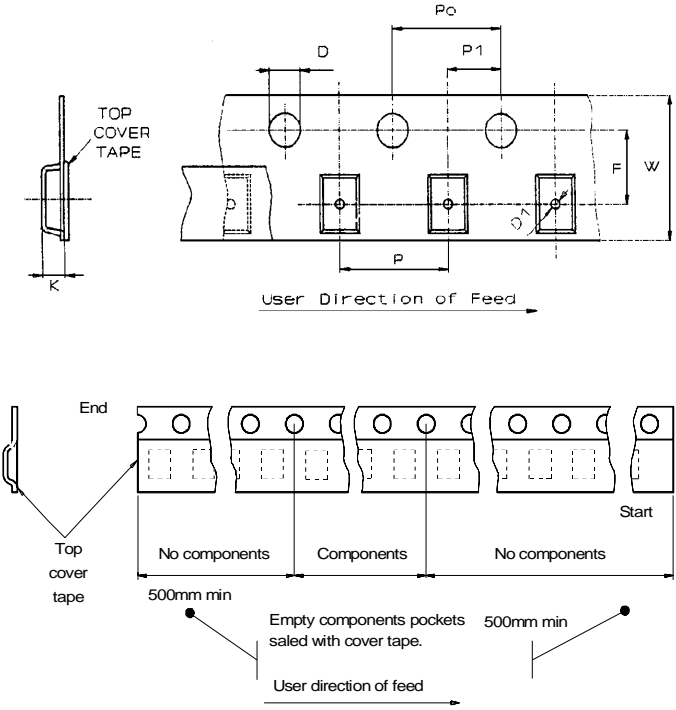


<b>Base Q.ty</b>	1000
<b>Bulk Q.ty</b>	1000
<b>A (max)</b>	330
<b>B (min)</b>	1.5
<b>C (<math>\pm 0.2</math>)</b>	13
<b>F</b>	20.2
<b>G (+ 2 / -0)</b>	16.4
<b>N (min)</b>	60
<b>T (max)</b>	22.4

**TAPE DIMENSIONS**  
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

<b>Tape width</b>	<b>W</b>	16
<b>Tape Hole Spacing</b>	<b>P0 (<math>\pm 0.1</math>)</b>	4
<b>Component Spacing</b>	<b>P</b>	12
<b>Hole Diameter</b>	<b>D (<math>\pm 0.1/-0</math>)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (<math>\pm 0.05</math>)</b>	7.5
<b>Compartment Depth</b>	<b>K (max)</b>	6.5
<b>Hole Spacing</b>	<b>P1 (<math>\pm 0.1</math>)</b>	2



All dimensions are in mm.

**REVISION HISTORY**

Date	Revision	Description of Changes
Jul 2004	1	<ul style="list-style-type: none"><li>- Minor changes</li><li>- Current and voltage convention update (page 3).</li><li>- "Configuration diagram (top view) &amp; suggested connections for unused and n.c. pins" insertion (page 3).</li><li>- 6 cm<sup>2</sup> Cu condition insertion in Thermal Data table (page 4).</li><li>- V<sub>CC</sub> - OUTPUT DIODE section update (page 4).</li><li>- PROTECTIONS note insertion (page 5)</li><li>- Revision History table insertion (page 20).</li><li>- Disclaimers update (page 21).</li></ul>

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