



DOUBLE CHANNEL HIGH SIDE SOLID STATE RELAY

TARGET SPECIFICATION

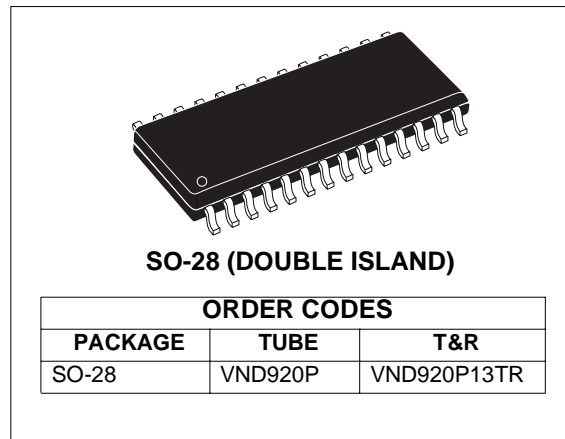
TYPE	R _{DS(on)}	I _{OUT}	V _{CC}
VND920P	16mΩ	35 A (*)	36 V

(*) Per channel with all the output pins connected to the PCB.

- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW STAND-BY POWER DISSIPATION
- REVERSE BATTERY PROTECTION (**)

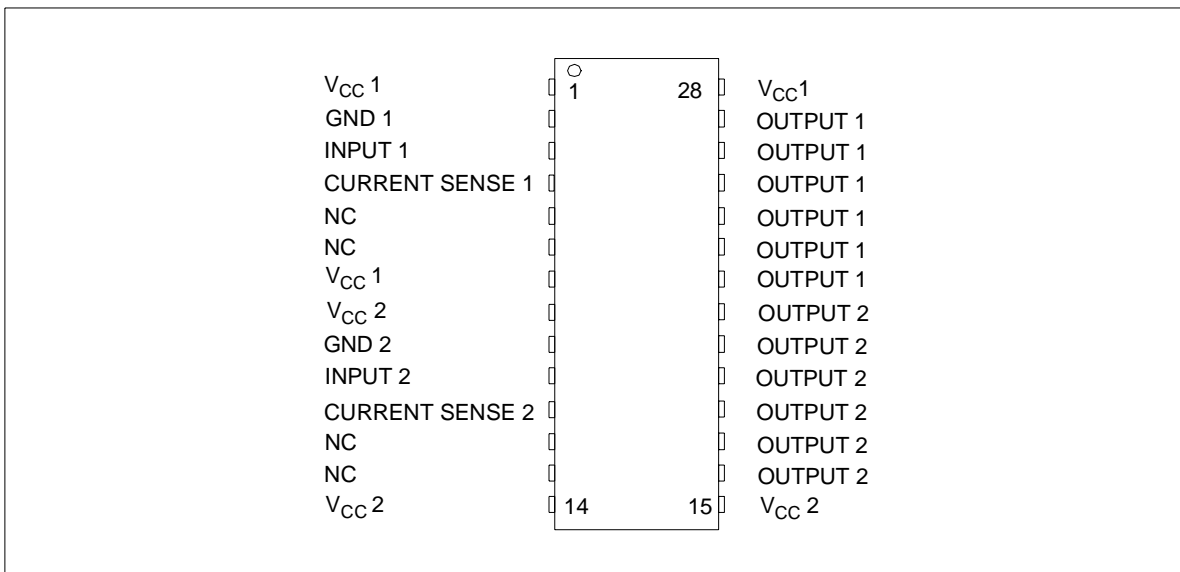
DESCRIPTION

The VND920P is a double chip device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load



with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Built-in analog current sense output delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

CONNECTION DIAGRAM (TOP VIEW)

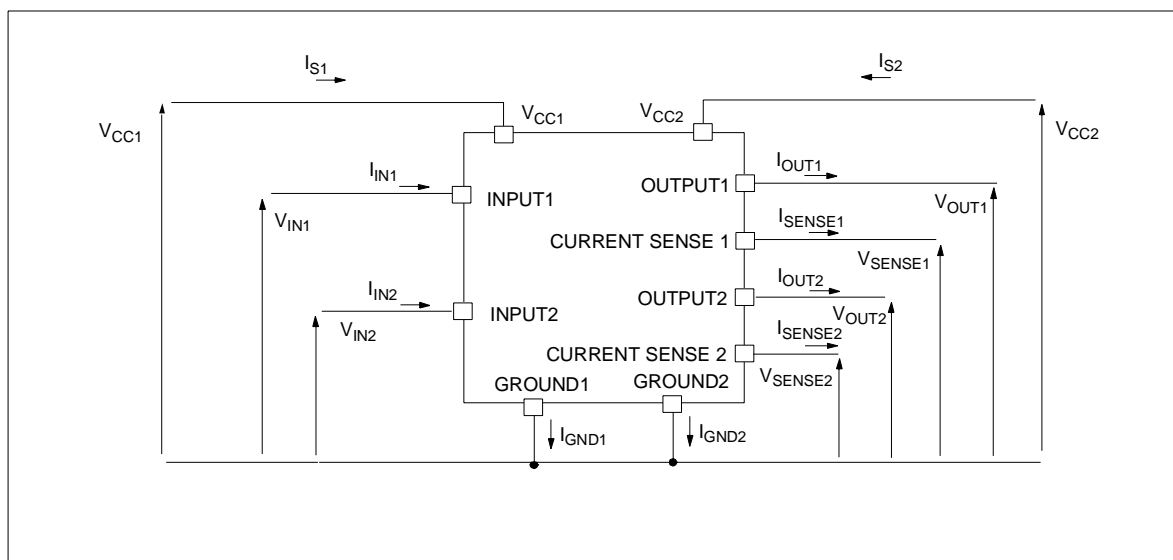


(**) See application schematic at page 10

ABSOLUTE MAXIMUM RATING (Per each channel)

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3	V
$-I_{GND}$	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
$-I_{OUT}$	Reverse DC Output Current	- 21	A
I_{IN}	DC Input Current	+/- 10	mA
V_{CSENSE}	Current Sense Maximum Voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5K Ω ; C=100pF)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	$-V_{CC}$	5000	V
E_{MAX}	Maximum Switching Energy (L=0.25mH; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=45A$)	355	mJ
P_{tot}	Power Dissipation $T_I \leq 25^\circ C$	6.25 (**)	W
T_j	Junction Operating Temperature	Internally limited	$^\circ C$
T_c	Case Operating Temperature	- 40 to 150	$^\circ C$
T_{STG}	Storage Temperature	- 55 to 150	$^\circ C$

(**) Per island

CURRENT AND VOLTAGE CONVENTIONS

VND920P

THERMAL DATA (Per island)

Symbol	Parameter	Value	Unit
$R_{thj-lead}$	Thermal Resistance Junction-lead	20	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient (one chip ON)	55 (*)	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient (two chips ON)	42 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 1cm² of Cu (at least 35µm thick) connected to all V_{CC} pins.
Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V < V_{CC} < 36V; -40°C < T_j < 150°C unless otherwise specified)

(Per island)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Operating Supply Voltage		5.5	13	36	V
V _{USD}	Undervoltage Shut-down		3	4	5.5	V
V _{OV}	Overvoltage Shut-down		36			V
R _{ON}	On State Resistance	I _{OUT} =10A; T _j =25°C			16	mΩ
		I _{OUT} =10A			32	mΩ
		I _{OUT} =3A; V _{CC} =6V			55	mΩ
V _{clamp}	Clamp Voltage	I _{CC} =20mA (See note 1)	41	48	55	V
I _S	Supply Current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V		10	25	µA
		Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C		10	20	µA
		On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A; R _{SENSE} =3.9KΩ				5
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0		50	µA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	µA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	µA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	µA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	R _L =1.3Ω (see figure 2)		50		µs
t _{d(off)}	Turn-off Delay Time	R _L =1.3Ω (see figure 2)		50		µs
dV _{OUT} /dt _(on)	Turn-on Voltage Slope	R _L =1.3Ω (see figure 2)		See relative diagram		V/µs
dV _{OUT} /dt _(off)	Turn-off Voltage Slope	R _L =1.3Ω (see figure 2)		See relative diagram		V/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IL}	Input Low Level				1.25	V
I _{IL}	Low Level Input Current	V _{IN} =1.25V	1			µA
V _{IH}	Input High Level		3.25			V
I _{IH}	High Level Input Current	V _{IN} =3.25V			10	µA
V _{I(hyst)}	Input Hysteresis Voltage		0.5			V
V _{ICL}	Input Clamp Voltage	I _{IN} =1mA	6	6.8	8	V
		I _{IN} =-1mA		-0.7		V

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

ELECTRICAL CHARACTERISTICS (continued)CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See Fig.1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	$I_{OUT}=1A; V_{SENSE}=0.5V;$ $T_j = -40^\circ C \dots 150^\circ C$	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	$I_{OUT}=1A; V_{SENSE}=0.5V;$ $T_j = -40^\circ C \dots +150^\circ C$	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT}=10A; V_{SENSE}=4V; T_j=-40^\circ C$ $T_j=25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	$I_{OUT}=10A; V_{SENSE}=4V;$ $T_j=-40^\circ C \dots +150^\circ C$	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT}=30A; V_{SENSE}=4V; T_j=-40^\circ C$ $T_j=25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	$I_{OUT}=30A; V_{SENSE}=4V;$ $T_j=-40^\circ C \dots +150^\circ C$	-6		+6	%
I_{SENSE0}	Analog Sense Leakage Current	$V_{CC}=6 \dots 16V; I_{OUT}=0A; V_{SENSE}=0V;$ $T_j=-40^\circ C \dots +150^\circ C$	0		10	μA
V_{SENSE}	Max Analog Sense Output Voltage	$V_{CC}=5.5V; I_{OUT}=5A; R_{SENSE}=10K\Omega$ $V_{CC}>8V; I_{OUT}=10A; R_{SENSE}=10K\Omega$	2 4			V V
V_{SENSEH}	Sense Voltage in Overtemperature conditions	$V_{CC}=13V; R_{SENSE}=3.9K\Omega$		5.5		V
$R_{VSENSEH}$	Analog Sense Output Impedance in Overtemperature Condition	$V_{CC}=13V; T_j>T_{TSD};$ All channels open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 2)			500	μs

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^\circ C$
T_R	Reset Temperature		135			$^\circ C$
T_{hyst}	Thermal Hysteresis		7	15		$^\circ C$
I_{lim}	DC Short Circuit Current	$V_{CC}=13V$ $5V < V_{CC} < 36V$	30	45	75 75	A A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=2A; V_{IN}=0V; L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
V_{ON}	Output Voltage Drop Limitation	$I_{OUT}=1A; T_j=-40^\circ C \dots +150^\circ C$		50		mV

Note 2: current sense signal delay after positive input slope

Note: Sense pin doesn't have to be left floating.

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Figure 1: I_{OUT}/I_{SENSE} versus I_{OUT}

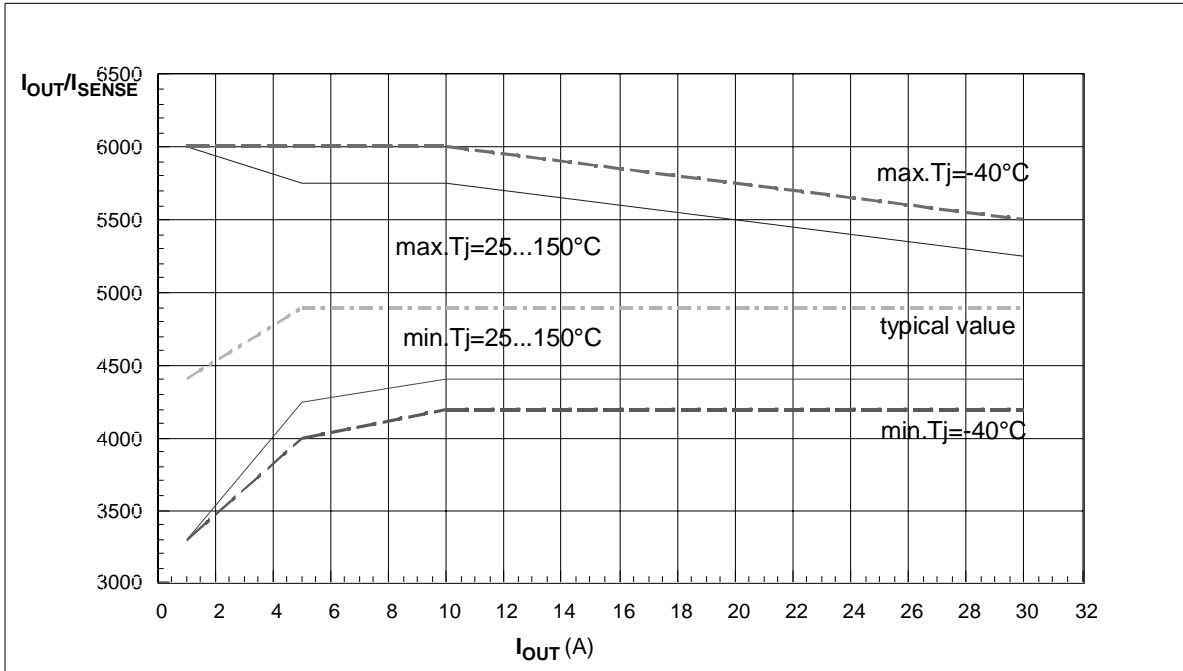
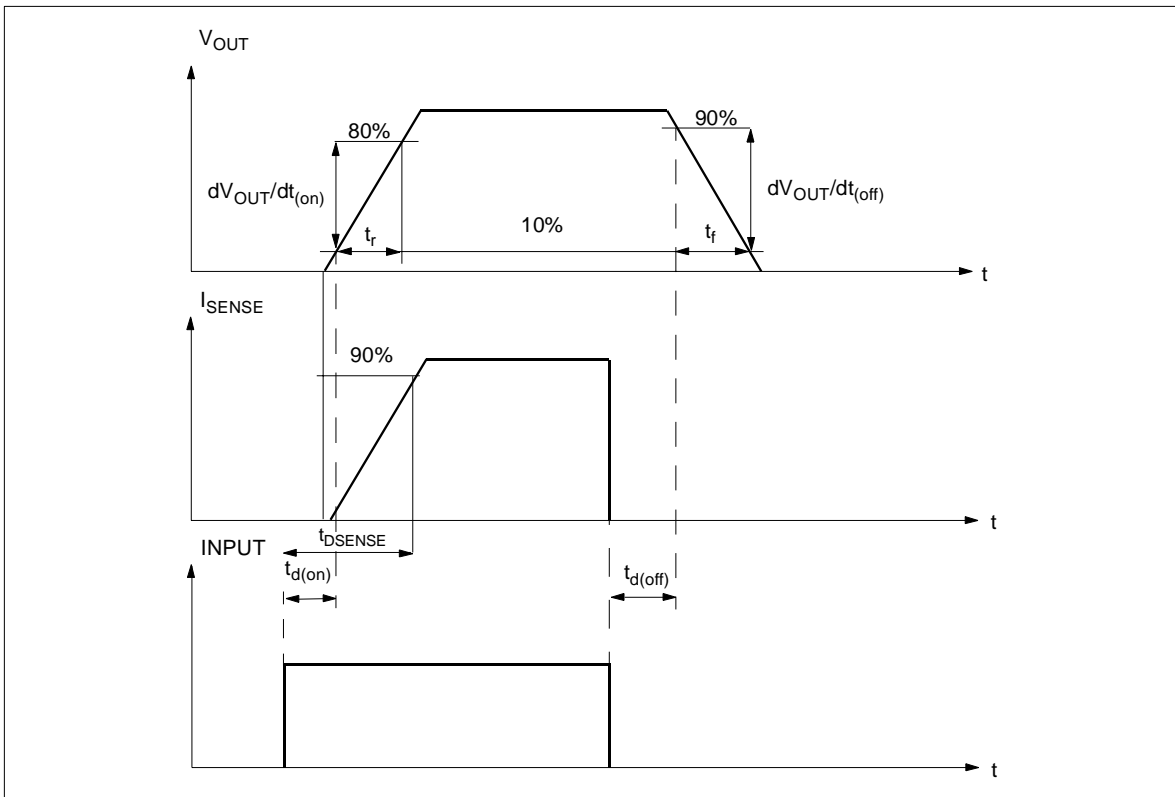
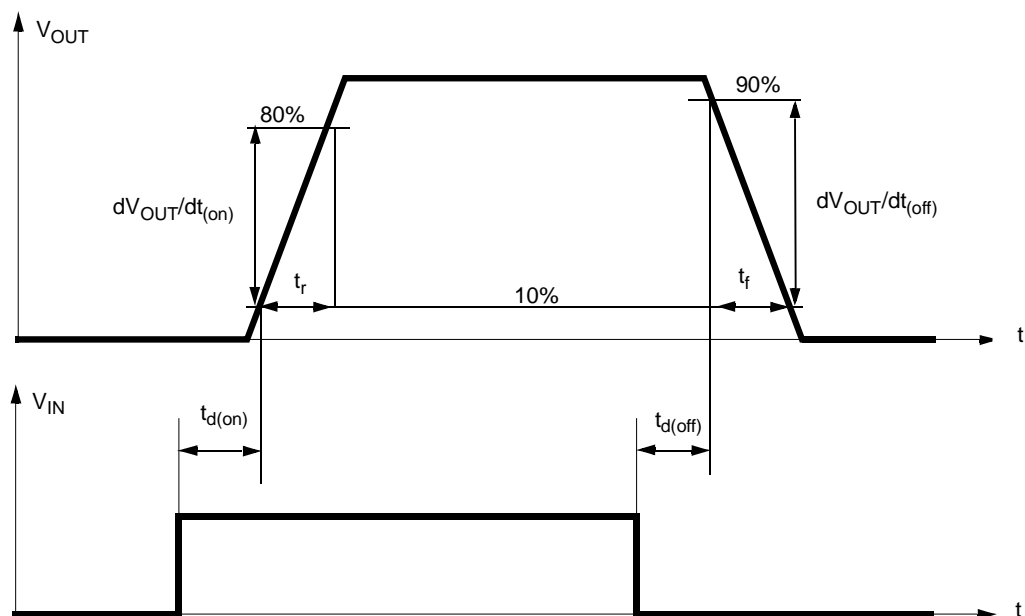


Figure 2: Switching Characteristics (Resistive load $R_L=1.3\Omega$)



Switching time Waveforms



TRUTH TABLE (Per each channel)

CONDITIONS	INPUT	OUTPUT	CURRENT SENSE
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD})$ 0 $(T_j > T_{TSD})$ V_{SENSEH}
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

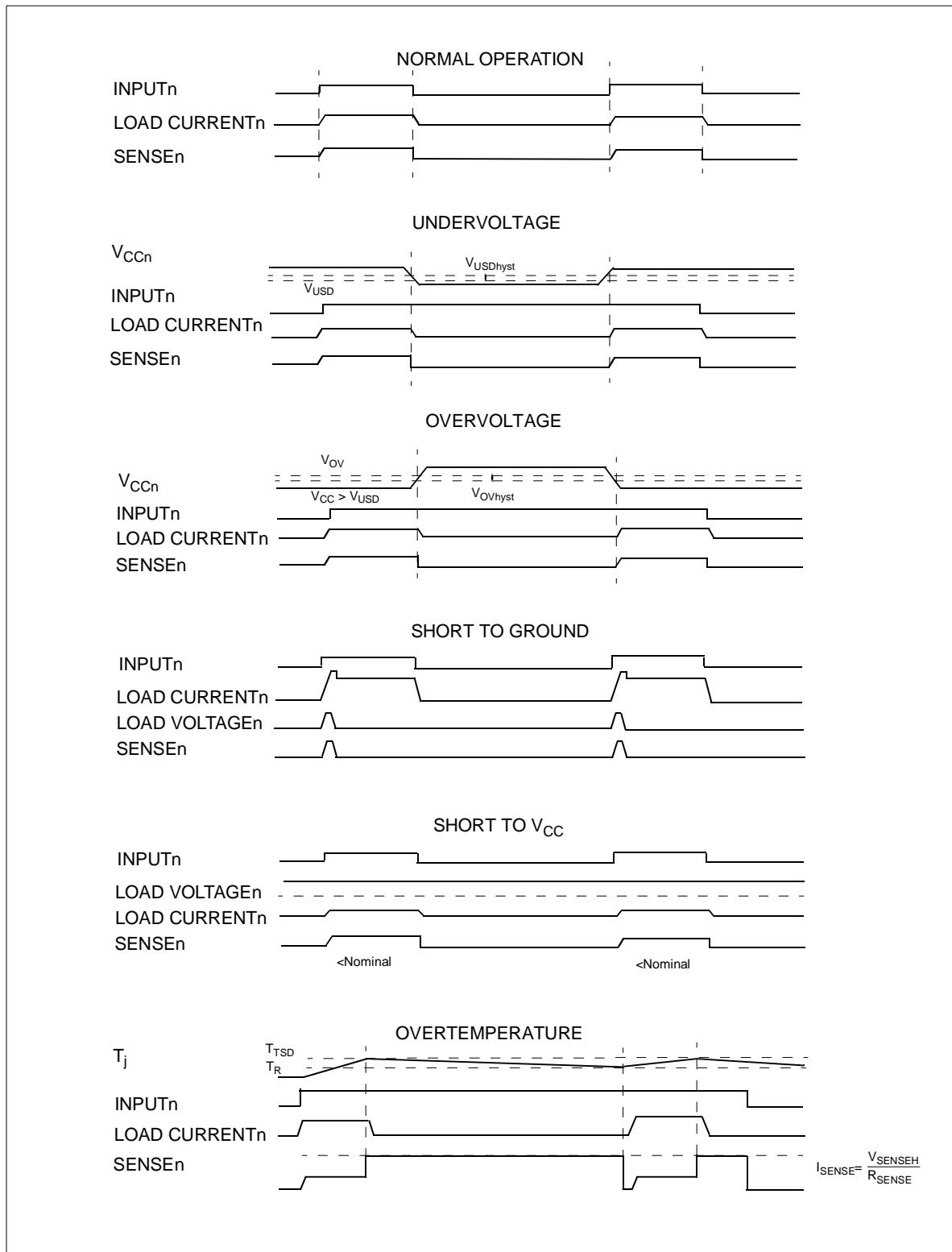
ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

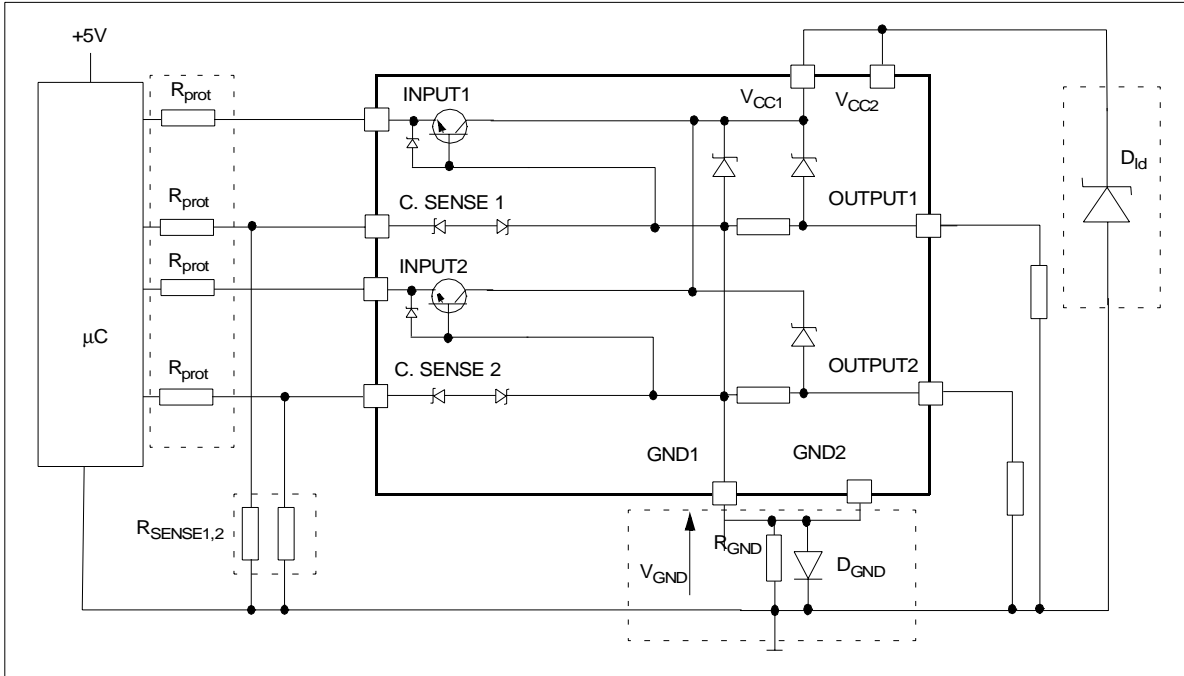
ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 3: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

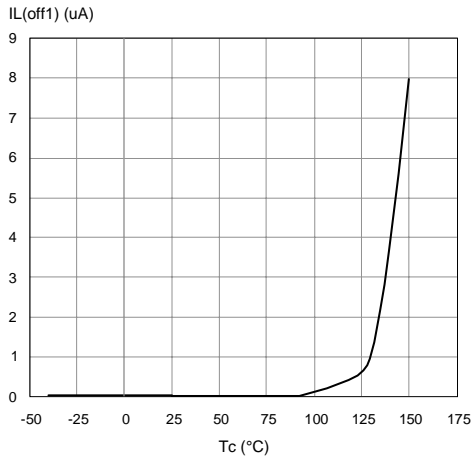
$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

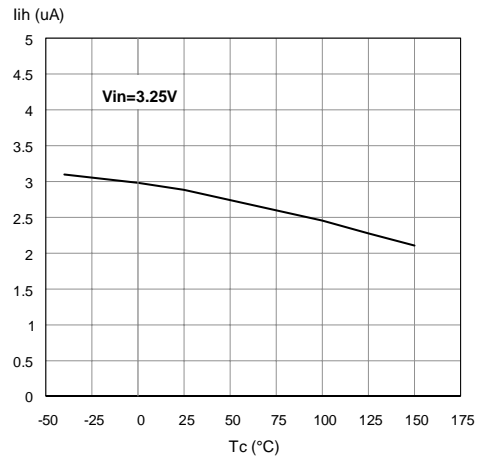
For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is $10\text{k}\Omega$.

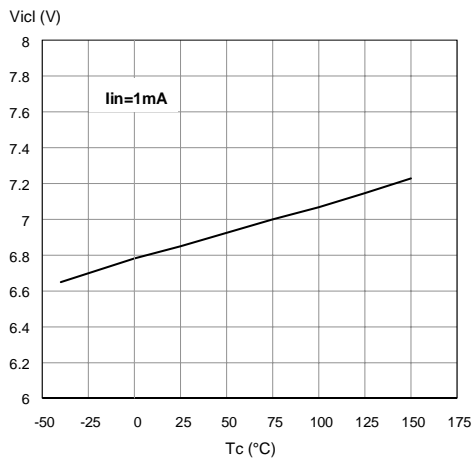
Off State Output Current



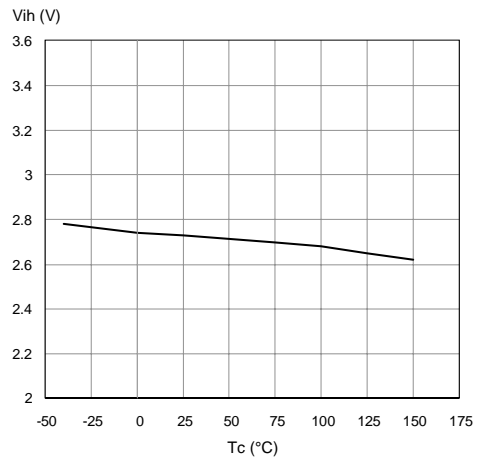
High Level Input Current



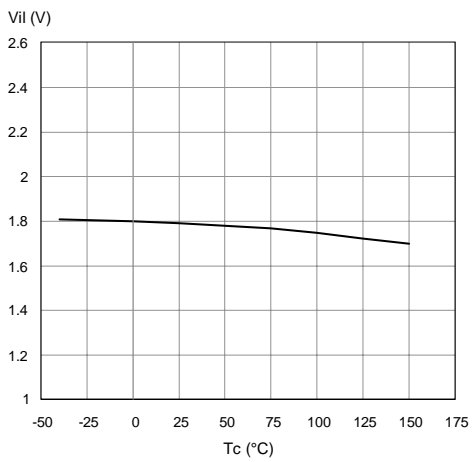
Input Clamp Voltage



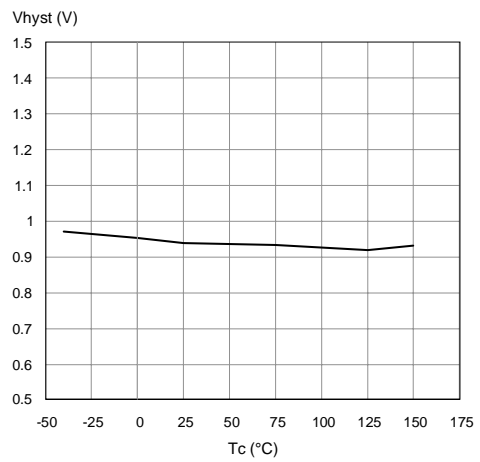
Input High Level



Input Low Level

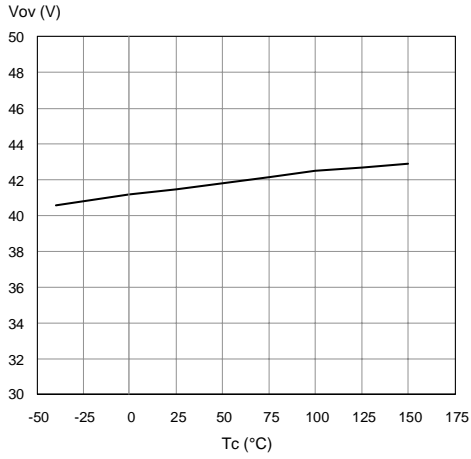


Input Hysteresis Voltage

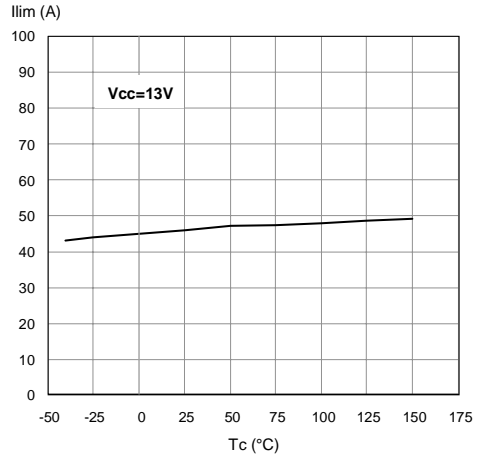


VND920P

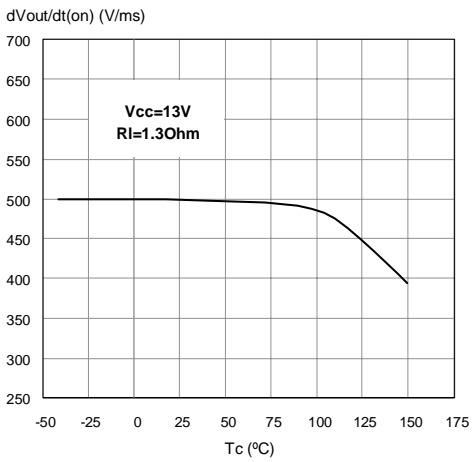
Overvoltage Shutdown



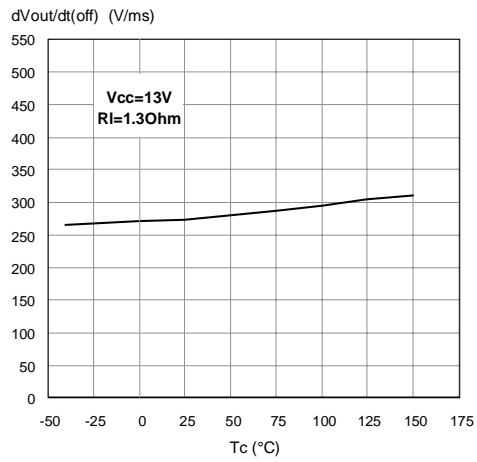
I_{LIM} Vs T_{case}



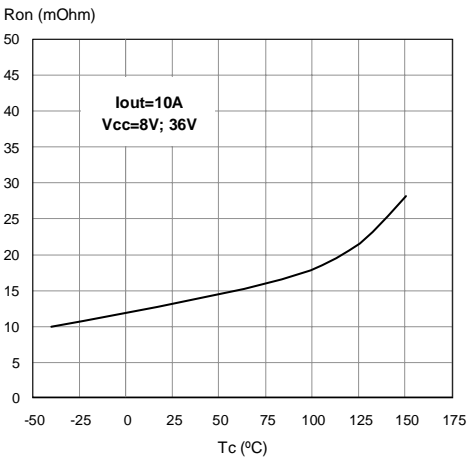
Turn-on Voltage Slope



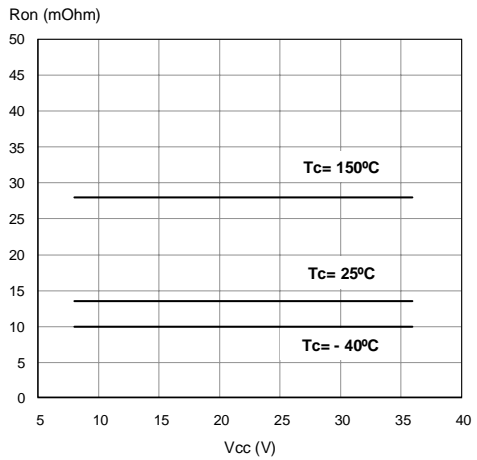
Turn-off Voltage Slope



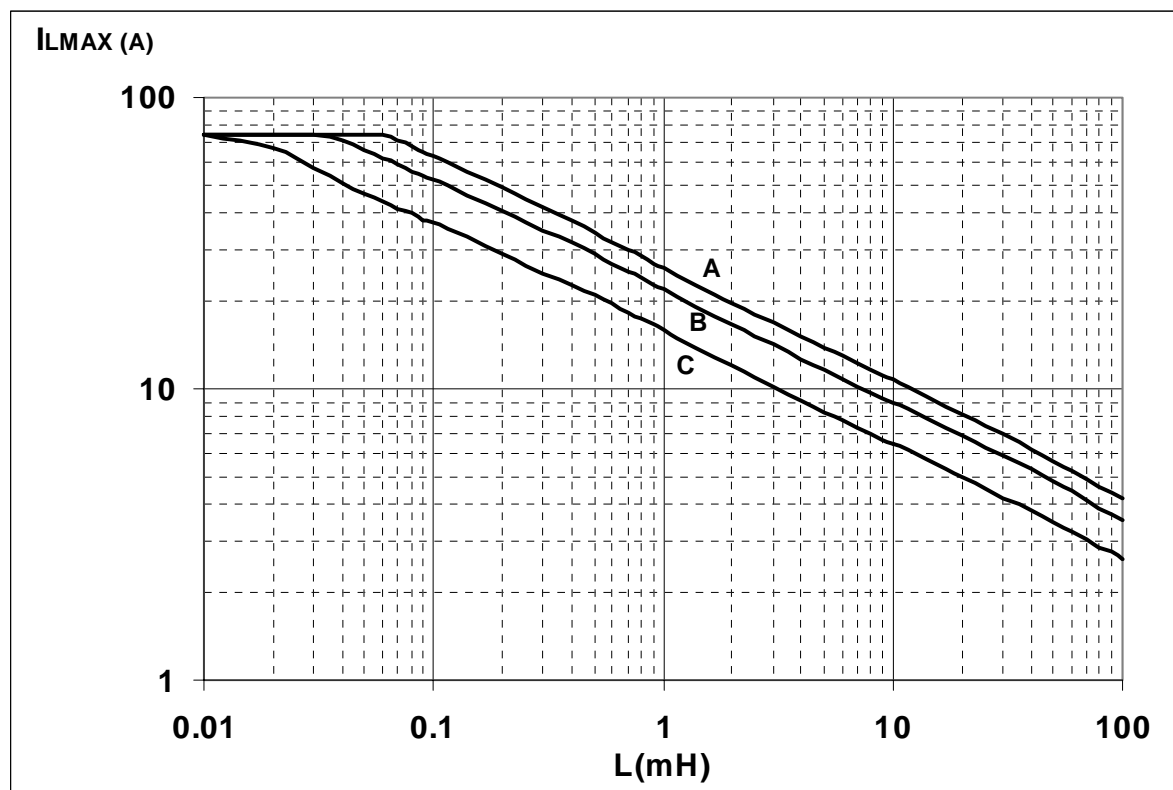
On State Resistance Vs T_{case}



On State Resistance Vs V_{CC}



Maximum turn off current versus load inductance



A = Single Pulse at $T_{Jstart}=150^{\circ}C$

B = Repetitive pulse at $T_{Jstart}=100^{\circ}C$

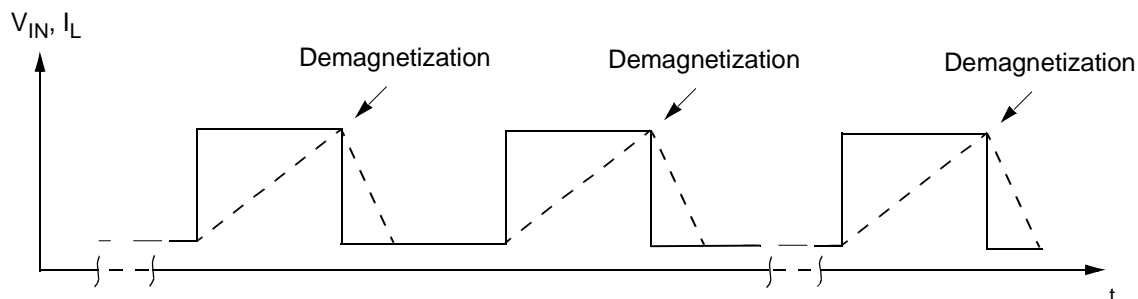
C = Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

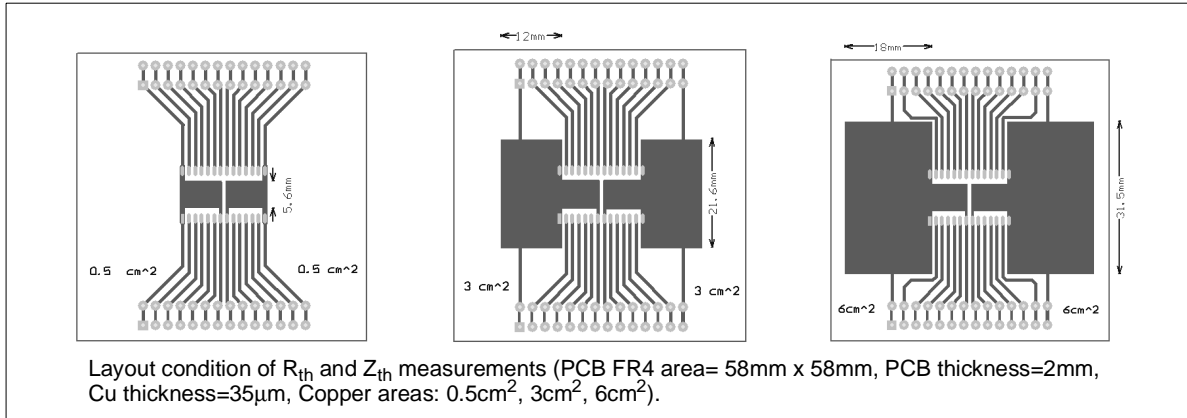
Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-28 DOUBLE ISLAND THERMAL DATA

SO-28 Double island PC Board

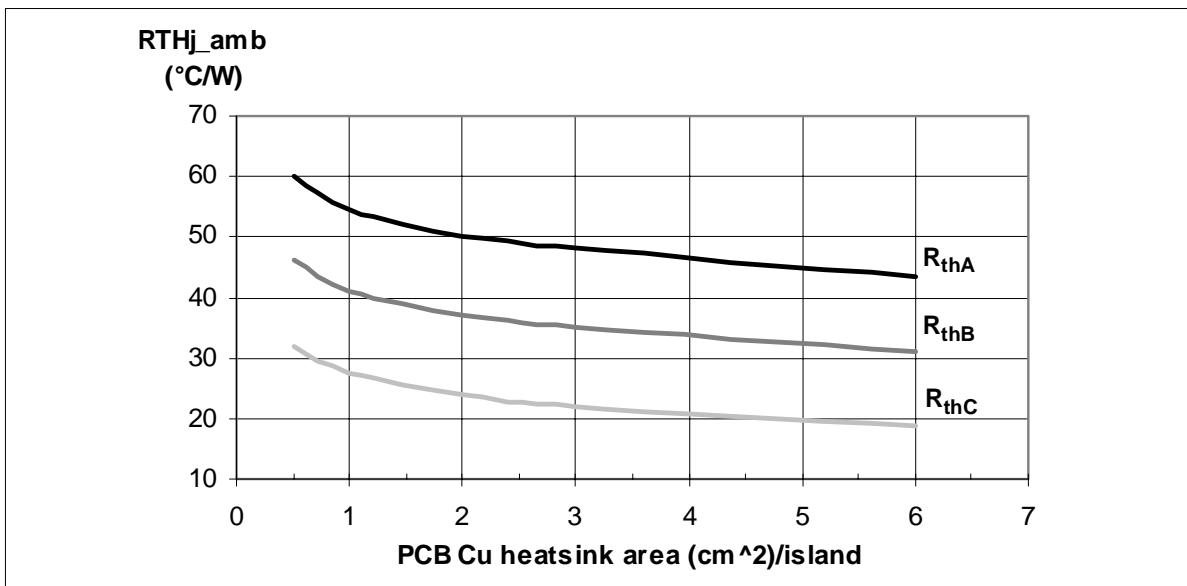


Thermal calculation according to the PCB heatsink area

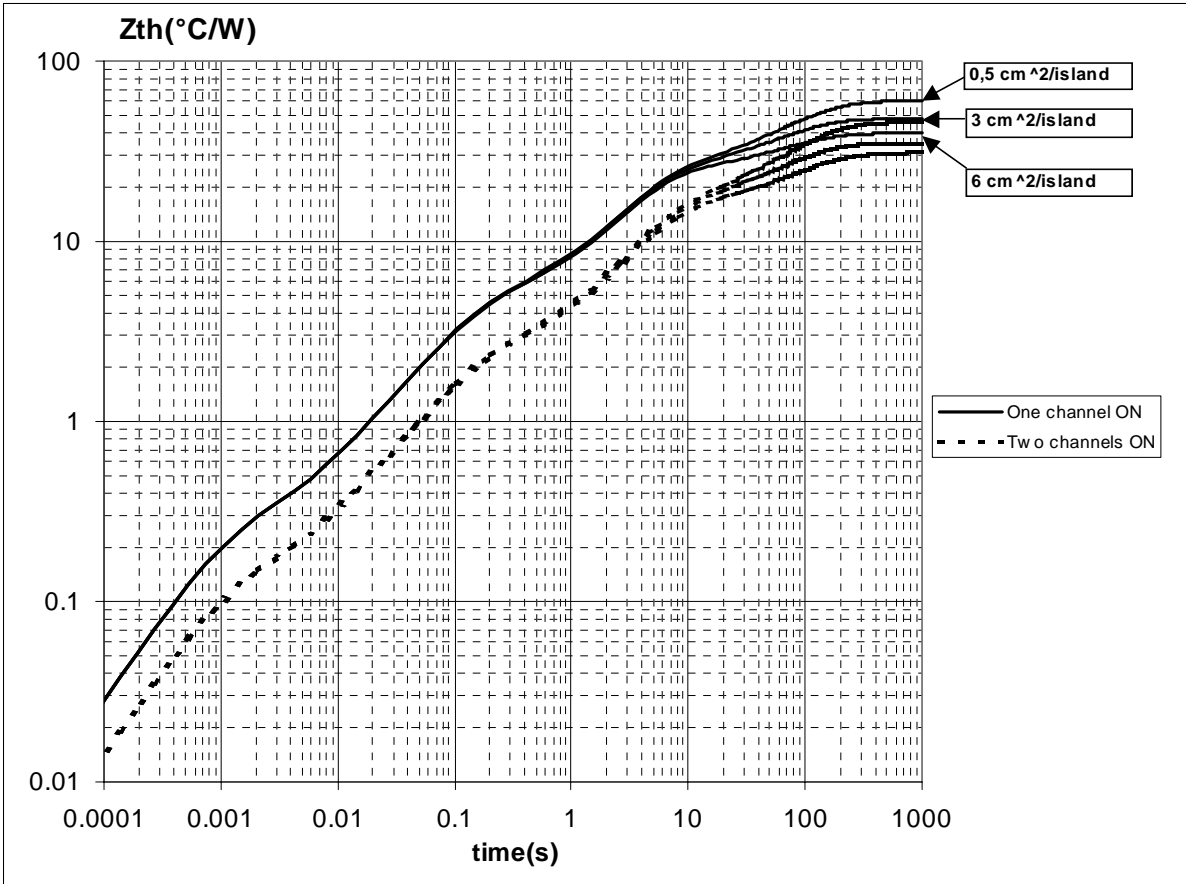
Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = Thermal resistance Junction to Ambient with one chip ON
 R_{thB} = Thermal resistance Junction to Ambient with both chips ON and $P_{dchip1} = P_{dchip2}$
 R_{thC} = Mutual thermal resistance

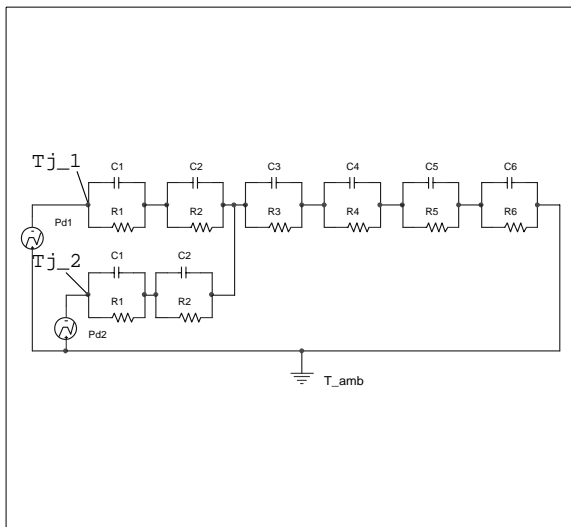
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



SO-28 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a two channels HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

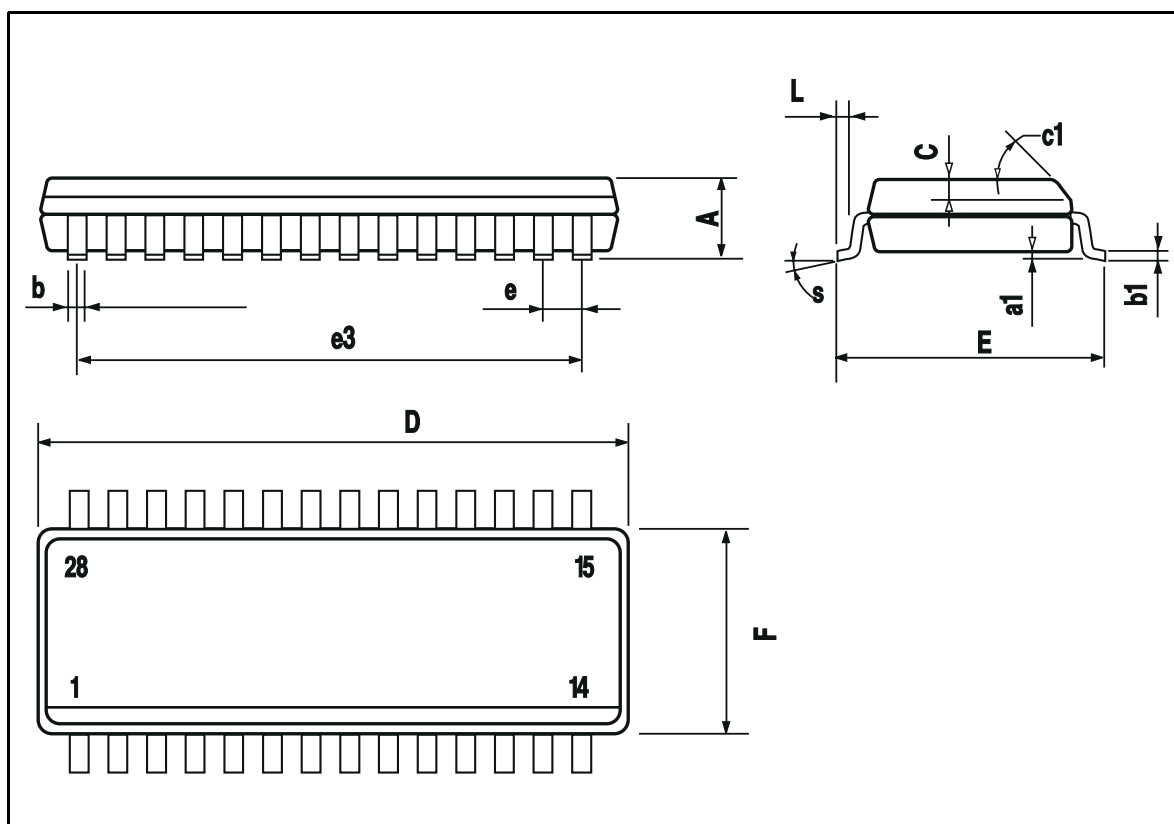
where $\delta = t_p/T$

Thermal Parameter

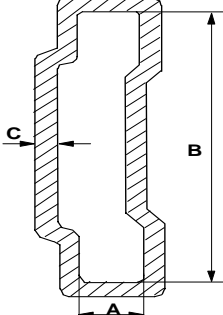
Area/island (cm ²)	0.5	6
R1= (°C/W)	0.02	
R2= (°C/W)	0.1	
R3= (°C/W)	2.2	
R4= (°C/W)	11	
R5= (°C/W)	15	
R6= (°C/W)	30	13
C1= (W.s/°C)	0.0015	
C2= (W.s/°C)	7.00E-03	
C3= (W.s/°C)	1.50E-02	
C4= (W.s/°C)	0.2	
C5= (W.s/°C)	1.5	
C6= (W.s/°C)	5	8

SO-28 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	17.7		18.1	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
S	8 (max.)					



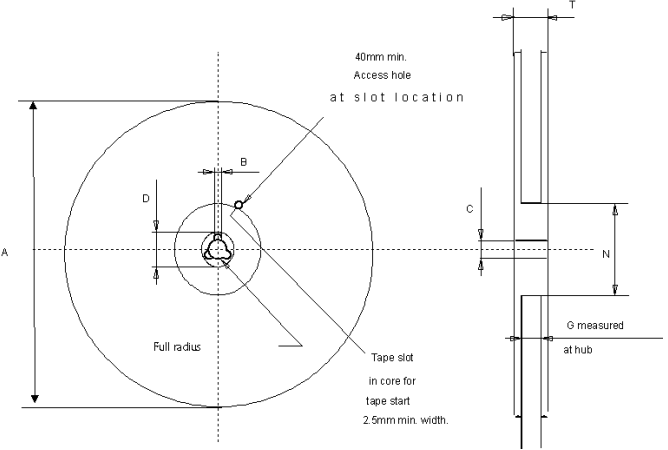
SO-28 TUBE SHIPMENT (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")

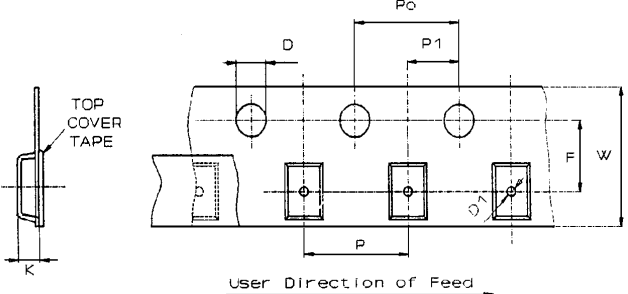


Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	16.4
N (min)	60
T (max)	22.4

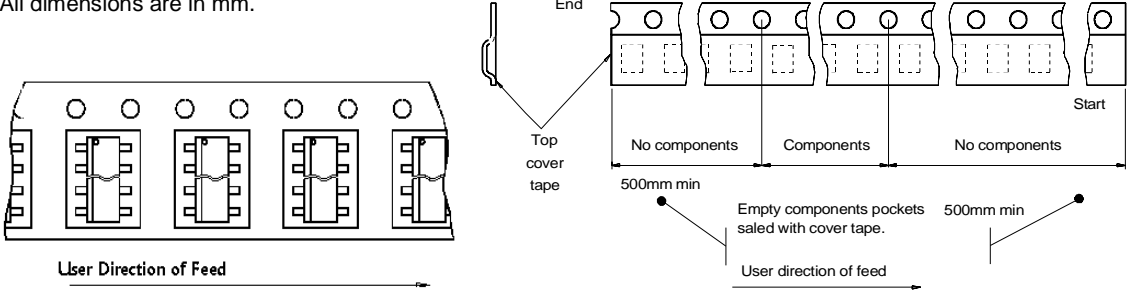
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2



All dimensions are in mm.



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